Impact of Random Telegraph Noise on the Precision of a Sub 20 ps Cyclic Vernier Time-to-Digital Converter

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Abstract

As CMOS scaling results in more frequent statistical occurrence of dominant Random Telegraph Noise (RTN) in MOSFET transistors, we analyse the severity of this phenomenon on the precision of high-resolution on-chip time measurement. The analysis is focused on a cyclic Vernier Time-to-Digital Converter (TDC) designed in 28 nm bulk CMOS with 15 ps LSB. RTN occurrence at various amplitudes obtained experimentally is modeled in the TDC circuit simulations. It is observed that the severity of consequences can reach from 1-2 LSB to a much larger error of 20 LSB. Further, in this speed-, area- and power-efficient cyclic Vernier architecture, the possible RTN-induced measurement error shows a complex pattern across the measurement dynamic range. This work highlights reliability concerns of high-precision time measurements in scaled CMOS process nodes due to the increasing probability of occurrence of the discrete noise patterns.

Index Terms

CMOS, MOSFET, Noise, Random Telegraph Noise (RTN), Random Telegraph Signals (RTS), Reliability, Time to Digital Converter (TDC),

I. Introduction

Time-to-Digital Converters are crucial for applications requiring precise time measurements, such as Time-of-Flight (ToF) sensors [1], Phase-Locked-Loops (PLL) [2], or Time over Threshold measurement e.g. in high-energy physics experiments [3]. They rely on accurately converting time intervals into digital values. Meanwhile, RTN, a phenomenon more and more significant in nanoscale CMOS [4] causes variations in the delay cells [5] [6]. When such fluctuation is present for example in a delay element of a cyclic TDC, it leads to changes in the oscillation frequency. In this work, we investigate the severity of such events on TDCs precision. Especially, we focus on circuits with nominal precision of several picoseconds. Such fast TDCs are enabled with CMOS scaling. To conduct these studies, we have designed a cyclic Vernier TDC in 28 nm CMOS, based on architecture presented in [7].

II. Time-to-Digital Converter Design

The resolution of most TDCs is limited by the minimum delay of the delay cells, which is dictated by the technology used [8]. To overcome this limitation, a cyclic Vernier topology is implemented. The resolution R is determined by the difference in oscillation periods between the fast and slow ring oscillators, as well as the number of signals compared by the arbiters during a single oscillation period τ_S and τ_F as shown in (1). In this case, eight signals from the slow oscillator (S1-S8) and the fast oscillator (F1-F8) are compared.

$$R = \frac{(\tau_S - \tau_F)}{8} \tag{1}$$

Fig. 1 presents the block diagram of a cyclic Vernier TDC. As shown in Fig. 2, the TDC operates synchronously with a 40 MHz clock signal. Once a conversion is completed, the TDC is ready to initiate a new conversion on the next rising edge of the clock, as indicated by the signal TDC_READY. The measurement period is defined by the duration of the TDC_IN pulse.When the rising edge of TDC_IN occurs, the slow ring oscillator is triggered, causing the slow counter to increment with each cycle. The fast ring oscillator is triggered by the falling edge of TDC_IN, incrementing the fast counter with each cycle. The fast oscillator progressively catches up to the slow oscillator by one least significant bit (LSB) per delay element. The arbiter compares the signals from the slow ring oscillator ($S1-S8$) with those from the fast ring oscillator ($F1-F8$) and identifies the position, P, where the fast oscillator catches up with the slow oscillator, marking the end of the conversion. At this point, indicated by the signal EOC, both ring oscillators (ROSCs) are halted. The time is then calculated using (2), which

considers the number of cycles from both the slow counter, N_S, and the fast counter, N_F, as well as the position, P (ranging from 1 to 8), where alignment is detected by the arbiter. The time constants τ_S and τ_F represent the oscillation periods of the slow and fast ring oscillators, respectively.

$$TDC_{out} = (N_S - 1) \cdot \tau_S - (N_F - 1) \cdot \tau_F + \frac{P \cdot (\tau_S - \tau_F)}{8} \tag{2}$$

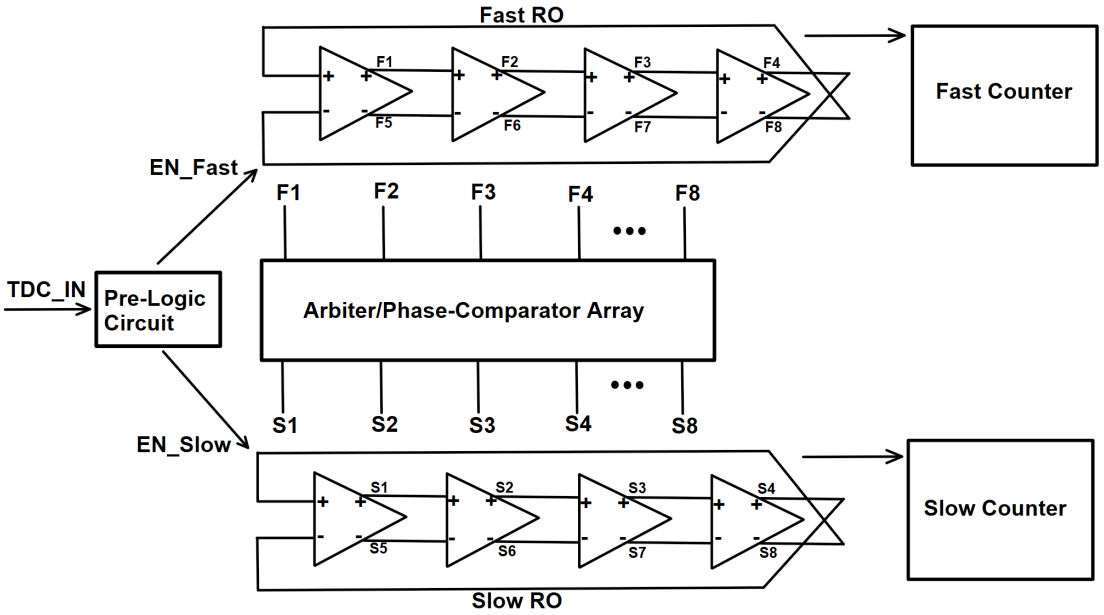

Fig. 1. Time-to-Digital Converter Block Diagram

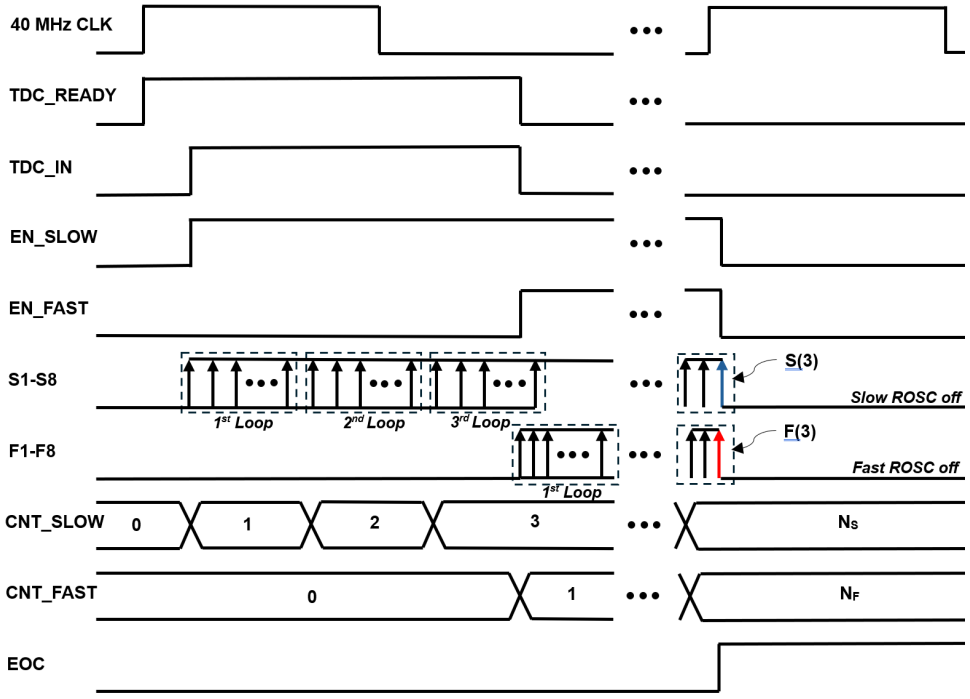

Fig. 2. Time-to-Digital Timing Diagram

Table I provides a comprehensive overview of the key performance parameters for the TDC. Based on simulations, the TDC demonstrates an average power consumption of $243.8\mu W$, indicating efficient energy usage for the given performance requirements. Additionally, the simulations reveal a maximum differential nonlinearity (DNL) of 1.57 LSB and an integral

TABLE I
TDC PERFORMANCE PARAMETERS

TDC Performance Parameters			
Tech.	***Arch.***	***LSB [ps]***	***DNL [LSB]***
28nm bulk CMOS	Cyclic Vernier	15	1.57
Power $[\mu W]$	**Area** μm^2	***Range [ns]***	***INL [LSB]***
243.8	1120	25	2.93

nonlinearity (INL) of 2.93 LSB. Furthermore, the design achieves a resolution of 15 picoseconds (ps), making it well-suited for high-precision applications that demand fine time measurement capabilities.

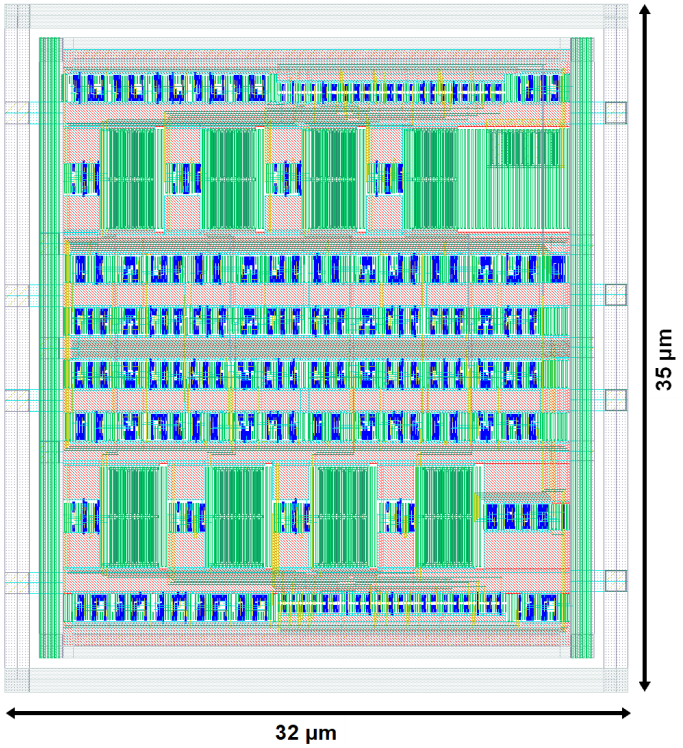

Fig. 3. Time-to-Digital Converter Layout

TABLE II
LAYOUT INFLUENCE

	Layout influence on oscillation frequency		
	f_{slow} ***[MHz]***	f_{fast} ***[MHz]***	***Resolution [ps]***
Pre-Layout	629.5	668	11.5
Post-Layout	258.5	266.8	15

The block layout in 28 nm CMOS process is shown in Fig. 3 and the oscillator frequencies along with the resulting TDC nominal precision are summarized in Table II. The pre-layout oscillation frequencies of the slow and fast oscillators are $f_{slow} = 629.5MHz$ and $f_{fast} = 668MHz$, yielding a resolution of 11.5 ps. Post-layout simulations indicate frequencies of $f_{slow} = 258.5MHz$ and $f_{fast} = 266.8MHz$, resulting in a resolution of 15 ps.

III. RANDOM TELEGRAPH NOISE

For over 50 years, RTN has been a concern in complementary metal oxide semiconductor (CMOS) technologies, growing in significance with process scaling. In nanoscale CMOS devices charge trapping and de-trapping activities at the $SiO_2 - Si$ interface [9], [10] present significant abrupt fluctuations in drain-current (I_D). It can be associated with variations in charge number, but also in local mobility fluctuations. Each RTN event is characterized with three specific parameters observable in the time domain: (A) RTN amplitude, defined as difference between two distinguishable levels in the I_D signal; a two-level

threshold voltage (ΔV_{TH}) that results in observed ΔI_D pattern is a commonly accepted model of RTN amplitude, (B) capture time (τ_c), the time spent at the high level of the RTN signal, (C) emission time (τ_e), the time spent at the low level of the RTN signal. In N-channel MOSFET if RTN is of acceptor type, it results in smaller than the nominal drain current, whereas a donor trap center causes a larger one. In P-channel MOSFET it is the opposite.

From single device observations, researchers have conducted essential RTN analyses to understand RTN characteristics. Specifically in 28 nm devices we have shown that in minimum size devices RTN amplitudes ($\Delta I_D/I_D$) of 2 % are common [11]. Also, in our experiments we have observed rare more dominant events. Further, our previous work [12] reports that RTN amplitude ($\Delta f/f_{mean}$), investigated statistically in a larger process node 40 nm CMOS using an array of Ring Oscillators (ROSC), can reach up to 26 %.

Furthermore, it is commonly accepted fact that RTN-induced signals have Lorentzian shape characteristics in Power Spectral Density (PSD), which can be observed with a dominant capture and emission time constant ($\tau_{c//e}$) region from milliseconds to microseconds. Given these specifications, we have analyzed how precision of the cyclic Vernier TDC, discussed in the previous Section, is influenced by RTN with given amplitudes. Considering that the capture and emission times are much longer than the nanosecond-range TDC conversion time, we work with two RTN cases: a trapped state and a de-trapped state.

TABLE III
IMPACT OF RTN ON RING OSCILLATIOR FREQUENCY

NMOS	Change in f_{OSC} due to RTN				
	0mV	***10mV***	***20mV***	***30mV***	***40mV***
f_{slow} [MHz]	629.5 (0%)	630.4 (+0.14%)	631.2 (+0.27%)	632 (+0.40%)	632.8 (+0.52%)
f_{fast} [MHz]	668 (0%)	668.9 (+0.13%)	669.8 (+0.27%)	670.7 (+0.40%)	671.5 (+0.52%)
PMOS	**Change in f_{OSC} due to RTN**				
	0mV	***10mV***	***20mV***	***30mV***	***40mV***
f_{slow} [MHz]	629.5 (0%)	627.2 (-0.37%)	626.1 (-0.54%)	624.8 (-0.75%)	623.4 (-0.97%)
f_{fast} [MHz]	668 (0%)	666.8 (-0.18%)	665.5 (-0.37%)	664.1 (-0.58%)	662.8 (-0.78%)

IV. ANALYSIS OF RTN ON TDC PRECISION

A. Impact of RTN on the ring oscillators

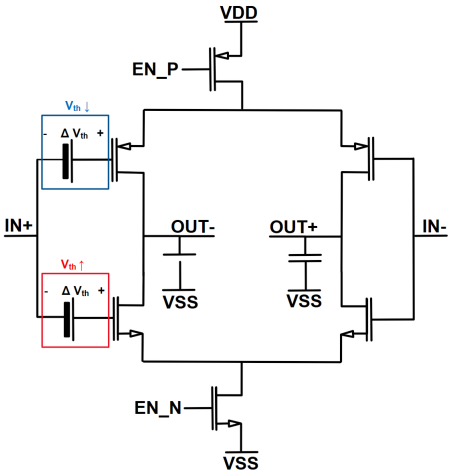

Fig. 4. RTN inside delay cell

We introduced RTN at various positions in the TDC. Following the expected amplitudes in minimum size devices and the threshold voltage, the relevant RTN model is obtained by shifting V_{TH} level by 10 mV, 20 mV, 30 mV and 40 mV. The model is simplified, as it is obtained by inserting a voltage source in the gate path of a MOSFET concerned, as shown in Fig. 4. The results showed that while the arbiter and counters exhibit good resilience against RTN, the delay elements of the ring oscillator are significantly affected. Each delay element in the ring oscillator consists of a pair of differential inverters. Donor type RTN was applied at the input of the first stage in both the fast and slow ring oscillators, as illustrated in Fig. 4. It causes a mismatch between the delay cells, because of the RTN character this mismatch is temporary. This results in a change in the oscillation frequency, causing the ring oscillator to become faster or slower, depending on whether RTN occurs in the N- or P-channel MOSFET, as shown in Table III. It should be noted that currently our design doesn't include a phase locked loop (PLL) to stabilize the oscillation frequencies. In a circuit with feedback loop the probability of observing the effects discussed further below depends on the frequency of the PLL low-pass loop filter. On the other hand it should be considered that our observations [12] have shown a higher probability of dominant RTNs at lower power supply level in a cyclic delay line. Meanwhile insertion of PLL is unavoidably associated with a lower voltage drop across the delay element.

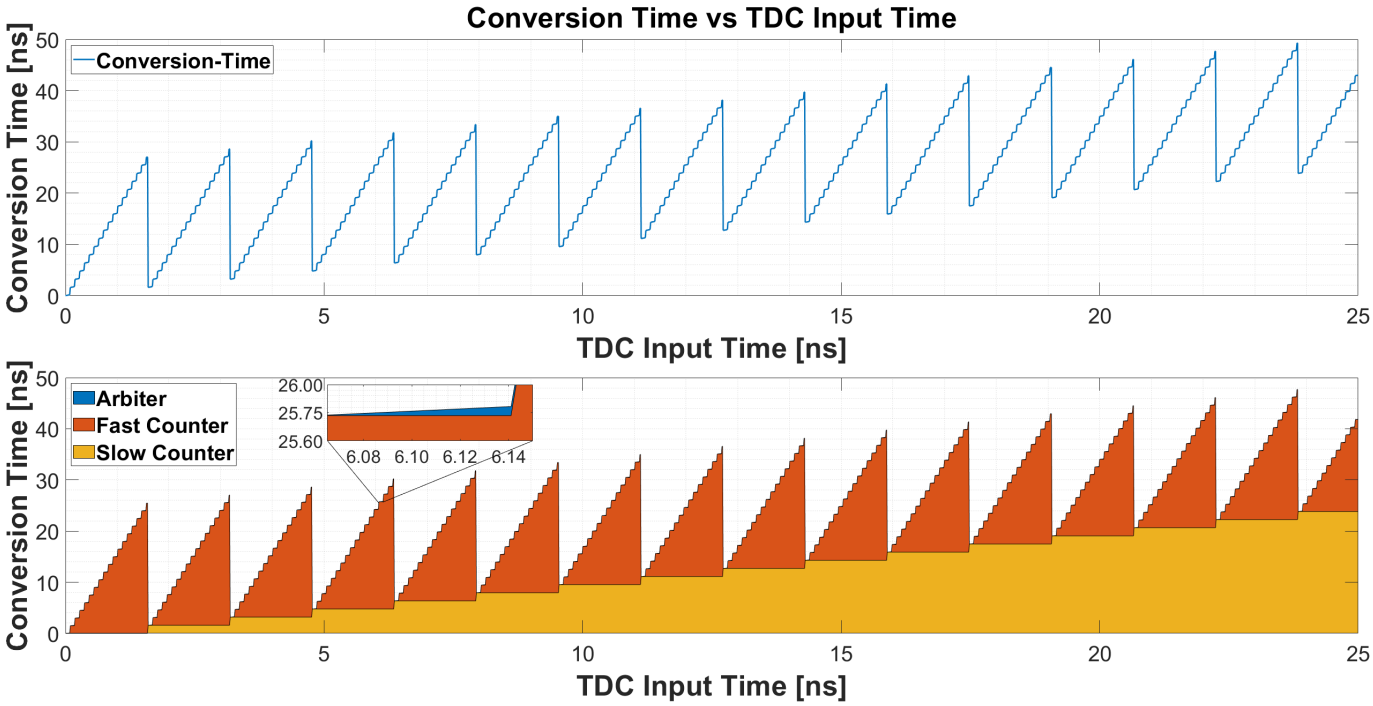

Fig. 5. Conversion Time vs TDC Input Time

B. Correlation between RTN and conversion time

Since RTN introduces mismatches between the delay cells, the fast ring oscillator requires varying amounts of time to catch up with the slow ring oscillator, leading to different counter values. The time shift caused by the mismatch accumulates with each oscillation cycle. Therefore, RTN has the most significant impact on the output code during long conversion times.

The conversion time of a cyclic Vernier TDC strongly depends on the input time and increases with it, as illustrated in Fig. 5. The conversion time is shortest when the input time is a multiple of the oscillation period of the slow ring oscillator, as no fine quantization is necessary. In this case, the TDC output time is determined solely by the value of the slow counter. Conversely, the conversion time increases significantly when the fast ring oscillator requires many cycles to catch up with the slow ring oscillator. The contribution of the arbiter to the conversion time is minimal and insignificant for RTN.

TABLE IV
IMPACT OF RTN ON OUTPUT CODE

	Change in Output Code due to RTN				
3.3ns	***0mV***	***10mV***	***20mV***	***30mV***	***40mV***
Arbiter	00000100	00000100	00000100	00000100	00000100
Counter Slow	00100	00100	00100	00100	00100
Counter Fast	00010	00010	00010	00010	00010
Output Code	287	287	287	287	287
	Change in Output Code due to RTN				
8.4ns	***0mV***	***10mV***	***20mV***	***30mV***	***40mV***
Arbiter	00100000	00100000	00010000	00001000	00001000
Counter Slow	01010	01010	01010	01010	01010
Counter Fast	00101	00101	00101	00101	00101
Output Code	729	729	728	727	727
	Change in Output Code due to RTN				
15.2ns	***0mV***	***10mV***	***20mV***	***30mV***	***40mV***
Arbiter	00001000	00000100	00000001	01000000	00100000
Counter Slow	10011	10011	10011	10010	10010
Counter Fast	01010	01010	01010	01001	01001
Output Code	1320	1319	1317	1314	1313
	Change in Output Code due to RTN				
23.8ns	***0mV***	***10mV***	***20mV***	***30mV***	***40mV***
Arbiter	00000010	01000000	00001000	01000000	01000000
Counter Slow	11111	11110	11110	11101	11101
Counter Fast	10001	10000	10000	01111	01111
Output Code	2066	2063	2060	2058	2054

However, as Fig. 6 illustrates, in case of RTN present in the oscillators the impact can be from several LSB, and in the worst simulated cases reach even 20 LSB at longer conversion times. Also because of the architecture-specific conversion

pattern, from Fig. 5, also the severity of RTN influence pattern is non-monotonous and already at short measured time intervals precision degradation is shown. We list details of selected input time intervals in Table IV as a supporting explanation. The output code of the arbiter, the slow- and the fast oscillator are shown without RTN (0 mV amplitude in the modeled threshold voltage shift) and with RTN at four simulated amplitude levels.

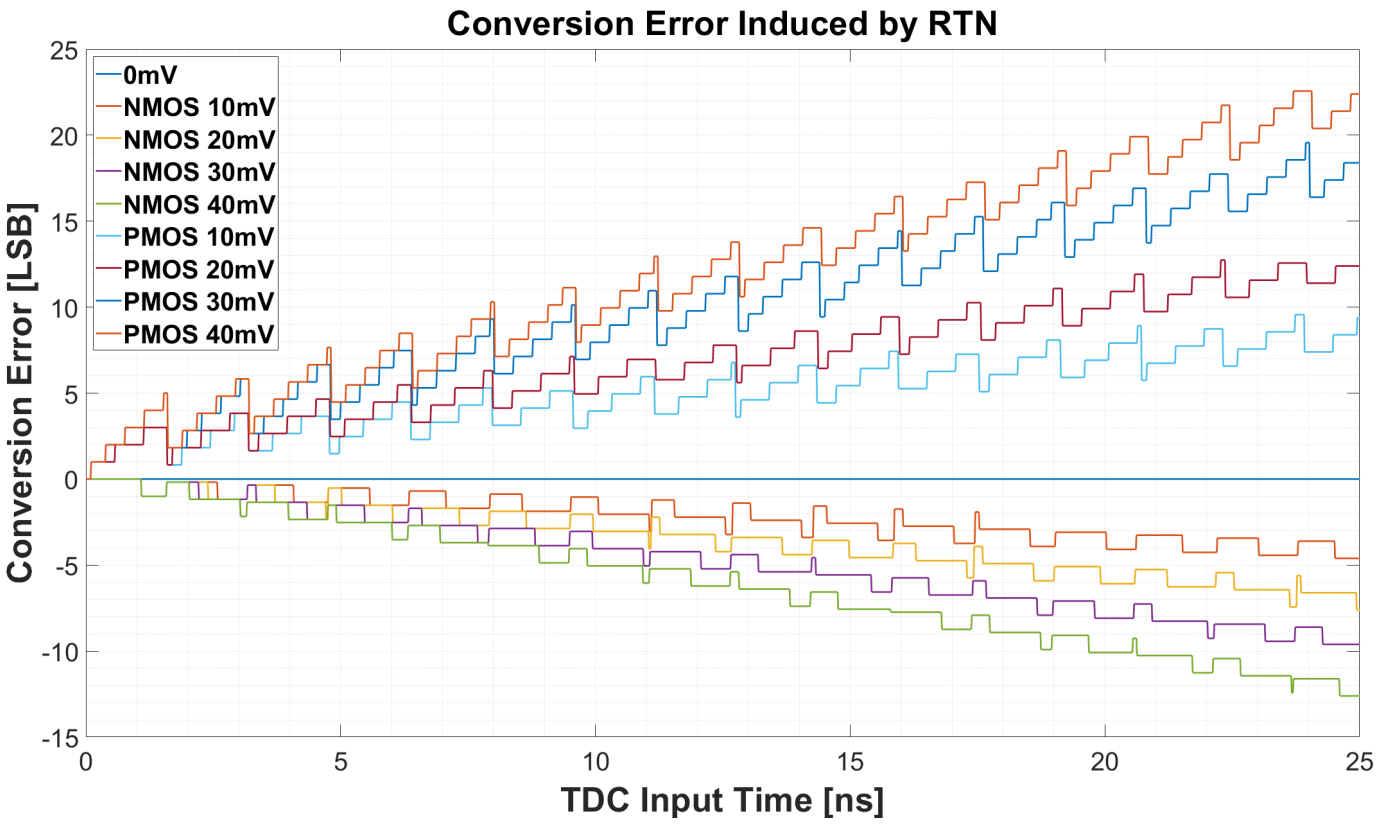

Fig. 6. Conversion Error Induced by RTN localized in the first stage of the fast oscillator, 2 cases with donor RTN center in n-channel and p-channel MOSFET

V. Conclusions

We have studied the impact of RTN on the precision of a cyclic Vernier time to digital converter, designed in 28 nm bulk CMOS process. The values for RTN amplitudes are based on noise measurements on single MOSFET in 28 nm and 40 nm CMOS, where values of 5-10% are not uncommon. It was shown that for TDCs with nominal (post-layout) LSB of 15 ps, common RTN events equivalent to threshold voltage of 10 mV (corresponding to 2% of the nominal value) can cause degradation in the range of 5 LSB. For more dominant RTNs, in the range of 10% this number may be around 20 LSB. Significantly, in this cyclic Vernier architecture, the pattern of the error does not increase monotonously with the measured time interval. According to our study, the shorter measured time intervals can already experience a considerable degradation in the measurement precision. The simulations assumed a single occurrence of RTN in the circuit. In reality, there may be a chance of no such trapping/detrapping center. However, the trend in nanometer technology nodes suggests that multiple RTNs may likely coexist in the same circuit.

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