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Signal Integrity of a High-Speed SERDES Interface

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Kurzfassung

Steigende Datenraten in elektrischen Systemen stellen Leiterplattenentwicklungen für Ingenieure vor große Herausforderungen. Insbesondere Fragen der Signalintegrität sind heutzutage ein wesentlicher Aspekt von Hochgeschwindigkeitsschnittstellen. Aus diesem Grund müssen Ingenieure die Auswirkungen auf die Signalintegrität kennen und wissen wie sie diese vermeiden oder reduzieren können. Diese Arbeit bewertet die wichtigsten Signalintegritätseffekte, welche bei High-Speed PCB Schnittstellen auftreten.

Im ersten Schritt wird der Einfluss der wichtigsten Signalintegritätseffekte Dämpfung, Übersprechen und Impedanzanpassung ermittelt. Hierzu wurden Berechnungen und Simulationen mittels RF-Simulationssoftware eingesetzt. Die Simulation zeigt, dass Übersprechen leicht verhindert werden kann, indem der Abstand zwischen den Übertragungsleitungen vergrößert wird. Die Berechnung der Leitungsimpedanz unter Berücksichtigung der von den Herstellern angegebenen Fertigungstoleranzen ergab, dass die reale Leitungsimpedanz bis zu 10 % von der gewünschten abweicht. In einem zweiten Schritt werden TDR-Messungen durchgeführt, um die Leitungsimpedanz und S-Parameter eines realen Hardwaredesigns zu bestimmen. Diese Messungen zeigen, wie Hardwaredesigns auf Korrektheit und Produktionsqualität überprüft werden können. Dieser Prozess ist für die Herstellung zuverlässiger Systeme vorteilhaft.

Mit diesen Schritten ist es möglich, Leiterplattenschnittstellen zu entwerfen, die mit 10 Gbit/s und höher arbeiten. Weiters ist es auch möglich, fertige Designs auf ihre Übereinstimmung mit den Anforderungen zu überprüfen. Um den Designprozess von Hochgeschwindigkeits-Leiterplatten weiter zu verbessern, wäre eine 3D-EM-Simulation ein geeigneter nächster Schritt. Auch die Untersuchung spezieller Leiterplattenmaterialien kann zu noch besseren Ergebnissen hinsichtlich der Signalintegrität führen.

Abstract

Raising data rates in electrical systems are making PCB developments very demanding for engineers. In particular, signal integrity issues are an essential aspect of high-speed interfaces nowadays. For this reason, engineers must know signal integrity effects and how to avoid or reduce them. This thesis evaluates the most common signal integrity effects on high-speed PCB interfaces.

In a first step, the impact of the primary signal integrity effects on attenuation, cross-talk, and impedance matching is determined. Therefore, calculations and simulations with RF simulation software were used. The simulation shows that cross-talk can be easily prevented by getting more distance between transmission lines. The calculation of the line impedance applied with the manufacturing tolerances given by manufacturers shows that the real line impedance varies up to 10 % from the desired one. In a second step, TDR measurements were done to determine line impedance and S-parameters of an actual hardware design. These measurements show how hardware designs can be checked for correct design and production quality. This process is beneficial for manufacturing reliable systems.

With these steps, designing PCB interfaces working at 10 Gbit/s and higher is possible. Furthermore, it is possible to verify final designs for their compliance with the requirements. A proper next step would be to improve the design process of high-speed PCBs 3D-EM simulation further. Also, the investigation of specialized PCB materials can lead to better results in terms of signal integrity.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

In recent years, technologies like 5G or UWB have been developed and integrated into millions of devices. What modern technologies like these have in common is that they often use very high frequencies for communication. Frequencies of up to 10 GHz are already state-of-the-art. Such high frequencies make developing devices using such transmission standards very challenging.
Testing and developing such high-frequency technologies require special measurement equipment. Such measurement devices have to sample and process immense amounts of data in a very short time. A UWB pulse is, for example, about 2 ns long [5]. More than two sampling points are necessary within these 2 ns to get an acceptable measurement. This results in a sample rate of multiple Giga samples per second.
State-of-the-art data converters provide sample rates of up to 10.4 GSPS with a resolution of up to 12 Bit [20]. Sampling with these parameters creates up to 125 Gbit of recorded data within one second. High-speed interfaces are necessary to get this amount of data from sampling devices to a device that can process the data (e.g., an ASIC or FPGA).
This thesis handles the design of high-speed interfaces on printed circuit boards (PCBs). Various topics regarding high-speed chip interfaces are addressed. The physical effects on multi-gigabit signals, the manufacturing of the interconnects, and given boundary conditions. An approach on how to design such an interface is made. It shows the necessary steps and considerations when designing high-speed components and implementing a high-speed interface. High-speed electronics design is an essential topic for future designs since more and more high-frequency applications will be developed. Therefore, much knowledge is necessary. Information about all components of such a design and the most important effects that can arise on such systems need to be well known. This knowledge makes it possible to create designs that are robust and run stable. Also, the effect on other systems can be estimated better, and interference between various components can be prevented.
Therefore, a wide knowledge of signal integrity and designing for high-frequency applications when designing electronic hardware is good.

Chapter 2

Signal Integrity

Gary Breed defines signal integrity as the "effect of all the impairments to a digital signal's waveform as it travels between the active devices in a circuit or system" [15]. So, signal integrity is about distorting effects on digital signals when traveling through a system.
Many effects can distort an electrical signal. Signal integrity is an important topic, especially for digital signals. Digital signals always contain high-frequency signal portions due to the square signal's steep rise and fall times. If the design of a digital interface is not handled carefully, the communication between two devices can get distorted. For a bad design, a square signal sent by a transmitter could look like the trace shown in Figure 2.1. Figure 2.1 shows a 300 MHz clock (square signal) at the end of a 50 cm transmission line that is running over three different boards.

Electric circuit designers must be aware of signal integrity to avoid this kind of distortion. Especially if signal lines are long compared to the clock rate, signal integrity issues are problematic [12]. A rule of thumb from Eric Bogatin [12] gives an estimated value of what long means in terms of SI (Equation 2.1). This rule defines a critical length based on the bandwidth (in the form of the rise time) and the physical dimension of the system. An engineer should pay special attention to signal integrity for signals where the time the signal travels along a transmission line (TD) gets higher than one-third of the rise time (RT).

$$TD < 1/3 \cdot RT \tag{2.1}$$

When spending effort on good SI design, there are three main aspects to consider. One is attenuation along a transmission line. The second one is reflections on transmission lines. Therefore, the characteristic impedance and source and load impedances must be considered. The third cause of SI problems is cross-talk between neighboring transmission lines.

2.1 Fundamentals

2.1.1 Impedances

According to Eric Bogatin, all main signal integrity problems can be explained based on impedance [12]. So, to discuss signal integrity first, the term impedance has to be clarified.

Figure 2.1: Example of a distorted digital signal. 300 MHz clock measured at the receiver input at the end of a 50 cm long fragmented transmission line.

Impedance is defined as the ratio between voltage and current, as shown in Equation 2.2. The impedance defines the ratio of the magnitudes of U and I and the phase offset between U and I in case an AC signal is applied.

$$Z = \frac{U}{I} \tag{2.2}$$

With the impedance definitions of the three ideal elements

- Resistors (R)
- Capacitors (C)
- Inductors (L)

passive networks and equivalent circuits can be defined. These three elements are also called lumped elements because they are seen as ideal elements without any parasitics caused by their physical dimensions or structure.

Resistors

The ohmic law defines the resistance of a resistor:

$$R = \frac{U}{I} \tag{2.3}$$

With this definition, it can be seen that the impedance of a resistor is the same as its resistance, as shown in Equation 2.4.

$$Z = \frac{U}{I} = R \tag{2.4}$$

Equation 2.4 highlights that the resistor's impedance is constant and does not depend on voltage or current. There is also no dependence on the time. Equation 2.4 demonstrates that a resistor is a pure real value in the complex AC calculation.

Capacitors

A capacitor's impedance depends on the charge stored in the capacitor and the applied voltage. The current through a capacitor is defined as shown in Equation 2.5.

$$I = \frac{dQ}{dt} \tag{2.5}$$

With $Q = U \cdot C$ Equation 2.5 turns into Equation 2.6.

$$I = \frac{du}{dt}C \tag{2.6}$$

This results in the following impedance definition for capacitors.

$$Z = \frac{U}{I} = \frac{U}{\frac{du}{dt}C} \tag{2.7}$$

When using complex AC calculation, the impedance of a capacitor is written as in Equation 2.8.

$$Z = \frac{1}{j\omega C} \tag{2.8}$$

Equation 2.8points out that the impedance of an ideal capacitor is purely imaginary.

Inductors

In the same way, as for the capacitor, the impedance of an inductor is not a constant value. The impedance of an inductor depends on the energy it has stored and the current flowing through it. The voltage across an inductor is defined according to Equation 2.9.

$$U = \frac{di}{dt} \cdot L \tag{2.9}$$

So, the inductor impedance is given by Equation 2.10.

$$Z = \frac{U}{I} = \frac{\frac{di}{dt} \cdot L}{I} \tag{2.10}$$

In complex AC calculation, the impedance is then written as in Equation 2.11.

$$Z = j\omega L \tag{2.11}$$

So, equal to the capacitor, it can be seen that the impedance of an ideal inductor is purely imaginary in complex AC calculation.

Transmission Lines

For a transmission line, the definition of the impedance is more complex than for lumped elements. A transmission line is a distributed element. Only in the case of a short transmission line ($l << \lambda_{min}/10$) the behavior of the transmission line can be approximated by lumped components. If the transmission lines are longer than $\lambda_{min}/10$, the voltage and current can have varying values over the length of the conductor. [28] To determine the impedance of a transmission line, a "piece of line infinitesimal length Δz can be modeled as a lumped element circuit" . [28] Figure 2.2 shows such a model.

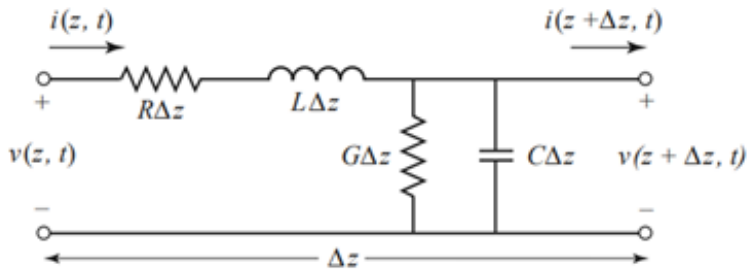


Figure 2.2: Equivalent circuit of a transmission line part with length Δz. With R = series resistance per length, L = series inductance per length, C = parallel capacitance per length, and G = parallel conductance per length. [28]

The following derivation of the characteristic impedance (Z_0) from this transmission line model is done in the same way as explained in chapter 2.2 of "Microwave and RF Design Volume 2" by Michael Steer [31]. Applying the Kirchhoff laws to this model leads to Equation 2.12.

$$v(z,t) - R\Delta z i(z,t) - L\Delta z \frac{\partial i(z,t)}{\partial t} - v(z+\Delta z,t) = 0 \tag{2.12}$$

Moreover, applying Kirchoff's current law on the circuit shown in Figure 2.2 gives Equation 2.13.

$$i(z,t) - G\Delta z v(z+\Delta z,t) - C\Delta z \frac{\partial v(z+\Delta z,t)}{\partial t} - i(z+\Delta z,t) = 0 \tag{2.13}$$

Dividing these two equations by Δz and taking the limit as $\Delta z \to 0$ lead to the following two differential Equations, 2.14 and 2.15.

$$\frac{\partial v(z,t)}{\partial z} = -Ri(z,t) - L\frac{\partial i(z,t)}{\partial t} \tag{2.14}$$

$$\frac{\partial i(z,t)}{\partial z} = -Gv(z,t) - C\frac{\partial v(z,t)}{\partial t} \tag{2.15}$$

Equations 2.14 and 2.15 are also known as the so-called telegrapher's equations. These equations can be simplified to Equations 2.16 and 2.17 for the sinusoidal steady-state condition.

$$\frac{dV(z)}{dz} = -(R + j\omega L)I(z) \tag{2.16}$$

$$\frac{dI(z)}{dz} = -(G + j\omega C)V(z) \tag{2.17}$$

From Equations 2.16 and 2.17, the following set of wave equations can be derived:

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0 \tag{2.18}$$

$$\frac{dI^2(z)}{dz^2} - \gamma^2 I(z) = 0 \tag{2.19}$$

with the propagation constant γ as:

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.20}$$

The propagation constant γ is the combination of the attenuation coefficient α and the phase-change coefficient β. So, the real part of the propagation constant $Re\{\gamma\}$ defines the attenuation on a transmission line in nepers per meter. Equations 2.21 and 2.22 are known solutions for Equations 2.16 and 2.17.

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z} \tag{2.21}$$

$$I(z) = I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z} \tag{2.22}$$

Now, replacing $V(z)$ in Equation 2.16 by 2.21 results in Equation 2.23.

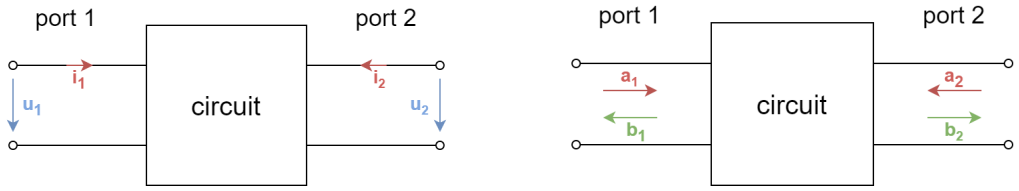
$$I(z) = \frac{\gamma}{(R + j\omega L)}(V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z}) \tag{2.23}$$

Equations 2.23 and 2.22 result in:

$$I_0^+ = \frac{\gamma}{R + j\omega L} V_0^+ \tag{2.24}$$

and

$$I_0^- = \frac{\gamma}{R + j\omega L}(-V_0^-) \tag{2.25}$$



(a) 2-port circuit with voltages and currents for impedance representation

(b) 2-port circuit with input and output waves for S-parameter representation

Figure 2.3: 2-port circuits for different representations.

The characteristic impedance of this part of the transmission line can be defined as shown in Equation 2.26.

$$Z_0 = \frac{V_0^+}{I_0^+} = \frac{-V_0^-}{I_0^-} = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.26}$$

2.1.2 S-Parameters

The impedances discussed in Section 2.1.1 describe the behavior of electrical components. Combining these components into a corresponding network, a different technique is advantageous in summarizing their behavior. Scattering parameters (S-parameters) do not define a network with voltages and currents but with incoming and outgoing waves. Coefficients represent the relationship between the incoming and outgoing waves. For each frequency, an own set of coefficients is provided. Thus, the S-parameters are referred to as a table-based model. An essential property of the S-parameters is that the number of required coefficients does not depend on the complexity of the network but on the number of incoming and outgoing ports. Therefore, the S-parameter can mask the complexity of the underlying physical network. As shown in Figure 2.3b, each network is represented by a block with two ports. Each port has two terminals providing an incoming and an outgoing signal.

The incoming and outgoing signals a_i and b_i identify the normalized traveling waves. They combine the contribution of the voltage and the current at the corresponding port normalized by the square root of the impedance of the signal source (Z_{Li}), also called reference impedance of the port. Equations 2.27 and 2.28 show the relationship between the voltage and current applied to a port and the incoming and outgoing waves at the same port. The complete derivation of how to get to these equations is described in chapter 2 of "Hochfrequenztechnik" by Holger Heuermann. [18]

$$a_i = \frac{u_i + Z_{Li} \cdot i_i}{2\sqrt{Re\{Z_{Li}\}}} \tag{2.27}$$

$$b_i = \frac{u_i - Z_{Li} \cdot i_i}{2\sqrt{Re\{Z_{Li}\}}} \tag{2.28}$$

S-parameters define the scattering of the incoming waves. So, there is a parameter for each port-to-port configuration, defining how much of the incoming signal is transferred to each port. For instance, a two-port system, as shown in Figure 2.3b has two parameters defining the scattering of the signal incoming at port 1 (a1) and two parameters defining the scattering of the incoming wave at port 2 (a2).

- $S_{11} = \frac{b_1}{a_1}|_{a_2=0}$ Reflection factor: defines the portion of a1 reflected at port 1
- $S_{21} = \frac{b_2}{a_1}|_{a_2=0}$ Transmission factor: defines the portion of a1 transferred to port 2
- $S_{11} = \frac{b_2}{a_2}|_{a_1=0}$ Reflection factor: defines the portion of a2 reflected at port 2
- $S_{12} = \frac{b_1}{a_2}|_{a_1=0}$ Transmission factor: defines the portion of a2 transferred to port 1

Writing this relation between the incoming and outgoing waves in the form of two equations leads to Equations 2.29 and 2.30.

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{2.29}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{2.30}$$

The equation system built by Equations 2.29 and 2.30 can also be written in matrix style as shown in Equation 2.31.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.31}$$

If this is put into a general form for a network with N ports, it results in Equation 2.32. From Equation 2.32, it can be deduced that an N-port network has NxN S-parameters, and an N-port network can be described using an NxN S-parameter matrix.

$$\begin{bmatrix} b_1 \\ b_2 \\ \cdot \\ b_N \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \cdot & S_{1N} \\ S_{21} & S_{22} & \cdot & S_{2N} \\ \cdot & \cdot & \cdot & \cdot \\ S_{N1} & S_{N2} & \cdot & S_{NN} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ \cdot \\ a_N \end{bmatrix} \tag{2.32}$$

From the definition $S_{ii} = \frac{b_i}{a_i}$ and the Equations 2.27 and 2.28 S_{ii} can be defined as Equation 2.33. Z_{Ii} is the input impedance of the according port and is defined as $Z_{Ii} = \frac{u_i}{i_i}$. Z_{Li} identifies the reference impedance at the according port.

$$S_{ii} = \frac{Z_{Ii} - Z_{Li}}{Z_{Ii} + Z_{Li}} \tag{2.33}$$

Equation 2.33 emphasizes that S_{ii} is an interpretation of the input impedance at the considered port. Thus, the input impedance of a port can be derived from S_{ii} as indicated in Equation 2.34. The only required information are the S-parameters S_{ii} and the impedances Z_{Li} to which the signals are referred to.

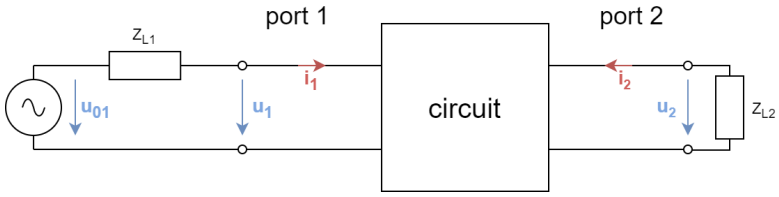


Figure 2.4: 2-port circuit with a voltage source, a source impedance Z_{L1} and a load impedance Z_{L2}

$$Z_{Ii} = Z_{Li}\frac{1 + S_{ii}}{1 - S_{ii}} \tag{2.34}$$

The transmission coefficient $S_j i$ defines the transmission factor from port i to port j. Equation 2.35 shows how the S-parameter $S_j i$ relates to the voltage transmission. Figure 2.4 summarizes the circuity for a 2-port network with the attached signal source.

$$S_{ji} = \frac{2u_j}{u_{0i}}\sqrt{\frac{Z_{Li}}{Z_{Lj}}} \tag{2.35}$$

2.2 Main Signal Integrity Effects

2.2.1 Attenuation

Attenuation is the damping of a signal amplitude when traveling through an electrical system. The attenuation on a printed circuit board (PCB) is mainly neglectable for low-frequent signals with a few MHz and below. The only attenuating factor for such signals is the voltage drop on the copper line caused by the resistance of the conductor. The polarization losses in the dielectric material used to compose the PCB are almost neglectable at low frequencies. This means that attenuation for low-frequency signals can be minimized by designing a transmission line for low electrical resistance.

For high-frequency applications in the hundreds of MHz range or even higher, multiple effects cause a higher attenuation [14]. For once, the so-called skin effect [31] leads to a higher resistance of the copper line. As indicated, the dielectric losses contribute significantly to the attenuation, especially at higher frequencies. Dielectric attenuation describes the attenuation of the electric field in the PCB material surrounding the copper trace. Both the attenuation in the dielectric material and the conducted attenuation within the line can lower the amplitude at the output of the line. The attenuation can be significant for high-frequent signals and increase the rise and fall time, as Figure 2.5 shows.

2.2.2 Reflections

Suppose a signal passes an impedance change (i.e. from the characteristic impedance of a transmission line (see section 2.1.1) to connected load impedance). In that case, this creates a signal in the opposite direction of the initial signal. This signal traveling in the

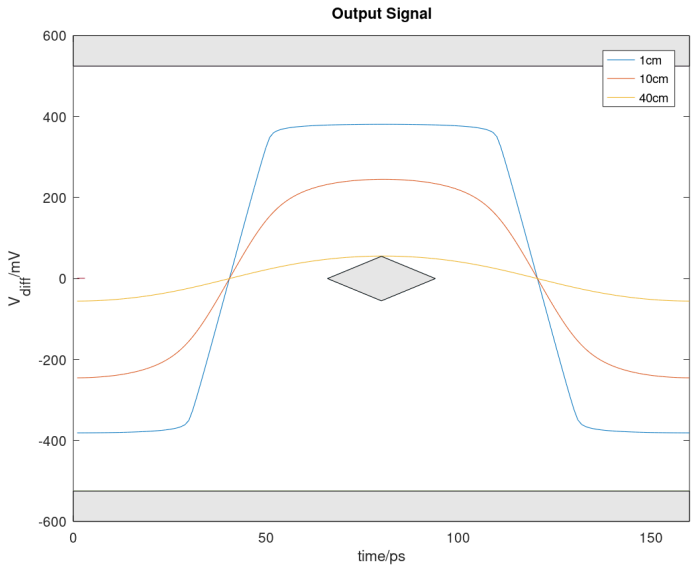


Figure 2.5: Signals showing attenuation effect at the end of 1 cm, 10 cm and 40 cm transmission line.

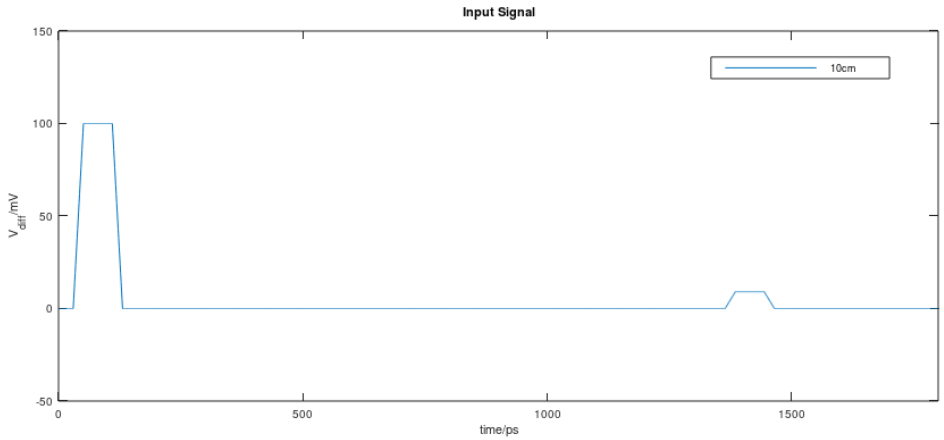
opposite direction is called reflection. How big the reflected signal is depends on the ratio of the differing impedances. The reflection factor can be calculated by Equation 2.36 [14], where Z_{Li} is the source impedance and Z_{Lj} is the load impedance.

$$\Gamma = \frac{Z_{Li} - Z_{Lj}}{Z_{Li} + Z_{Lj}} \tag{2.36}$$

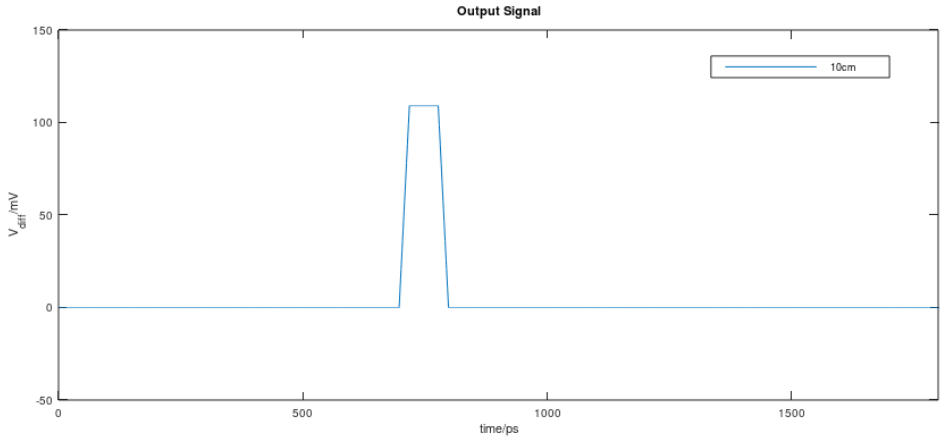
For example, if there is a mismatch between the transmission line's impedance (Z_{Li}) and the impedance of the connected load (Z_{Lj}), there is a reflection coefficient Γ. The signal in the opposite direction of the initial signal, will have an amplitude of Γ times the initial signal. Figure 2.6 shows the simulation of such a reflection. Figure 2.6a represents the input signal of the simulated transmission line. The first high pulse is the initially inserted signal. The second lower pulse after about 1.4 ns is the part that is reflected at the end of the transmission line. The time it takes a signal to travel along a transmission line is called propagation delay. The time distance between the first pulse's rising edge and the reflected pulse's rising edge is precisely two times the propagation delay. Figure 2.6b shows the signal received at the simulated transmission line's output.

2.2.3 Cross Talk

Signals with short rise and fall times can affect the signals on adjacent transmission lines. This effect is called cross-talk. There are two types of cross-talk. One is far-end cross-talk (FEXT), which describes the cross-talk influence on the transmission line end that is further away from the aggressor signal source. The second type of cross-talk is the near-end cross-talk (NEXT). It describes the influence on the end of a neighboring line closer to the aggressor signal source.



(a) Electrical signal present at the transmission line's input. The initial pulse sent by the source and the reflected signal after two times the propagation delay.



(b) Signal as it is present at the transmission lines output.

Figure 2.6: Reflection on a 10 cm long microstrip transmission line.

For NEXT, only the coupling between the aggressor and the victim influences the amplitude of the disturber signal. So, the proximity between the two lines is the main parameter influencing NEXT.

For FEXT, the coupling region's length also affects the disturber's magnitude. This correlation is especially a problem for parallel data and clock lines. If a clock and data line or several data lines are routed close to each other over long distances, this could cause signal distortion due to far-end cross-talk.

Figure 2.7 shows a simulation example for cross-talk on two parallel transmission lines. As it can be seen, FEXT is much more significant than NEXT. This significant difference is due to the simulated line length of 20 cm.

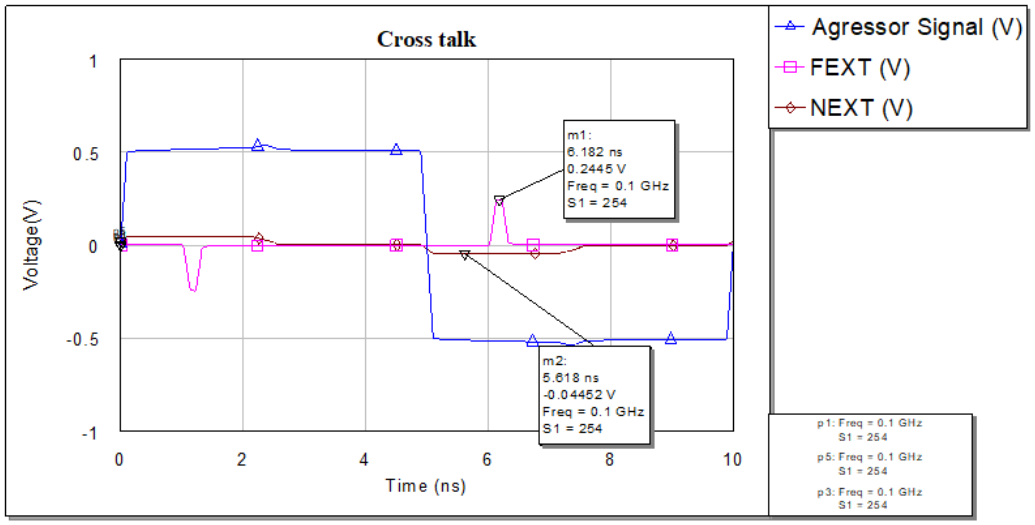


Figure 2.7: Simulation result showing far-end and near-end cross-talk for 20 cm coupled transmission lines. The aggressor signal is a square wave with 100 ps rise/fall time.

Chapter 3

High-Speed Interfaces

High-Speed interfaces, or so-called multi-gigabit interfaces (MGT), can transmit and receive multiple gigabits of information within one second. Nowadays, there are already manifold standards for multi-gigabit interfaces. Well-known standards are, for instance, the Peripheral Component Interconnect Express, better known as PCIe or JESD204a/b/c standards. [1] [24] [23]
PCI Express is the most common high-speed interface for PC components. It is used to connect peripherals like graphics cards, SSDs, or network cards to the CPU of a PC. The most recent revision of the PCIe standard is PCIe 6.0 [1]. This standard allows transmission speeds up to 64 GT/s, which means $64 \cdot 10^9$ transfers per second. For interfacing high-speed data converters, the JESD204 interface is more commonly used. It allows transmission rates up to 32 GT/s. [23]

Most such standards are separated into logical layers. There are specifications for the physical layer, the data link layer, and the transaction layer.

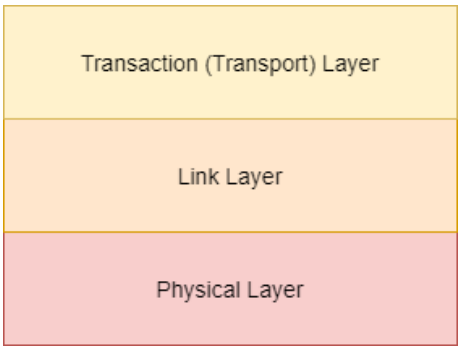


Figure 3.1: Typical layering of interface specifications.

The physical layer defines the constraints for the physical setup. Parameters like the impedance of a transmission line, the highest allowed losses on a signal line, or the maximum connection length are defined in the physical layer. Also, the waveform is defined in this layer, such as the signal's voltage levels or rise and fall times (see Chapter 3.1.1). The

data link layer is set on top of the physical layer. This layer states the requirements for a stable connection between two (or more) actors. It can define the sequencing of frames, the encoding and decoding of packets, and further properties supporting a stable connection. The transaction or transport layer converts the data into the correct format. Data frames are generated. Additional start or end bytes and parity or CRC bytes can be added to ensure the data's integrity.

3.1 JESD204

JESD204 was developed as an interface for high-speed data converters. It was designed as a serial interface. The transported data is serialized in the transmitter and then deserialized in the receiver again. This serialization is done to benefit from higher data rates, which come with serial data transmission. For this reason, this type of interface is called SERDES (SERialize-DESerialize) interface.
The first draft of the interface allowed a single serial interface lane. Since revision A, the standard allows the use of multiple parallel lanes. However, the data is still transported serialized over the single lines, not in parallel. Meanwhile, the standard has reached revision C [23], which also allows higher data rates (up to 32 GT/s) and provides features like deterministic latency (see 3.1.4).

3.1.1 Physical Layer

The detailed electrical specification of JESD204B is defined in chapter 4 of the standard specification provided by JEDEC [24].
The topology of the interface is a "unidirectional, point-to-point" connection, using "controlled impedance traces on printed circuit boards" [24]. The characteristic impedance of these traces shall be 100 Ω differential. A minimum allowed insertion loss is defined for the transmission lines connecting the devices. Figure 3.5 shows the minimum allowed channel insertion loss. The allowed data rate goes from 312.5 Mbps up to 12.5 Gbps (JESD204B [24]) or even 32 Gbps (JESD204C [23]).

Eye Mask

For the definition of the signal shape, a so-called eye mask is defined. If an eye mask is placed on a digital pulse's timing diagram, the mask defines the magnitude and timing constraints for the signal. Figure 3.2 shows an example. The signal is in an allowed range as long as the signal lines are not crossing the grey area in the middle (eye mask).

In the JESD204b standard, such eye diagrams are defined for each interface side, the transmitter, and the receiver. The eye diagrams' time values depend on the used data rate. So, for a lower bit rate, the duration of a high or low pulse is longer than for a higher rate. For this reason, the timing values of the eye masks are given in the unit UI (Unit Interval). One UI is the duration of one bit, so for a 12.5 Gbps signal, 1 UI would be 80 ps.

$$1\,\mathrm{UI} = \frac{1}{f_{data}} = \frac{1}{12.5\,\mathrm{GHz}} = 80\,\mathrm{ps} \tag{3.1}$$

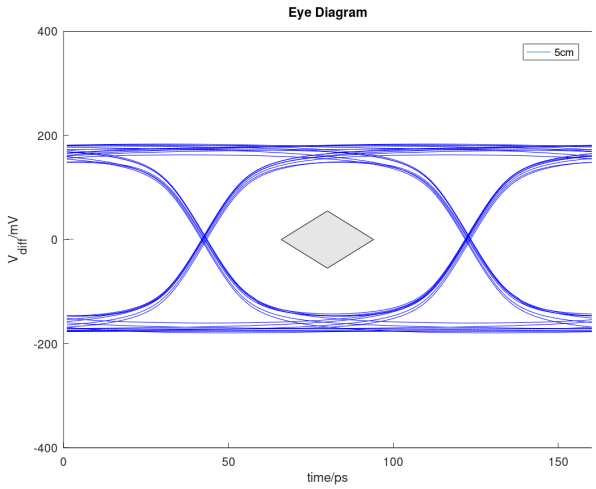


Figure 3.2: Eye Diagram simulated for a 12.5 GBit/s signal on a 5 cm line. In the middle of the diagram, the JESD204B eye mask for 12.5 GBit/s data rate is placed. [24]

Figure 3.3 shows the transmitter eye mask of the JESD204b standard. This eye mask shows the magnitude and timing constraints for a 6 to 12.5 Gbps signal. This range defines the highest data rates allowed according to the JESD204b standard. The values of the variables used in the diagram are defined in Table 3.1. The values and the diagram are taken from the JESD204b standard [24].

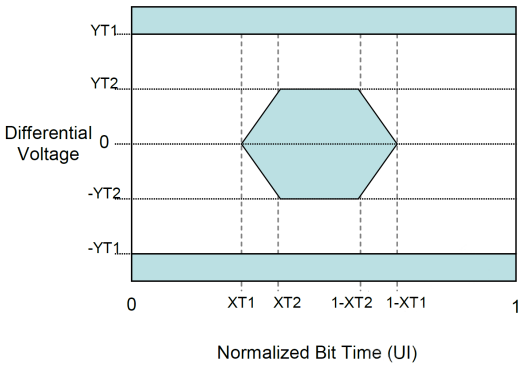


Figure 3.3: General JESD204B transmitter eye mask out of the JESD204B standard. [24]

$XT1$	$XT2$	$YT1$	$YT2$
UI	UI	V	V
0.15	0.4	0.385	0.18

Table 3.1: Transmitter eye mask values for the JESD204B LV-OIF-11G-SR electrical specification.

So, this means that (a single pulse of) the output signal of a JESD204b compliant trans-

mitter has to fit into the white area of Figure 3.3.

Figure 3.4 shows the signal constraints for a JESD204b compliant receiver. The according limits are listed in Table 3.2. So if (a single pulse of) the signal is entirely in the white area and not interfering with the mask, a receiver must decode the signal correctly. For hardware designers, the goal is to design an interconnect between transmitter and receiver such that the signal still fits the receiver eye mask at the end of the line. Again, the values and the diagram are taken from the JESD204b standard [24].

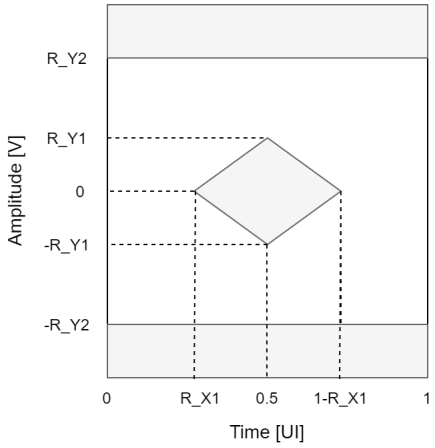


Figure 3.4: JESD204B Receiver Eye Mask [24]

R_X1	R_Y1	R_Y2
UI	V	V
0.35	0.055	0.525

Table 3.2: Receiver eye mask values for the JESD204B LV-OIF-11G-SR electrical specification.

Another requirement defined by the JESD204b physical layer is the insertion loss. The insertion loss defines the amount of attenuation allowed on the transmission line. Figure 3.5 shows the allowed insertion loss defined by the standard.

What this constraint means for a transmission line design is described in Chapter 5.

SERDES

One part of the physical interface is the data's serialization and deserialization (SERDES). While the data words are handled parallel within the devices (data converter, FPGA, ASIC, etc.), the data is transmitted in serial. Therefore, so-called SERDES blocks are implemented in most high-speed data converters. Every JESD204-compliant transmitter must have a serializer, and every JESD204-compliant receiver must have a deserializer. This extra step is performed because higher data rates can be achieved with serial transmission. For data rates in the Gbps range, aligning data bits along multiple parallel data

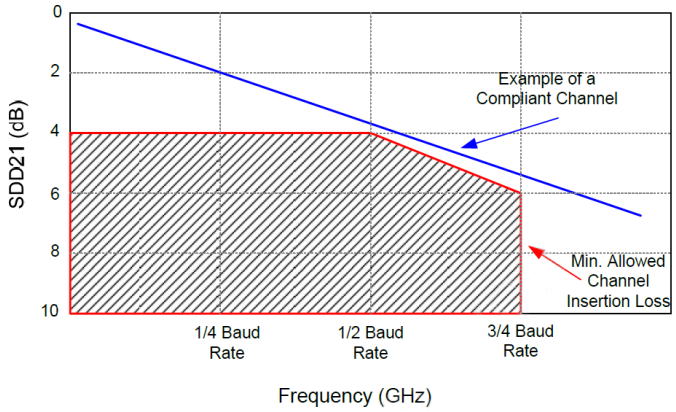


Figure 3.5: Insertion loss constraint defined by the JESD204b standard. [24]

lines is very hard. In serial data transmissions, only the clock has to be aligned with the data input. Also, the physical design of the interface between two devices gets simpler since the number of necessary connections gets much lower.
Although the JESD204 standard defines a serial interface, it allows multiple data lanes. However, even with multiple data lanes, the data is still transported as serial data. Therefore, data frames can be guided via different lanes, but each frame is still transmitted in serial via a single lane. In the transmitter, the frames can be placed in the correct order again by reading the headers of the frames. This process allows for even higher data rates through the use of multi-channel serial transmission. Using multiple data lines instead of one is also a significant benefit when aiming for lower-cost designs. Increasing the number of lanes can be used to reduce the data rate per lane without compromising the overall data rate. The mentioned design approach achieves a transfer rate reduction at the cost of design complexity and production cost.

3.1.2 Data Link Layer

The data link layer covers two main aspects. On the one hand, the data encoding and decoding are performed. On the other hand, the synchronization between the receiver and transmitter is accomplished. For synchronization, the so-called code group synchronization (CGS) is used [36]. In this step, the transmitter sends well-known packets to the receiver. The receiver must then find these packets in its input stream to synchronize with the transmitter. The so-called initial lane alignment sequence (ILAS) is used to measure the mismatch between the single data lanes and align the timing of the input signals with a dynamic buffer. [36]

An 8b/10b encoding is also defined in the JESD204b standard for better signal integrity. This encoding converts 8-byte data frames into 10-byte long packets. The encoding algorithm ensures roughly the same amount of logical highs and logical lows per packet. This equality logic level avoids long, high, or low durations on the physical signal. Such long high or low times would make ac-coupling of the data lines problematic. This way, ac-coupling is no problem. The encoding also provides particular error detection.

3.1.3 Transport Layer

In the transport layer, the data to be sent is packed into frames. A frame consists of one or more octets. If the amount of sample bits is not a multiple of 8, so-called tail bits are used to fill up the remaining bits to complete the last octet.

In addition to the data, control bits can be packed into the frames. Control bits can be used, for instance, to indicate status information. [36]

3.1.4 Special Features

Length Tuning

A feature of the JESD204 standard that is very helpful for the hardware design is a dynamic lane buffer in the receiver. This feature buffers data input from each data lane and aligns the timing of the lines. For that reason, the data lanes of the interface need not be length-matched, which makes the PCB design a lot simpler.

Deterministic Latency

Another feature provided by this standard is the so-called deterministic latency. Deterministic latency specifies the time difference between when data is ready to be sent and when the receiver has received the data and is ready to be processed. This time difference must be constant and well-known to be attributed to the deterministic latency. With this property, it is possible to get the input timing of multiple ADCs or the output timing of multiple DACs aligned.

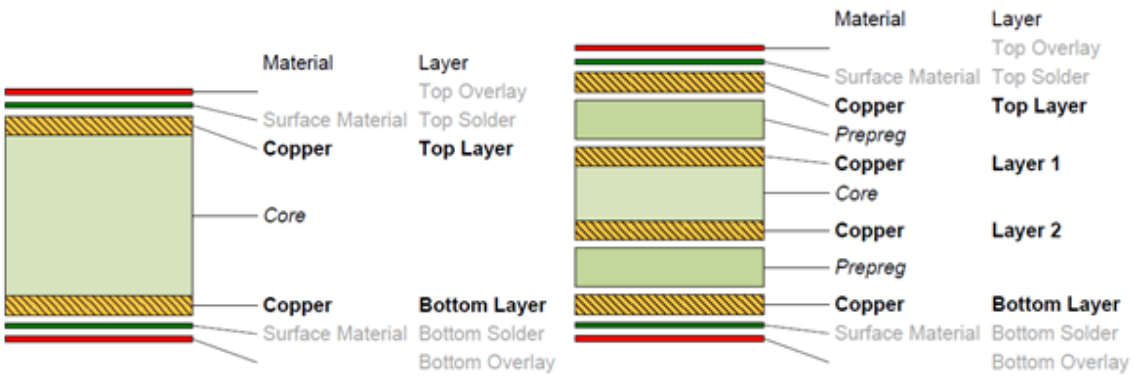
Chapter 4

Printed Circuit Boards (PCBs)

A printed circuit board (PCB) is a board for carrying and connecting electrical components such as integrated circuits (ICs) and passive components (resistors, capacitors). The construction of such a PCB is a layered stack-up of copper planes and insulating sheets. Copper tracks are constructed by etching the copper sheets. These copper tracks are used as connections between the electrical components.

4.1 Construction

A PCB is constructed by layering up copper sheets and insulating laminates. In Figure 4.1a, a so-called 2-Layer PCB stack-up is shown, and in Figure 4.1b, a 4-Layer PCB stack-up is shown. Such a PCB can have copper layers starting from 2 up to 100+. [27]
The laminates in between the copper sheets can be separated into two types.
Type one is a prepreg layer [17]. Prepregs are not fully hardened fiberglass laminates. Such a layer has a certain amount of resin to make the material flexible. These materials are necessary for PCBs with more than two layers. If the copper layer is etched, a prepreg layer fits into the structure of the etched copper.



(a) 2 Layers (b) 4 Layers

Figure 4.1: Standard 2-Layer and 4-Layer stack of a printed circuit board.

The second type is a laminate consisting of pressed and hardened prepreg layers [17], also called core [26].
A simple two-layer PCB, for example, is just a core layer with copper on each side. This technique allows stacking the PCB layers without having air pockets. Typically, core layers and prepreg layers are stacked up alternately. A typical stack is shown in Figure 4.1b. If all PCB layers are stacked, the board is heated to harden the prepreg. This process can be done as a single step to harden all layers or in several cycles.
For the final thickness after all stacking steps, manufacturers give a ±10% tolerance [7] [8].

4.2 Materials

The standard conducting material in PCBs is copper. Almost all PCB manufacturers use copper sheets as conducting layers. However, there is a wide variety of materials for the insulating layers. The most standard PCB laminate is called FR-4 [17]. It is a fiberglass material class often used for PCBs because it is hardly flammable and cheap. The material properties of FR-4 have a specific range of variation. For instance, the dielectric constant starts from 3.9 and goes up to 4.7 [10], which is a wide range (see Figure 5.4). Another material constant is the dissipation factor. The dissipation factor defines how strongly a signal's attenuation varies with the signal's frequency. For FR-4 materials, it is at about 0.02 [10]. The impact of these constants on the signal integrity is explained in section 5.4 and the following. For most PCB applications, FR-4 is a sufficient material.
For high-frequency applications, FR-4 has a very high dielectric attenuation (section 2.2.1). At frequencies in the GHz range and above, the high dissipation factor and the variety of the dielectric constant are most certainly an issue. Therefore, there are special dielectrics for high-frequency applications. Manufacturers like the Rogers Corporation or Panasonic produce high-quality HF laminates. For instance, RO4000 series materials [2](Rogers) or the Megtron 6 [3](Panasonic) have well-defined dielectric constants of about 3.5, and these materials' dissipation factor is much lower. It ranges from about 0.002 to 0.004, which is factor 5 to 10 better than what can be expected from standard FR-4. These low dissipation factors and well-defined dielectric constants allow the design of PCBs that can handle wideband signals to the GHz frequency range.
There are even more materials like ceramics or aluminum, which can be used for high-temperature applications or flex materials for bent PCBs, but these are relatively rarely used.

4.3 Etching

The copper layers need to be shaped to create contours and structures like traces, transmission lines, or planes on the copper layers. This shaping is done by etching the material [17]. Similar to IC manufacturing, a photoresist layer is placed on the copper sheet. This photoresist is then illuminated through a mask. The mask defines where the copper is edged and where the copper stays in place. After removing the non-illuminated photoresist, an alkaline solution is used to remove the copper at the positions where there is no protecting photoresist anymore.
With this technique, copper planes with tracks and traces are created. By etching traces

with a width down to 50 μm can be created. According to IPC A-600, the track width can have a tolerance of up to 20%, but most manufacturers have higher standards than stated in the IPC document. The reason that there are such high tolerances is that etching is a somewhat imprecise technique. When etching copper traces, there will not be straight etches. Figure 4.2 shows that every trace will look like a trapezoid.

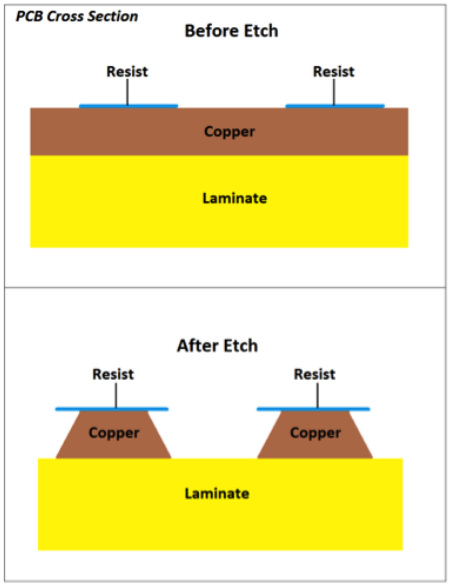


Figure 4.2: Schematic display of PCB etching process. [6]

4.4 Vias

Vias are interlayer connections on a PCB. The standard through hole via is a hole in the PCB that is galvanized. With this technique, an electrical connection through a PCB can be established. Traces or copper planes on any layer can connect such a via. A spacing between the via and the copper is kept on layers where no connection to the via is wanted.

For more advanced designs, there are blind and buried vias [25]. Blind vias only reach from either the top or bottom layer to some inner layer. Buried vias do not reach any outside layer (Top, Bottom), so they are buried in the PCB stack. These kinds of vias are much more expensive than the standard through-hole vias. One benefit of blind and buried vias is that they can connect traces on inner layers without generating a stub. Another advantage is that these kinds of vias save space in the layout since they are only present on a few layers. Figure 4.3 shows these three via types.
A cheaper option for removing stubs from vias is the back drilling technique [9]. Back-drilled vias are standard vias where the finished via is drilled from one side of the PCB with a broader drill diameter than the via diameter. With this additional step, the connection of the layers drilled with the broad drill can be removed.

For vias, there are certain manufacturing limitations, too. An aspect ratio (drill diameter to drill depth) of at least 1:10 must be fulfilled for through-hole and buried vias. Blind

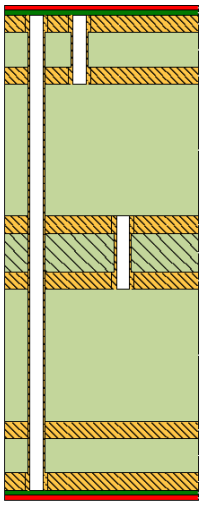


Figure 4.3: Via types: Through Hole(left)/Blind Via(center)/Burried Via(right)

vias are only possible for an aspect ratio of 1:1.

4.5 Solder Stop

An additional insulation layer is attached after all copper sheets are etched and all layers are stacked. The so-called solder stop layer is a thin film on the outsides of the PCB. It covers the complete surface of a PCB except for the soldering pads. The components are mounted on the soldering pads. This layer protects the copper traces from pollution or harm. The reason that it is called solder stop is that it also builds a mask for soldering. The solder stop prevents the solder paste from floating to other pads and creating shortcuts.

4.6 Surface Finish

Applying the surface finish is one of the last steps of producing a PCB. The free copper pads are processed with other materials. A thin layer of tin or gold can be applied to protect the copper from oxidation and provide an excellent soldering surface [17]. The cheapest and one of the most common surface finishes of PCBs is the so-called HASL finish. All uncovered copper surfaces get covered with a thin tin layer at this type of surface. For more complex PCBs with higher demands, there are also gold finishes like ENIG. These are more durable and create better electrical contact between the copper pad and the component.

Chapter 5

Transmission Line Design

5.1 Design Requirements

A design for a PCB interface between a high-speed data converter and a controller should be implemented. The interface should fulfill all requirements for a JESD204B interface [24]. According to the standard, the data rate goes up to 12.5 Gbps, and the rise/fall times are $\geq$ 24 ps. As an interconnect, a differential transmission line must be matched to a load impedance of 100 Ω. The differential interface voltage has a magnitude of at least 360 mV differential. Also, the maximum allowed insertion loss for the interface's transmission line is defined. Figure 5.1 shows the insertion loss limit.

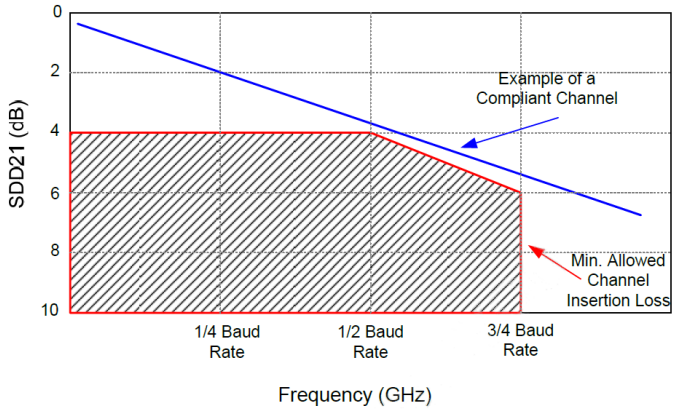
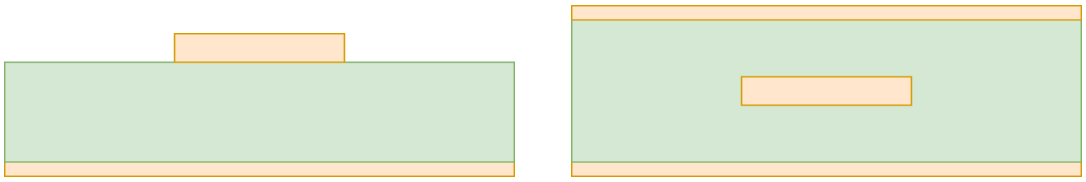


Figure 5.1: Insertion loss constraint from the JESD204B specification. [24]

For the received signal, a receiver eye with a height of 110 mV differential and a width of 27.027 ps is specified. Figure 3.4 shows the corresponding eye mask.

A standard low-cost material such as FR-4 is the preferred choice for the base material of the PCB. This choice is preferred as it keeps production costs low, and the production and delivery times are shorter than with other base materials. The design should also estimate how large the distance between the two components can get before the signal integrity



(a) Microstrip cross-section. A single copper line is located on top of a dielectric layer, and a reference plane is at the bottom side.

(b) Stripline cross-section. A copper line in the middle of a dielectric layer with a reference plane on top and bottom.

Figure 5.2: Cross-sections of PCB transmission lines.

becomes a problem. Also, the effects of possible discontinuities, such as vias or connectors, should be estimated.

5.2 Transmission Line Structures on PCBs

A transmission line is a conductor transporting an electric signal and the corresponding return path [13]. PCB transmission lines are typically created by copper traces and the surrounding area, usually a dielectric material or air. The two most straightforward sorts of PCB transmission lines are microstrips and striplines. A microstrip line is a copper trace on top of a PCB. A dielectric layer separates the trace from a ground layer. Figure 5.2a shows a cross-section of a microstrip line. The second transmission line type is the so-called stripline. Unlike microstrip lines, a Stripline is not on the outside of a PCB. It consists of a copper trace embedded in the dielectric layer. Above and below the copper trace, a ground plane is present. A cross-section schematic of a stripline is shown in Figure 5.2b.
The copper lines' dimensions (height, width, thickness) and the dielectric layers' material properties define the characteristics of the transmission lines.

Both variants can be designed as single-ended as well as differential transmission lines. In both cases, a second signal line is placed next to the initial one to get a differential line design. For differential lines, the distance between the two signal lines is an additional factor affecting the characteristics of the transmission line.

5.3 Single-Ended vs Differential

There are many differences between single-ended and differential transmission lines. Both variants have advantages and disadvantages. As the name already says, a signal is transmitted through a single copper line in single-ended transmission lines. A reference to the signal is needed to have a signal level on the transmission line. On a PCB, this reference is the ground plane. The ground plane represents a reference level for all signals and voltages on the board. This reference plane is also the return path for the signal since the electric current needs a closed loop.
For an ideal differential pair, no reference plane would be needed. The signal would be carried purely by the differential lines. A differential transmission line builds a closed loop

already, and no additional ground is needed. For a differential transmission line on a PCB, a ground plane should still be neighboring the differential line. On a PCB, the ground plane also works as a reference for differential pairs due to the PCB structure. Also, a path for common mode currents is necessary.
So, one benefit of a differential transmission line is that the ground plane has less influence on the transmission line design. Also, the influence of surrounding line structures and EMC is minor for differential pair designs. Disturbances would affect both pair lines at a similar level, resulting in a common mode influence, but the differential signal is almost unaffected.
The drawback of differential transmission lines is that the differentially routed lines need much more space than a single-ended transmission line. So, the lower area consumption makes single-ended lines easier to route.

5.3.1 Tight Coupling and Loose Coupling

A differential pair can be designed with the two differential lines very close to each other or with some more distance between them. If the distance between the two differential lines, compared to the width of the line, is low, then the pair is tightly coupled. This coupling affects the characteristic properties of the lines. If, on the other hand, the lines are placed further apart, they are loosely coupled. For loosely coupled differential pairs, the coupling has only a minor effect on the transmission line's characteristics.
The benefit of loose coupling is that the impedance control gets easier. Loosely coupled differential pairs can be handled like two single-ended transmission lines. The coupling effects must be considered when designing the transmission line as a tightly coupled differential pair.
The benefit of tightly coupled lines is that the influence of distortions will be less. Most distortions will affect both lines almost the same way because they are close together. This proximity of the lines would mostly cancel out the differential signal error.

5.4 Design of a Controlled Impedance Trace

When designing a transmission line, several design decisions have to be made. First of all, a transmission line type must be chosen. The two main types of PCB transmission lines are defined in section 5.2.

There are several pros and cons for both line types. Striplines, for example, have better shielding since they are embedded between two ground planes. For striplines, far-end crosstalk is also less problematic. The disadvantage of striplines is the requirement of designing an impedance-controlled transition from an outer layer to the conductor located in an inner layer of the PCB. This connection has to be made in the form of a via (see section 4.4). Generally, the characteristic impedance of vias is challenging to define it properly. Furthermore, another disadvantage is the additional cost for blind vias or back drilling.
For this design, the choice was made to use Microstrip lines. It is easier to measure signals carried by microstrip lines than striplines since they are on the surface of a PCB. Another reason is that filter elements like a DC block capacitor can be placed on a microstrip line without changing the PCB layer. This is beneficial or even necessary for many high-speed

interfaces.

5.4.1 Single-Ended Microstrip Line

The designed transmission line must have a well-defined characteristic impedance to avoid reflections.
Equation 5.1 shows the calculation of a microstrip lines impedance according to IPC 2141 [21]

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \cdot ln\left[\frac{5.98h}{0.8w + t}\right] \tag{5.1}$$

Where w is the width of the conductor, t is the thickness of the conductor, h is the height of the insulating layer, and ε_r is the dielectric constant of the insulating material. Its characteristic impedance Z_0 should match the source and load impedance to minimize reflections on a transmission line. Typical standard impedances would be, for example, $50\,\Omega$ or $75\,\Omega$ single-ended and $85\,\Omega$ or $100\,\Omega$ differential. $100\,\Omega$ differential is also the impedance requested by the JESD204 standard [24]. Four parameters specify the characteristic impedance of a single-ended microstrip line: w, h, t, and ε_r. The first three parameters concern the geometrics of the microstrip line. The parameter ε_r provides the dielectric constant of the substrate. ε_r of important PCB substrate materials range between 2 - 10 [28]. As section 4.2 mentions, the most standard PCB material is the so-called FR-4. It has a dielectric constant of about 3.5 - 4.7 [10].

A second parameter that can be selected very well is the thickness of the copper trace. Several heights of the copper cladding ranging from $12\,\mu m$ to $105\,\mu m$ [4] are provided by different manufacturers. For the inner layers of a PCB, the end thickness of the layer when the PCB is finished is almost the same as the defined base thickness. There is no additional processing of the inner layers besides the etching process. To the outer layers of a PCB, about $20\,\mu m$ of extra copper is added in the plating process [22]. In case a high thickness is not needed, a low thickness is recommended. A lower thickness of the copper layer allows for manufacturing finer structures. A higher thickness would be needed to sustain high currents or to provide a low DC resistance. The thinnest copper thickness that most standard PCB manufacturers provide is an $18\,\mu m$ copper base thickness, which is after processing at least $33.4\,\mu m$ according to [22]. Prime manufacturers provide even $12\,\mu m$ and $9\,\mu m$ base thickness. Handling these low-thickness copper layers results in increased manufacturing costs.
Most manufacturers provide just an approximative value for the copper thickness. For instance, an $18\,\mu m$ thickness of about $35\,\mu m$ is defined. There is no exact value of the tolerance of this thickness. However, Equation 5.1 can be used to estimate the influence of the thickness tolerance. Figure 5.3 shows the variance of the characteristic impedance in relation to the copper thickness. The thickness is varied from minus 10% ($t_{min} = 33.4\,\mu$m) to plus 10% ($t_{max} = 36.74\,\mu$m) of the targeted thickness ($t = 35\,\mu$m). For this range, the transmission line's characteristic impedance varies in a range of about $0.5\,\Omega$.

After selecting the substrate's dielectric constant (Dk) and the copper thickness, two parameters are left to choose for impedance-controlled microstrip lines. The line width can be manufactured very precisely. In this way, that parameter can be used to fine-tune

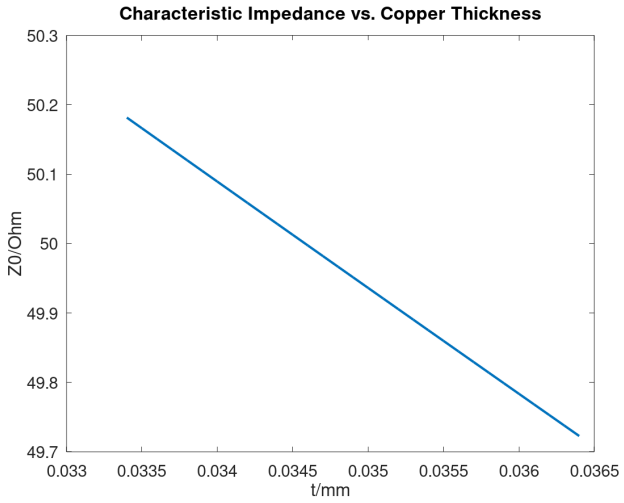


Figure 5.3: Calculation of Z_0 for varying copper thickness

the line impedance in a later step. As a good starting point, a line width of 10 mil (254 μm) is chosen. This linewidth matches the footprint of a 0201 passive component (0201 means that the component is 20 mil long and 10 mil wide). This matching width is beneficial when placing filter components on a transmission line. For example, a DC-blocking capacitor can be placed on a microstrip line without changing the line width.
The last parameter, the height, can be calculated by transforming Equation 5.1.

$$h = exp\left(Z_0 \frac{\sqrt{\varepsilon_r + 1.41}}{87}\right) \cdot \frac{0.8w + t}{5.98} \tag{5.2}$$

Using Equation 5.2, we get a height of $h \approx 152.6\,\mu$m. So, a microstrip transmission line with the following parameters:
$w = 0.254mm$
$h = 0.157mm$
$t = 0.035mm$
$\varepsilon_r = 4.3$
would have a characteristic impedance of approximately 50 Ω. The dielectric constant of FR4 substrates is often not specified precisely by manufacturers. The Dk value of FR4 changes depending on the duration it is stored before processing, which makes defining a precise value tough. Due to this reason, the characteristic impedance of the transmission line at the manufactured PCB will vary. As mentioned, the FR4 ε_r ranges from about 3.9 to 4.7 [10]. This range of Dk values would cause a variation of the characteristic impedance, as shown in Figure 5.4.

So, the vagueness of the dielectric constant and the copper thickness gives a tolerance of about ±2 Ω for the characteristic impedance. Of course, this tolerance can be minimized by using higher-quality PCB material. The ε_r is defined more precisely for more expensive dielectric materials. Another factor that affects the impedance of a microstrip transmission line is the solder mask. Most PCBs are covered with a solder mask for easier soldering and a protection layer. The effect of this layer needs to be considered, too. Equation 5.3 [16]

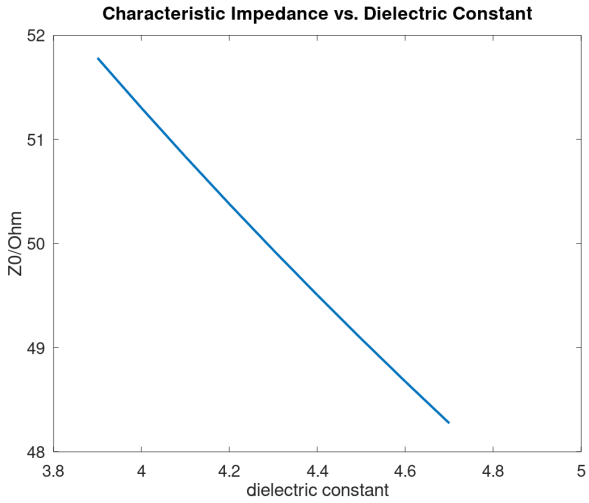


Figure 5.4: Calculation of Z_0 for the given range of ε_r

estimates how the solder mask affects the characteristic impedance.

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r \left(1 - e^{\left(\frac{-1.55h_1}{h}\right)}\right)}} \cdot ln\left[\frac{5.98h}{0.8w + t}\right] \tag{5.3}$$

In Equation 5.3, h_1 is the height h plus the additional height of the dielectric, which embeds the copper line. This equation is similar to Equation 5.1, but the first part indicates that the dielectric constant's influence on the impedances has changed. This factor is now adapted to represent the dielectric and air combination on top of the microstrip line. As stated in the paper of Doug Brooks [16], the formula gives similar results as Equation 5.1 for very low h_1 and predictions similar to the equation for a stripline when h_1 is getting big. For instance, if $h_1 = h + 45\,\mu$m the copper line is covered by an additional $10\,\mu$ of dielectric material. The calculated impedance would be about 15% lower than the exposed microstrip.
A simulation was performed to indicate how well these equations fit and how well the characteristic line impedance matches $50\,\Omega$. The transmission line is simulated in Cadence Microwave Office using the determined design values. In the schematic shown in Figure 5.5, a Microstrip Line (MLIN) was placed between 2 ports. The ports are defined to have an impedance of 50 Ohm. The microstrip line and the substrate (MSUB) are configured according to the specified values. Showing the S parameters S11 and S21 in a graph indicates how well the matching fits. The S parameters are shown in Figure 5.6.

The graph shows that the input reflection coefficient is -26.04 dB at worst.

The tuning tool provided by Cadence Microwave Office is used for a simplified approximation of the microstrip dimensions. This tool allows tuning schematic parameters and instantly seeing the influence on the simulation result. The tuning tool determined the lowest return loss for a thickness of about $144\,\mu m$. A simulation run with the updated value for the height parameter shows that the S11 Parameter has improved by over 16 dB

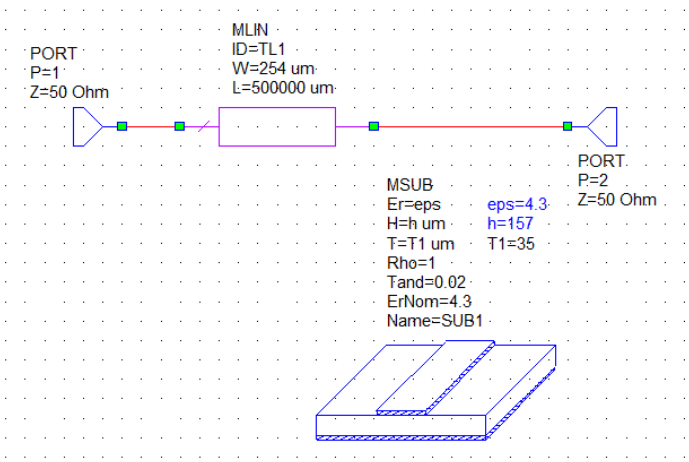


Figure 5.5: Schematics of a microstrip line in the Cadence Simulator.

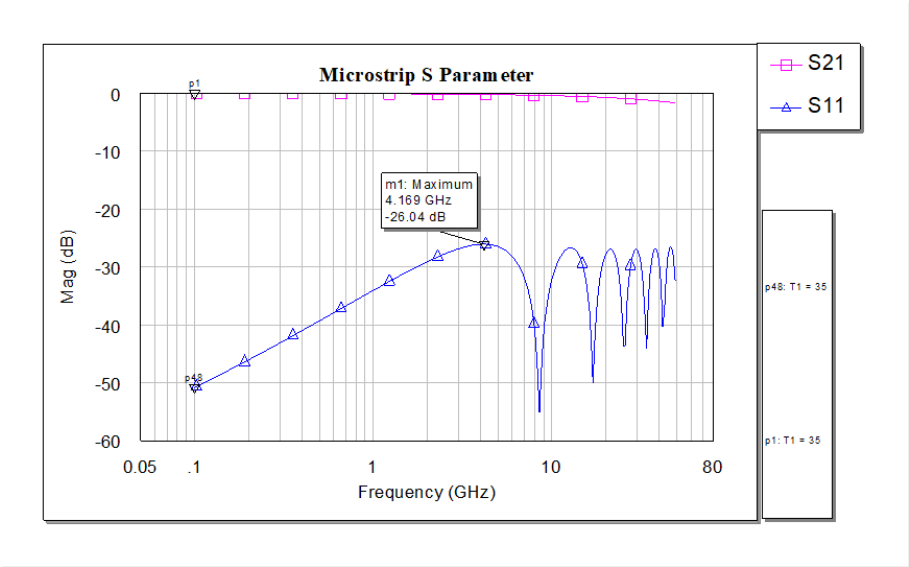


Figure 5.6: S11 and S21 of the microstrip line shown in Figure 5.5.

to -42.95 dB.

A simulation was performed to visualize the mismatch as an impedance value in Ohm. Therefore, a step signal is simulated at the input port of the system, and the time domain signal is measured. A reflection will be visible on the signal graph for any impedance discontinuity in the system. Therefore, the measured signal, the source signal, and the impedance the source sees at any time can be calculated. A long transmission line with 100 cm length was used for the simulation. The line length sets the duration where the source is loaded with the impedance of the transmission line. In Figure 5.7, this would be about 11 ns before the graph shows exactly the load impedance. The source is loaded with the characteristic line impedance in this 11 ns. Using the best-case dimensions determined by the Cadence tuner tool, the simulation software calculates an impedance of

49.93 Ω. For the worst-case scenario with the minimum $\varepsilon_r = 3.9$ and the maximum copper thickness of $t = 36.6\,\mu$m, the simulation shows a line impedance of 51.85 Ω. This value is about 2 Ω higher than the best case. The estimation is presented in Figures 5.3 and 5.4. A microstrip line coated with a solder mask is displayed as a third curve. An embedded microstrip line with an additional 10 μm of solder stop on top was used as a simulation model. The simulation of the embedded microstrip results in a line impedance of 47.44 Ω. This deviation is an insignificant but noticeable (15%) deviation from the value expected from Equation 5.3.

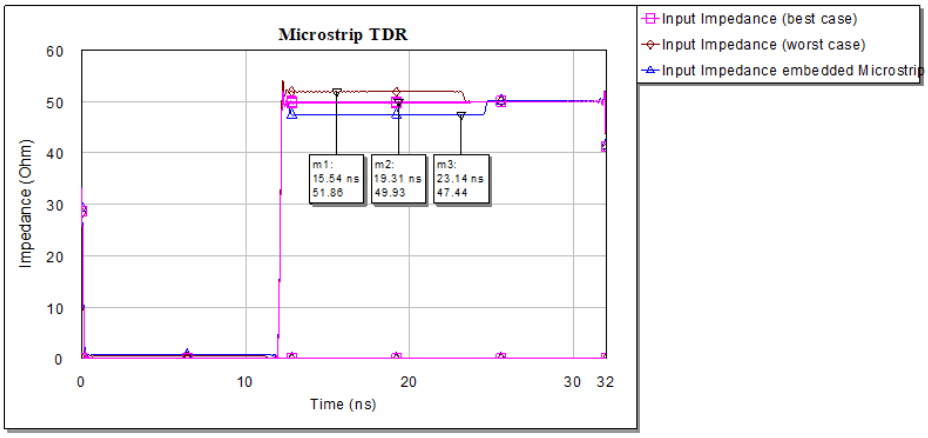


Figure 5.7: Step response simulated for a 50 Ω microstrip line in different configurations. Best case condition for copper thickness and dielectric constant (pink)/Worst case condition for copper thickness and dielectric constant(brown)/Best case condition with additional dielectric layer on top(blue).

In the simulation presented in Figure 5.7, a lossless microstrip line was assumed only to simulate the influence of the characteristic line impedance. The attenuation of the line was neglected. It would change the result clearly on such a long line. Figure 5.7 also shows that the embedded microstrip line signal is slower than the pure microstrip line. A look at Equation 5.4 can easily explain the lower speed of the wave propagation. If on top of the microstrip line, there is air with an $\varepsilon_r = 1$, the effective epsilon is lower than for a fully embedded microstrip where the effective dielectric constant is almost the same as ε_r and therefore, has a lower velocity.

$$v = \frac{c}{\sqrt{\varepsilon_r \mu_r}} \tag{5.4}$$

5.4.2 Differential Microstrip

For a differential transmission line, a characteristic impedance of 100 Ω is the most standard value. This value is also the line impedance specified by the JESD204B standard [24]. The differential impedance combines the two individual line impedances for uncoupled microstrip lines. For example, in the case of two identical and coupled microstrip lines with a characteristic impedance Z_0, this would be:

$$Z_{diff} = 2 \cdot Z_0 \tag{5.5}$$

If the spacing between the two lines gets less than three times the line width [13], the lines' coupling will affect the line's impedance. This impact can be approximated by the following equation [13]

$$Z_{diff} = 2 \cdot Z_0 \cdot \left[1 - 0.48 \cdot exp\left(-0.96 \cdot \frac{s}{h}\right)\right] \tag{5.6}$$

s = space between traces
h = height of the substrate

So, in case the traces are coupled closely, either the copper traces have to be of lower width or the distance between the transmission line and the reference plane has to be decreased. Otherwise, the differential impedance would be reduced.

For example, if the single-ended 50 Ω trace introduced in Section 5.4.1 is used to create a tightly coupled differential pair with a spacing of 6 mil (152 μm) between the traces, this would lower the differential impedance Z_{diff} by about 17.25% according to equation 5.6.

$$Z_{diff} = 2 \cdot Z_0 \cdot \left[1 - 0.48 \cdot exp\left(-0.96 \cdot \frac{0.152}{0.142}\right)\right] = 82.748\,\Omega \tag{5.7}$$

When simulating this setup (line width = 10 mil/ spacing = 6 mil) in Cadence Microwave Office Simulator a differential impedance of 85 Ω is the result. So, the estimation given by Equation 5.6 is relatively close.
As a countermeasure to get $Z_{diff} = 100\Omega$, the characteristic impedance Z_0 of the individual lines has to be increased. It can be increased by lowering the traces' width or increasing the substrate's height. However, changing the height of the substrate is not a practicable option. Adjusting the height would change the characteristic impedance for single-ended transmission lines again. So if coupled differential pairs are used, the differential pair width will always be lower than the single-ended microstrip width.

To get a differential microstrip line with a differential impedance of 100 Ω, according to Equation 5.7, a Z_0 of about 60 Ω is necessary. Applying Equation 5.1 on the given parameters would result in a new line width of 164.5 μm.

To check the quality of this estimation, again, the tuner tool of the Cadence Microwave Office simulator was used to get the optimal line width. In the schematic (Figure 5.8), a Mixed-Mode Converter (MMCONV) was added to simulate the differential pair as a two-port system and directly get the differential impedance. The MMCONV block converts a differential port with a positive and negative pin into a differential and a common part. The common part was connected to the ground for the simulation since the differential impedance is the wanted result. By tuning the line width to the value where the input

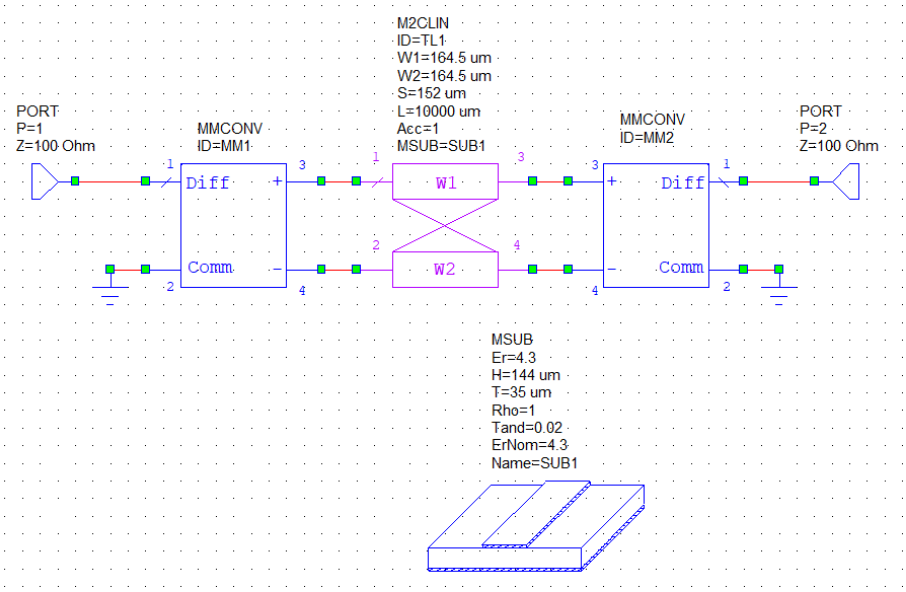


Figure 5.8: Simulation setup for simulating a differential microstrip line.

reflection S11 is the lowest, a best-case width of 177 μm was determined.

The same simulation of a transmission line excited by a step signal as it was conducted for the single-ended microstrip line was also performed for the differential microstrip line. Figure 5.9 shows the simulation result for the differential line, for the best-case differential microstrip line, a differential microstrip line with worst-case copper thickness, and ε_r. The third curve represents an embedded differential microstrip line to simulate a solder stop layer.

The tolerance of copper thickness and the dielectric constant creates a variance in the differential impedance of a little over 3 Ω. This deviation is conclusive since it is almost twice the impedance change than it is for the single-ended microstrip, and in this setup, there is twice the number of lines. However, there is a remarkable deviation in the line impedance for the embedded differential microstrip. As highlighted by Figure 5.9, an additional 10 μm on top of the copper lines decreases the line impedance by more than 10%. So, the influence of a solder mask is more significant for a differential microstrip transmission line than for a single-ended one. This difference could appear because the additional coating influences the characteristic impedance of the single lines, but mainly, the coupling between the lines changes.

5.4.3 Source of Impedance Discontinuities

A perfect transmission line would have no impedance discontinuities and, thereby, no reflections. However, this optimal behavior is hardly achievable in real life. There are many sources of discontinuities in a transmission line. On a microstrip line, for instance, vias for a layer change, mounting pads for components, connectors, or even a bend in the line are sources of impedance variations.

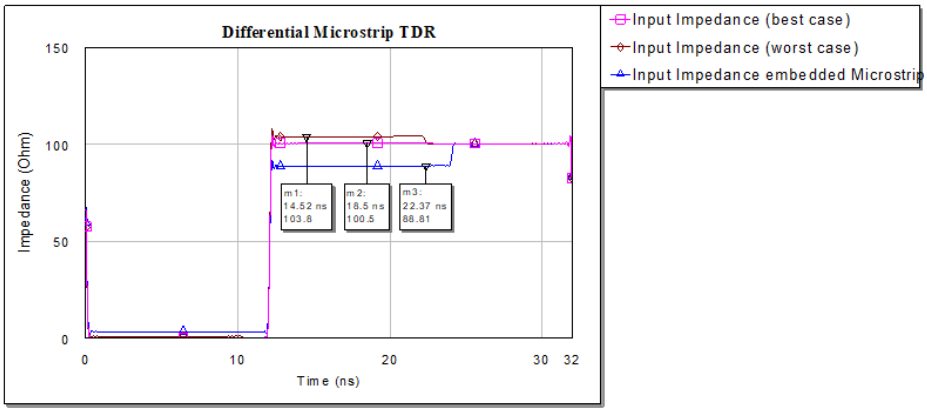


Figure 5.9: Step response simulated for a 100 Ω differential microstrip line in different configurations. Best case condition for copper thickness and dielectric constant (pink)/Worst case condition for copper thickness and dielectric constant(brown)/Best case condition with additional dielectric layer on top(blue).

If possible, the previously mentioned structures should be avoided to design a microstrip transmission line as well as possible. Typically, it is impossible to design a microstrip line without any bends since devices on PCBs cannot be placed so that all copper traces are straight lines. Therefore, bends can be designed for low impedance change. In "Impacts of Bends and Ground Return Vias on Interconnects For High-Speed GHz Designs" [38], the different impacts of different "bend designs" are discussed. The slightest impedance change is shown for rounded bends. Such round bends make sense since the microstrip structure's width-to-height ratio never changes in this structure. Nevertheless, the paper also shows that 45-degree bends are almost as good as rounded corners. Bends with 45-degree angles have the benefit that PCB designs are easier to draw.
Vias should be avoided for high-speed signal lines. The transition from a trace to a via will always generate a change of impedance due to the geometry. Thus, vias should only be used rarely on transmission lines to keep signal integrity high.
The return path must also be considered when placing vias on a signal line. Therefore, there should be at least one via for the return path (e.g., signal ground) next to each signal via. In most cases, this would be a ground via. For signal integrity, it is even better if there are several vias for the return path instead of only one. [38]

5.5 Cross Talk

Cross Talk effects appear if two or more signal lines are placed physically close to each other. In this case, a fast switching signal of one line will induce noise into adjacent signal lines through capacitive and inductive coupling. This noise can reach a high enough level to distort the signal on the victim line significantly. When designing transmission lines, there are several aspects to pay attention to to decrease such distortions.
The main parameters that affect the level of cross-talk are

- the distance between the signal lines,
- the length of the region where the signal lines are coupled and
- the rise/fall time of the aggressor signal.

Far-end cross-talk (FEXT) is the aggressor line's influence on the victim line's far end. The far end is the end of the line, which is further away from the signal source. The FEXT depends on the length of the coupled region (Len) and the rise time (RT).

$$FEXT = \frac{Len}{RT} \cdot k_f \tag{5.8}$$

In Equation 5.8, k_f represents the coupling coefficient, depending on the mutual conductance and the mutual inductance between the coupled lines. This factor depends on the geometry and distance of the aggressor and victim lines. As illustrated in Figure 5.10, the model fits very well with the simulation performed with the Cadence Microwave simulator. For this simulation, a square signal with a rise and fall time of 500 ps was used as the aggressor signal. Under these conditions, the voltage on the far end of the coupled line was five times higher than at the simulation with a 100 ps rise and fall time.

Consequently, for a signal with a very short rise time, the FEXT gets high. However, for high-speed interfaces, typical signal rise times are, for example, a few hundred picoseconds for LVDS [37] or even down to 20 to 30 ps in a JESD204 interface [35]. For such signals, FEXT can get a significant problem on microstrip lines.

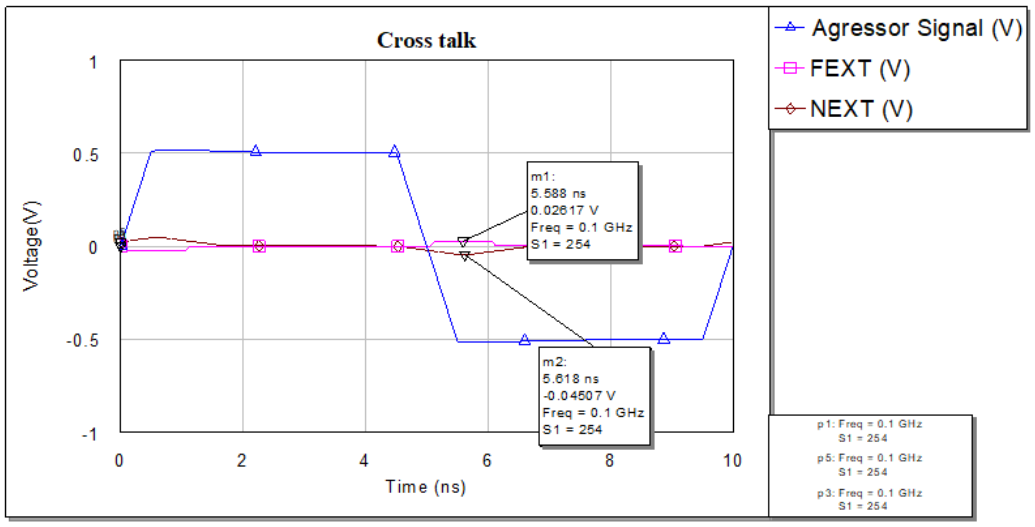
When varying the coupling length, the simulator also shows the same behavior as predicted by Equation 5.8. The voltage at the far end of the victim line is nearly twice the value if the coupling length is 20 cm instead of 10 cm. This doubling of the amplitude is shown in the simulation result in Figure 5.11.

Figures 5.10 and 5.11 also show the independence of the near-end cross-talk (NEXT) amplitude from rise-time and coupling length. The NEXT amplitude only depends on the mutual conductance and the mutual inductance. The only exception would be if the coupled distance is too short, so the NEXT does not reach its maximum magnitude. In this case, the amplitude depends on the coupling length, too.

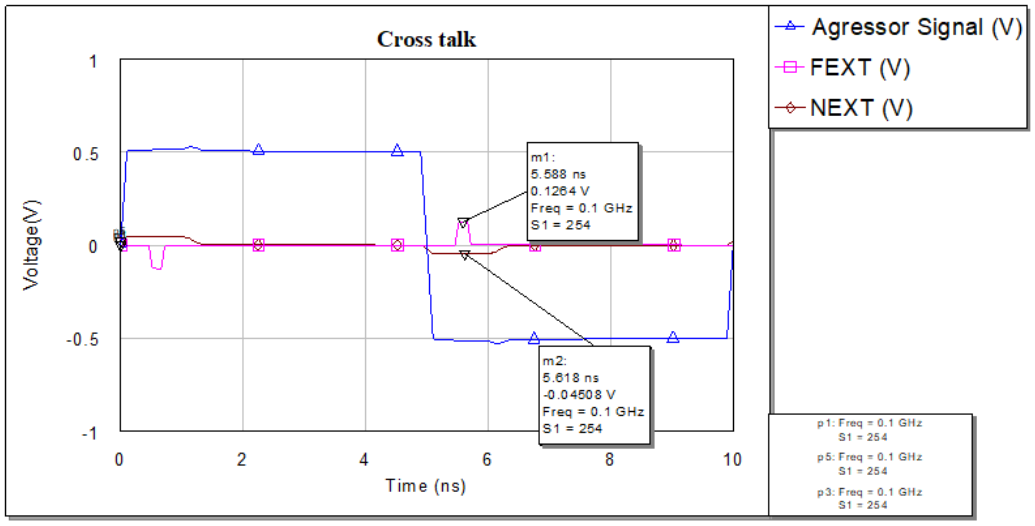
The only effective countermeasure to lower the NEXT would be increasing the distance between the transmission lines. A simulation was performed to show the correlation between the spacing between two coupled lines and the cross-talk effect. The simulation was performed for two coupled microstrip lines. Figure 5.12 shows the result of this simulation. The transmission lines in the simulation model have a width of 254 μm, a coupling length of 10 cm, and variable spacing. The aggressor signal was the same as used for the simulation of Figure 5.11.

The superposition principle is valid for cross-talk effects. For that reason, the cross-talk can get double the size indicated in these simulations if a second aggressor is placed on the other side of the victim line.

Figure 5.12 highlights that the cross-talk can reach up to one-third of the aggressor signal for the given aggressor signal for very tightly coupled lines. The aggressor signal, in this

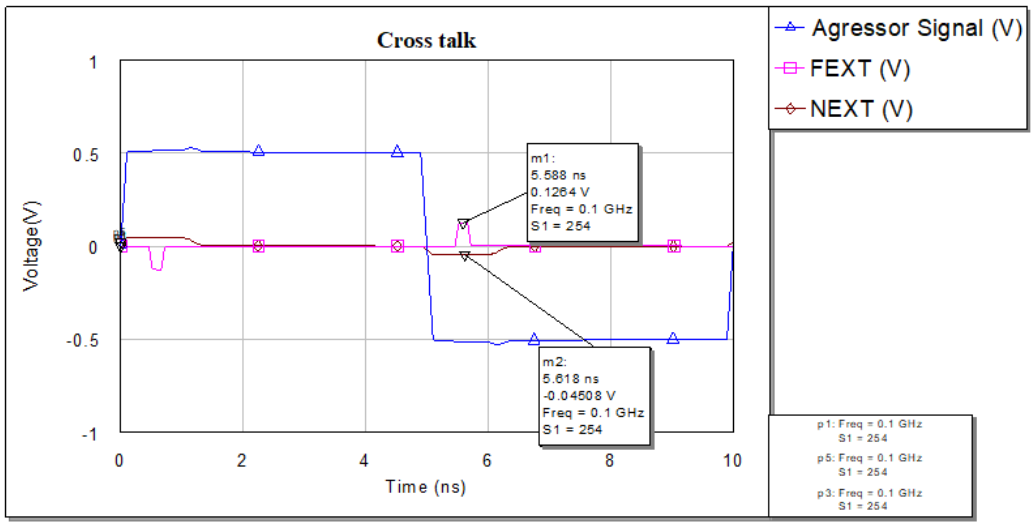


(a) 500ps rise/fall time

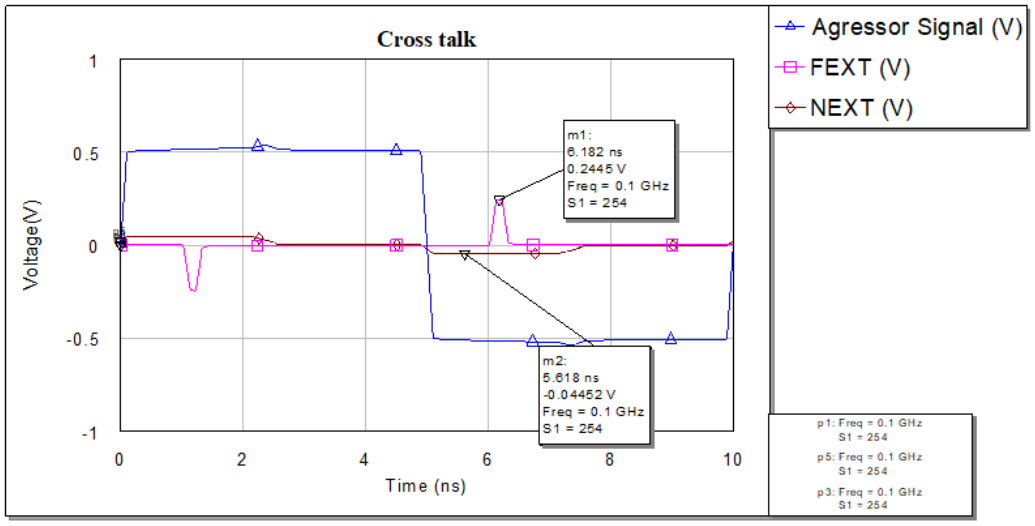


(b) 100ps rise/fall time

Figure 5.10: Crosstalk on a 10 cm long microstrip with 254 μm spacing to the aggressor line.



(a) 10 cm coupling length



(b) 20 cm coupling length

Figure 5.11: Crosstalk on a 10 cm and a 20 cm long microstrip with 254 μm spacing to the aggressor line.

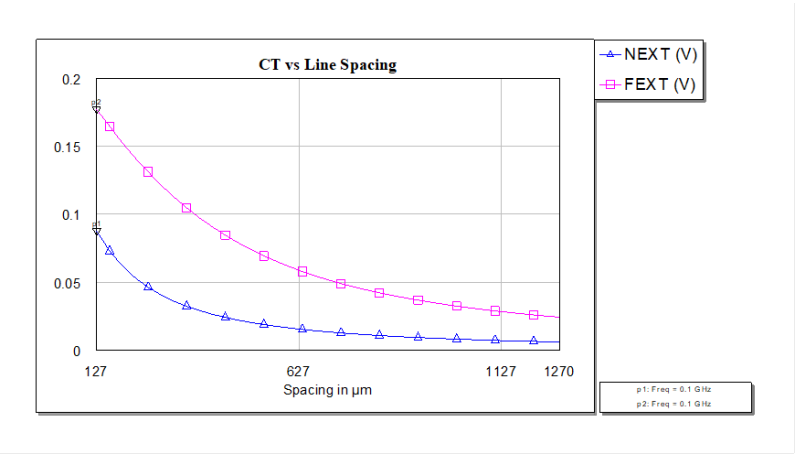


Figure 5.12: NEXT(blue) and FEXT(pink) for varying spacing between coupled lines.

case, has a rise time of 100 ps and an amplitude of 0.5 V. If the spacing between the lines were at least three times the line, the amplitude of the FEXT would be lower than 10% of the aggressor signal.

Since on most PCBs, the copper traces are coated with a solder stop mask, the influence of the coating regarding the cross-talk must be considered, too. Figure 5.13 presents the same simulation as Figure 5.12 with two additional curves for the NEXT and FEXT of an embedded microstrip line. The same values as in Section 5.4.1 were used to predict the impact of the embedding.
An additional dielectric layer is added on top of the microstrip stack-up. It covers the copper trace with an additional 10 μm dielectric layer. This additional layer represents the solder stop of the PCB. The simulation shows that the FEXT of the embedded microstrip line is significantly lower than with the uncovered microstrip line. In contrast, NEXT gets slightly higher for the embedded line.

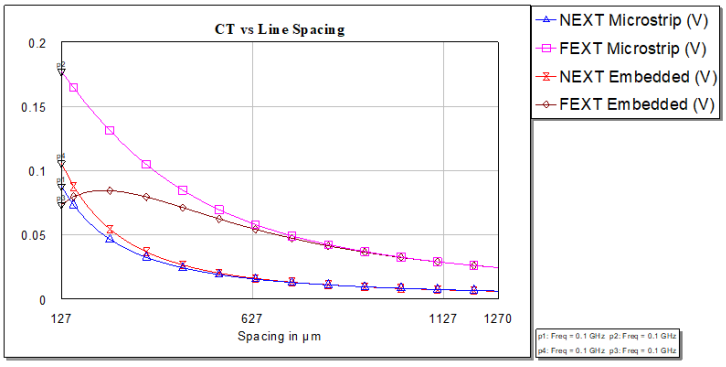


Figure 5.13: NEXT and FEXT for pure microstrip and embedded Microstrip Lines.

The results of this simulation indicate that FEXT can be reduced by coating the transmission line with a thicker solder stop layer. For transmission lines located at the inner

layers of the PCB, as in the case of a stripline design, no part of the electrical field is in the air. The impact of the relative coupling capacitance is, in this case, similar to the relative inductance [13]. This configuration would make the far-end coupling factor $k_f = 0$. Therefore, a stripline design has almost no far-end cross-talk. This relationship is presented in Figure 5.14.

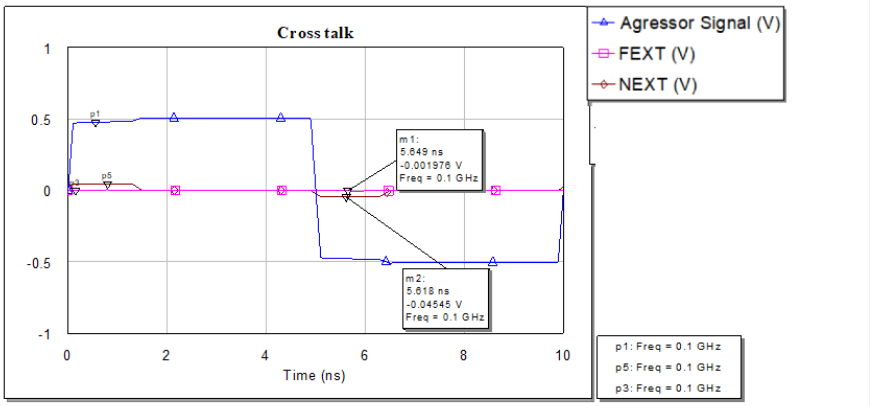


Figure 5.14: Cross-talk simulation for a stripline design. With a square signal as the aggressor signal. Showing FEXT and NEXT signals.

Differential lines are less sensitive to cross-talk. This lower sensitivity is caused by the aggressor line, which induces a voltage into both differential pair lines. Therefore, the impact of cross-talk on the differential signal is less than on a single-ended signal line. For differential pairs, an additional parameter affects the cross talk, the coupling between the two lines of the differential pair. The tighter the coupling between the two lines of the differential pair is, the less difference is between the voltages induced by the aggressor. Thus, the impact of cross-talk on the differential signal gets smaller when the differential pair's coupling gets tighter.
In Figure 5.15, the same simulation as for Figure 5.12 is presented, except that the differential signal of a differential pair is taken as the victim signal. It can be recognized that the FEXT (pink lines) is at least 16% lower than in the single-ended model. In the case of the tightly coupled model (dark pink line), the FEXT is even 33% lower. So, the FEXT can be reduced by one-third when using a differential pair instead of a single-ended transmission line. Of course, this is only valid for the differential part of the signal. However, the common-mode voltage is not an issue since most differential inputs have a high common-mode rejection ratio (CMRR).
The NEXT on the loosely coupled differential pair (light blue line) has almost the same values as the single-ended signal. That the NEXT is not reduced for differential pairs can be explained because the NEXT effect on the higher distanced line is already so low that it almost does not affect the signal on this line. So, only the closer line is affected by the NEXT induced from the differential signal. For the tightly coupled differential pair (dark blue line), the NEXT is even lower than for the single-ended line.

The NEXT on the loosely coupled differential pair (light blue line) has almost the same values as the single-ended signal. This behavior is introduced by the higher distance between the aggressor line and the differential line that is further away. The NEXT is already so low that it almost does not affect the signal on this line. Thus, the NEXT induced from the differential signal affects only the closer line. For the tightly coupled differential pair (dark blue line), the NEXT is even lower than for the single-ended line.

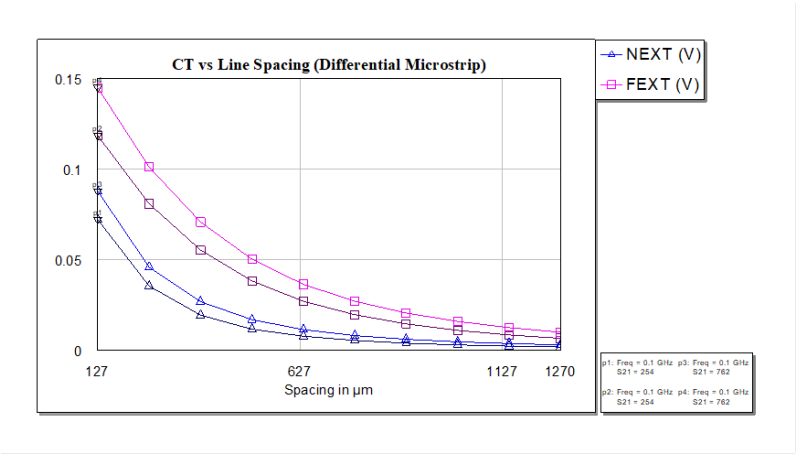


Figure 5.15: Cross-talk on a differential microstrip.

Also, the case of embedded lines has to be considered for differential microstrip lines. Figure 5.16 compares NEXT and FEXT of the pure and embedded microstrip. As can be seen, the FEXT of the embedded differential pair is noticeably smaller than the FEXT of the standard differential pair, the same as for the single-ended line. The NEXT is slightly higher in the embedded case but only for a shallow distance.

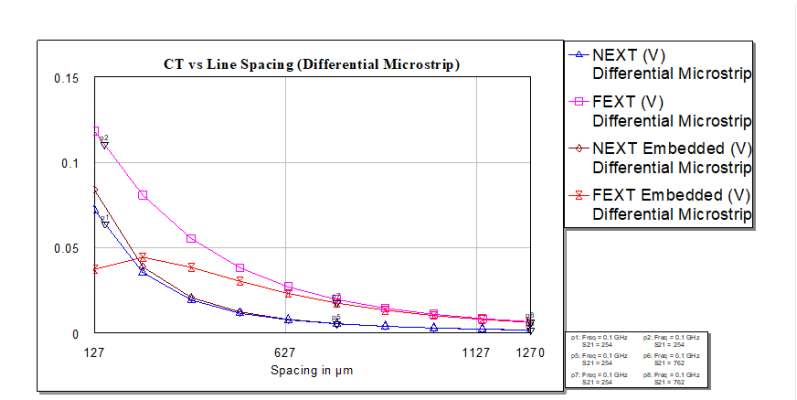


Figure 5.16: Cross-talk on a differential microstrip.

If the aggressor line were a differential pair, the influence of cross-talk would be further minimized. The two lines of a differential pair would be separate aggressor lines that transmit opposite signals so that they would cancel each other at least partially. So, three

straightforward steps can be applied to lower cross-talk in a high-speed data interface. On the one hand, using differential signaling, and on the other hand, cover the copper traces with some dielectric material. The most effective but often hardly possible measure is to place transmission lines far away from each other.

5.6 Transmission Line Attenuation

A transmission line's attenuation α consists mainly of two parts. On the one hand, the conduction attenuation α_c and on the other hand, the dielectric attenuation α_d.

$$\alpha = \alpha_c + \alpha_d \tag{5.9}$$

The conduction attenuation depends on the signal line's frequency and geometry.

$$\alpha_c = \frac{R_s}{Z_0 w} Np/m \tag{5.10}$$

Here, w identifies the width of the transmission line, and R_s summarizes the frequency-dependent surface resistivity of the copper line. It is defined by $R_s = \sqrt{2\pi f \mu_0 / 2\sigma}$ [31]. Equation 5.10 shows that making the transmission line wider will keep α_c low.

The dielectric attenuation is polarization loss in the dielectric material around the transmission line. This polarization loss depends on the dielectric layer's material properties, as shown in Equation 5.11 [31].

$$\alpha_d = \frac{\omega}{c}(tan\,\delta)\frac{\varepsilon_r(\varepsilon_e - 1)}{2\sqrt{\varepsilon_e}(\varepsilon_r - 1)} \tag{5.11}$$

Equation 5.11 highlights that α_d is independent of the geometry of the line. It depends only on the frequency and the dielectric properties ε_r and $tan\delta$. Hence, changing the PCB's dielectric material is the only way to lower the dielectric attenuation for a given signal. If a signal with lower frequencies or lower rise/fall times can be used, this is another way to lower the dielectric attenuation. A lower signal frequency also reduces the conduction attenuation. So, for both types of attenuation, frequency is a crucial factor.
In Figure 5.17, the curves of α, α_c and α_d are displayed for a $254\,\mu m$ wide $50\,\Omega$ microstrip line on a standard FR-4 substrate ($\varepsilon_r = 4$, $tan\delta = 0.02$). The graphs show that conductor attenuation is the main contributor to the overall attenuation in a lower frequency range. If the frequency exceeds a few hundred MHz, the dielectric attenuation gets the dominant part of the attenuation. In the case of transmission lines designed for high data rates, attenuation can be a limiting factor. Since the attenuation is proportional to the length of the transmission line, there are two countermeasures to reduce attenuation for high-speed applications. One is to shorten the length of the transmission line. The second option is to use PCB material with a low loss tangent ($tan(\delta)$). Megtron 6 [3], for instance, is such a low-loss material.

A simple calculation shows how frequency-dependent attenuation affects a digital signal. As an input signal, a trapezoidal signal with a rise time of 20 ps and a magnitude of 1 V

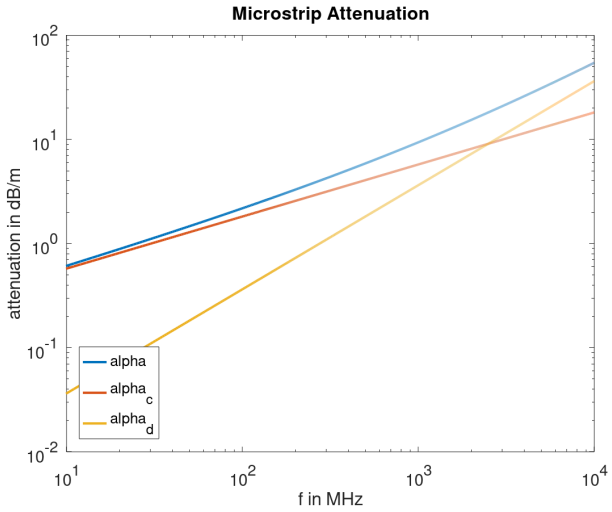


Figure 5.17: Attenuation factors ($\alpha, \alpha_c, \alpha_d$) over frequency.

peak-peak is used. Figure 5.18 presents the according signal as a blue line. With the fast Fourier transformation, the given digital signal is converted to the frequency domain. The frequency-dependent attenuation is applied to the converted signal by multiplication in the frequency domain. After that step, the signal is converted back into the time domain. Figure 5.18 presents the initial trapezoidal signal (blue) and the resulting signal (orange) after applying the frequency-dependent attenuation. As expected, the high-frequency content of the signal is attenuated stronger than the low-frequency part. So, the attenuated signal (orange) has an increased rise time, and the edges of the signal are much smoother than the edges of the initial signal.
For the example presented in Figure 5.18, the attenuation was calculated for a $254\,\mu m$ wide $50\,\Omega$ microstrip line with a length of 10 cm. The dielectric material parameters were taken from standard FR-4 material, $\varepsilon_r = 4.3$ and $tan(\delta) = 0.02$.

In the case of a stripline, the effect is similar to the presented calculations. The dielectric conductance is more prominent for the stripline as the transmission line is fully embedded in the dielectric material. For microstrip, the electrical field is partially in the air where almost no dielectric attenuation is recognizable.

5.7 Differential Pair Length Matching

One challenge of differential signaling is the inter-pair length matching of the differential pair. By inter-pair length matching, the adjustment of the two lines of a differential pair to have the same length is meant. An ideal differential signal has a phase offset of 180 °. However, the phase offset will change if the signals on the two lines are not equally fast. Such phase difference causes a partial conversion from the differential to the common-mode. Usually, common-mode signals are not a big issue since most differential receivers suppress common-mode signals well. Nevertheless, if the common-mode signal is created through mode conversion, this reduces the signal quality. The problem can be shown in the time domain, as it is visualized in Figure 5.19.

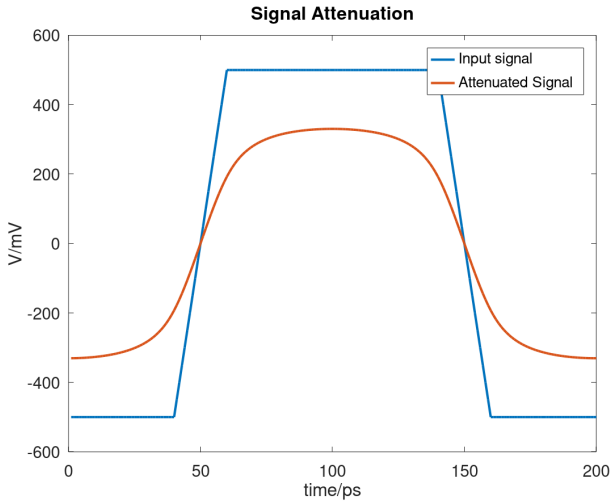


Figure 5.18: Digital signal (blue) and attenuated signal (orange) at the end of a 10 cm microstrip line.

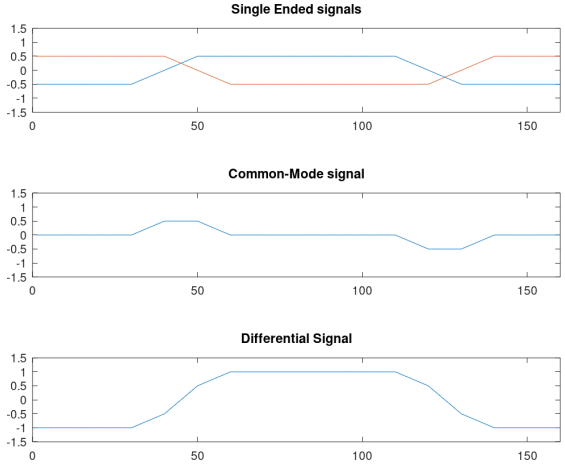


Figure 5.19: Simulation result for a differential pair inter-pair mismatch.

The more the phase shift between the two differential parts differs from 180 °, the more common mode signal is present. The effect on the differential signal is pointed out in the lowest graph of Figure 5.19. For a digital signal, this would mean the eye is closing. Signals with a lower rise and fall time make the opening in the eye diagram smaller. The relationship to the physical length is given via the phase velocity v. Equation 5.12 shows how the mismatch's length and timing relate.

$$\Delta l = v \cdot t \tag{5.12}$$

The closer the lengths of the lines are, the less mode conversion will take place. According to the authors of "High Speed Digital Design: Design of High Speed Interconnects and

Signaling" [40], a line length difference of below 5 mils is a good design target. In this case, some tolerance is left if several boards are connected.

5.8 Via Influence

Another structure that has a significant influence on signal integrity is the via. Vias create a discontinuity in the characteristic impedance of a transmission line. Many parameters are relevant for good via design. First, the geometry of the via has to be defined. The via diameter, pad size, and anti-pad size define the geometry. Anti-pad size is the space without copper around the vias pad. Another essential information is the information which signal layers the via interconnects. A third important aspect is the return path. The return current will also change layers but through another via. Therefore, ground vias should be placed next to the via on the signal line.

The Saturn PCB Toolkit [30] can be applied to get a first estimate of suitable via dimensions. The minimum via diameter of 0.2 mm and the standard PCB thickness 1.6 mm are taken as a starting point. A diameter of 0.5 mm is used for the via pad size since this gives the most petite annular ring standard PCB manufacturers produce without extra cost. Given these parameters, the PCB Toolkit calculated an anti-pad diameter of 0.83 mm to get a via impedance of about 50 Ω.

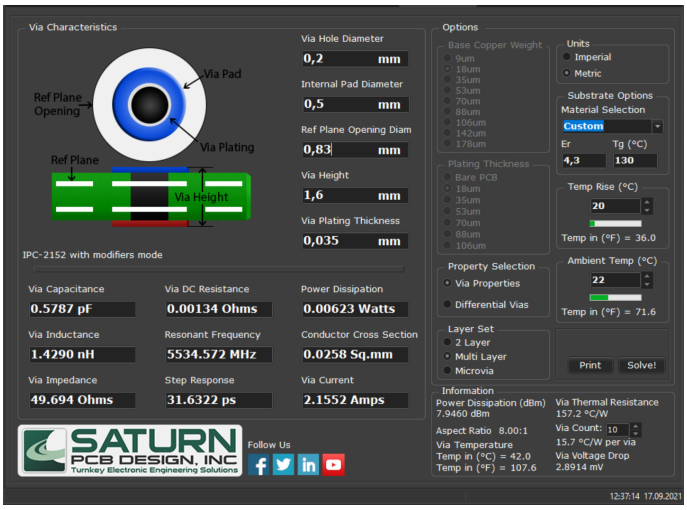


Figure 5.20: Saturn PCB Toolkit

To get a differential impedance of 100 Ω with two vias of the same dimensions, the PCB Toolkit proposes a center-to-center distance of 1.0 mm.

5.9 DC blocking

A DC blocking element is placed on a transmission line to minimize a signal's common-mode part (also called the DC part). Therefore, a simple series capacitor can be used. To

keep the reflection at the transition to the capacitor low, the width of the capacitor should be about the same as the width of the transmission line. For example, a 0201 capacitor is 20 mil long and 10 mil wide. With these dimensions, it fits exactly on a 10 mil wide signal trace. Another reason to use capacitor values this small is that such small components perform better at high frequencies because of lower parasitic effects.
The value of the capacitor depends on the minimum signal frequency at which the transmission line will be operated. Texas Instruments gives a formula to get a value for the coupling capacitance to help connect high-speed ADC interfaces. [19]

$$Z_C = \frac{1}{2\pi f_{clk} C} \tag{5.13}$$

Nevertheless, the chip most manufacturers already recommend capacitance values for the AC coupling.
The location of the capacitor on the line can influence the quality of the signal, too. Of course, a capacitor creates a discontinuity in the line impedance and, therefore, some reflection. Simulation results published by Gustavo Blando [11] show that the best position to place a DC-blocking capacitor is close to the line end. Whether this is the transmitter or receiver side has no significant influence on the signal quality.

Chapter 6

Measurement Methods

There are various methods to measure transmission lines and impedances. They can be separated into two main groups. There are measurements in the time domain and measurements in the frequency domain. For example, time domain reflectometry (TDR) measures the behavior of a transmission line over time. On the other hand, a vector network analyzer (VNA) measures the electrical network's behavior over a specific frequency range.

The benefit of time-based measurements is that the transient behavior of a signal on a transmission line or in a system can be captured. Thus, variations along a transmission line could be assigned to certain positions on the line. Furthermore, a system changing its behavior over time could be detected.

This kind of information is not directly available for frequency domain measurements. On the other hand, VNA measurements have the benefit of showing the reflections of a network over a specific frequency range. This information is, for instance, important when measuring antenna designs. This information allows measuring an antenna's resonance frequency directly.

6.1 Time Domain Reflectometry

As the name already says, the TDR measures reflections in the time domain. An initial signal is injected into the system that should be characterized. The reflections generated by the system are then measured [29]. The initial signal is typically a very short pulse or a step signal with a very short rise time. Modern measurement equipment can create edges with a rise time of less than 7 ps. [32]

How steep the edge of the initial signal should be depends on two conditions. First, it depends on the bandwidth for which the system under test is designed [34]. Of course, a higher bandwidth requires a lower rise time of the injected pulse. Figure 6.1 shows a table of TDR rise time recommendations. This table is from a Tektronix application note [34]. It correlates established data interfaces with their bandwidths and the recommended TDR rise time for each interface.

In addition, it is crucial to define the TDR rise time as the smallest distance between

Standards		Standards Characteristics				TDR Rise Time Needs	
		Data Rate (Gb/s)	Bit width (ps)	Rise time spec'ed ps*	Rise time est., ps*	Reflected t_{TDR} needs, ps**	Tektronix module
1st generation standards, t_{rise}* = 15% of bit width	Infiniband	2.50	400	100	60	40(30)	80E04
	PCI Express	2.50	400	50	60	40(30)	80E04
	SATA II	3.00	333	67	50	34(25)	80E04
	XAUI	3.125	320	60	48	32(24)	80E04
2nd generation standards, t_{rise}* = 20% of bit width	4 Gb/s FC	4.25	235	60	47	32(24)	80E04
	SATA II	6.00	167	N/A	33	22(17)	80E08
	Double XAUI	6.25	160	N/A	32	21(16)	80E08
3rd generation standards, t_{rise}* = 25% of bit width	8 Gb/s FC	8.50	118	N/A	29	32(24)	80E08
	10 G Base-R	10.31	97	24	24	20(15)	80E10
	10 G Base-R FEC	11.10	90	24	23	15(11)	80E10

* 20-80% rise times, when available from a standard
** 10-90% TDR rise time specifications (20-80% equivalent provided in parenthesis)

► **Table 4.** *Reflected TDR rise time requirement for standards.*

Figure 6.1: TDR timings recommended by Tektronix application note. [34]

two impedance changes [34]. The rise time should be shorter than the shortest propagation delay between two impedance changes in the system. With this condition fulfilled, the measurement resolution is high enough to identify all discontinuities in the measured system. According to the Tektronix application note, using at least the third harmonic (for faster standards) or even the fifth harmonic frequency as measurement bandwidth is recommended. For a 10 Gb/s interface, this would be 15 GHz.

When capturing the reflections of the system to measure, the initial pulse is ignored. The signal sampling only happens in a particular time window after injecting the initial pulse. Hence, all signal changes after the measurement device's initial pulse are covered reflections.
TDR measurements usually apply a sampling oscilloscope measurement principle. The measurement is executed with a relatively low sampling rate of a periodic signal. This relatively slow measurement is repeated to get a higher number of sampling points. For every measurement cycle, the sampling point is moved by a minimal time gap against the initial pulse. This movement of the sampling point is usually performed by using a delay line with a variable time delay. The measurement and the moving of the sampling point are executed repeatedly with a sampling rate of typically a few hundred kSps. If all the measured values are combined to one result, a measurement with high time resolution is the outcome. This result covers all reflections created by the device under test over time.

Any change in the measured voltage can be related to a corresponding impedance variation from the time domain measurement. By this approach, the impedance changes in the system can be determined. Through that analysis, TDR makes it possible to measure characteristic impedances of transmission lines.

6.1.1 Transmission Line Measurement

For transmission line measurements, the capturing window must be long enough to measure at least one complete signal propagation along the transmission line and back again. If the capturing window is selected long enough, all impedance changes (e.g., vias or bends in a microstrip line) can be seen in the measured signal trace. This feature makes TDR useful for detecting and locating problematic structures (such as vias or connectors) in a transmission line.
On the other hand, TDR also allows to check if a transmission line has the correct characteristic impedance. Thereby, the correctness of the design and the production of the PCB can be verified.

6.1.2 S-Parameter Measurement

TDR measurement also offers the possibility of providing the S-parameters of a system [29]. Therefore, the measured time domain signal is transferred into the frequency domain. This transformation can be achieved by using fast Fourier transformation.

6.2 VNA Measurement

A vector network analyzer measurement is a frequency domain measurement. A sinusoidal signal with a specific frequency is injected into the device or network, which should be analyzed. The signal reflected by the network is extracted in the VNA using a directional coupler. This directional coupler couples only the incoming signal to the measurement path but not the outgoing. Such directional couplers only work for AC signals. For this reason, VNAs cannot characterize systems for very low frequencies or DC signals.
The frequency of the injected signal is swept in a defined measurement range with a defined step size. For each step, the reflected signal is measured. Comparing the injected signal to the reflected part gives the S-Parameter S11.
For two-port measurement, the reflected portion of the signal is measured, and the signal received on the other side of the system (e.g., a transmission line) is measured. This measurement provides the insertion loss S21, too.

Some VNAs do have a TDR measurement option, too. In this case, the S-Parameters are measured in the frequency domain, and the time domain signal is calculated using the inverse Fourier transformation. The accuracy in terms of timing resolution for this kind of TDR measurement is strongly dependent on the frequency range the VNA can operate.

Chapter 7

Measurements

Two different types of measurements are performed to check the design of an existing PCB design. On the one hand, a transmission line of a stacked PCB setup designed as a gigabit interconnect is characterized. On the other hand, the S-Parameter of a Xilinx gigabit receiver is captured. A high-speed oscilloscope (Keysight N1000A DCA-X [33]) with TDR functionality is used for both measurements. The oscilloscope is equipped with four TDR probe heads (N1055A [32]). With four probe heads, it is possible to conduct a differential transmission line on both ends and measure even the time domain transmission (TDT) and not just time domain reflection (TDR). Before the measurement, the probes get calibrated in the frequency range of DC up to 35 GHz using a mechanical calibration standard.

7.1 Transmission Line Measurement

A TDR/TDT measurement is performed to characterize the transmission line of an already working design. Figure 7.1 shows the schematic representation of the setup used for the transmission line measurement. Two adapter boards are used to connect to the board under test (the mainboard). The adapter boards allow conducting of transmission line measurements on the mainboard via two 2.92 mm coaxial connectors.

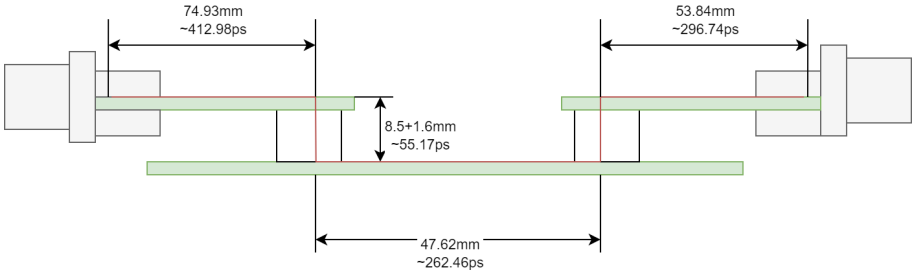


Figure 7.1: Schematic representation of measurement setup. Two 2.92 mm connectors (grey) interface the transmission line (red) on the main board via two board-to-board connectors(white).

The measurement is performed twice to compare two different mainboards. The only

difference between the two boards is the material used in production. The material IT-968, with a dielectric constant of 3.7 for the first mainboard, was used for the dielectric layers. The differential pairs on this board were designed to have a characteristic impedance of approximately 100 Ω for an ε of 3.7.
The second board is built with IT-180A material. This material has a dielectric constant of approximately 4.3. The loss tangent of the IT-180A is approximately 0.016. Since the dimensions of the differential pairs are the same for both boards, the higher dielectric constant will cause a lower characteristic impedance.

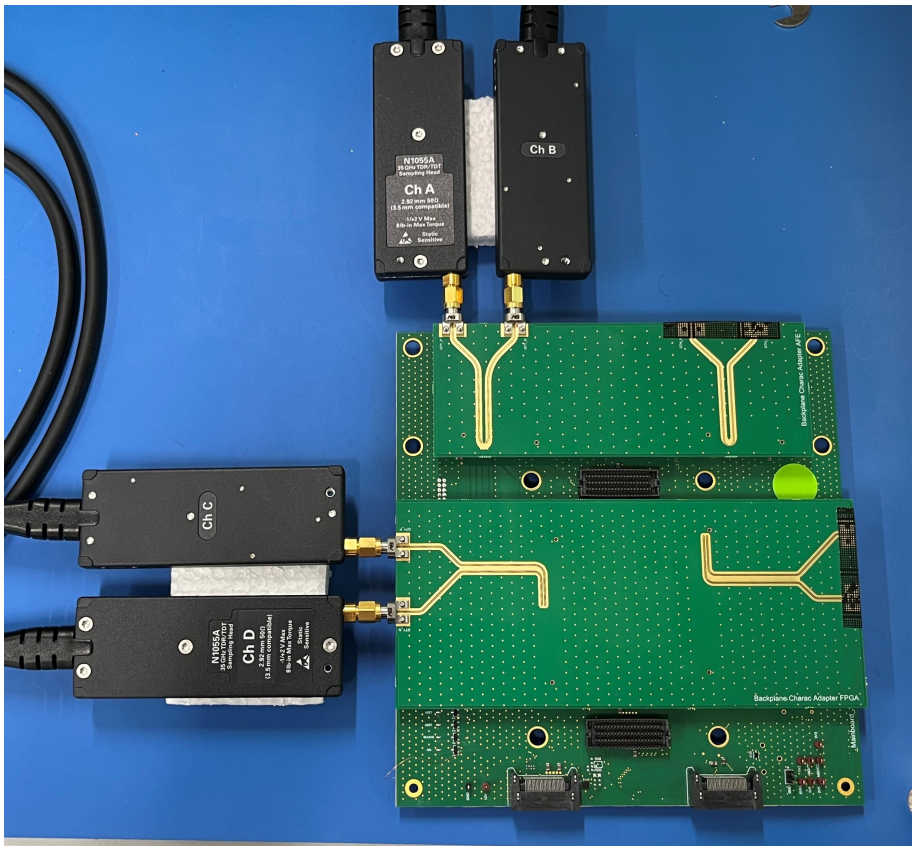


Figure 7.2: Picture of the TDR measurement setup in the laboratory. The two adapter PCBs with the 2.92 mm connectors stacked on the mainboard to characterize. The TDR probes are connected to the boards on the top and left side of the picture.

Two results are of interest for this measurement. The first one is the pure TDR measurement of the transmission line. The timing representation indicates where impedance changes appear and how significant the impact of these changes is.

The second result of interest is the S-Parameters of the transmission line. The S-parameters characterize the transmission line in the frequency domain and allow further analysis using simulation software on a PC.

7.1.1 TDR Measurement

Figure 7.3 shows the TDR measurement for the setup with the first mainboard (IT968). The TDR signal used for this and the following measurements is a differential voltage step of 0.4 V amplitude and a rise time of 32 ps.
In the timing diagram, the transitions between the adapter PCBs and the main PCB can be seen very well. At about 850 ps, a peak up to about 110 Ω can be recognized in the measurement. The reflection at the transition between the adapter board and the mainboard causes this peak. A second impedance change at time 1700 ps can be interpreted as transitioning to the second adapter board.

The signal is almost constant between these two timings at about 90 Ω. In this range, the value is equivalent to the characteristic impedance of the transmission line on the mainboard.

Figure 7.3: Screenshot of the TDR measurement showing the impedance traces for the measurement setup with the IT968 mainboard. The yellow line is the differential impedance, and the green represents the common-mode impedance.

Figure 7.4 shows the TDR result for the second mainboard (IT-180A). In this screenshot the same transitions can be seen as for the previous measurement. The main difference is that in the time frame where the signal represents the characteristic impedance of the mainboard, the signal is lower than for the measurement with the IT-968 material. Thus, for the second mainboard, the characteristic impedance of the differential pair is slightly higher than 80 Ω.

The higher dielectric constant of the IT-180A material results in a lower characteristic

Figure 7.4: Screenshot of the TDR measurement showing the impedance traces for the measurement setup with the IT180-A mainboard. The yellow line is the differential impedance, and the green identifies the common-mode impedance.

impedance, as expected. Figure 5.4 shows exactly that relation for varying ε_r. The higher the dielectric constant gets, the lower the impedance will be.

The second line (green) in Figures 7.3 and 7.4 shows the common mode component of the differential pair. This information highlights, for instance, a mismatch between the two lines of the differential pair. In these measurements, the common-mode part is almost zero all the time. This result means that there is no mismatch between the P and N parts of the differential pair.

7.1.2 S-Parameter Measurement

The oscilloscope also provides S-parameters as a measurement result. The measured time domain signal is transformed to the frequency domain using FFT to get the S-parameters. Figure 7.5 shows S11 (yellow) and S21 (blue) of the measurement setup (IT968) provided by the oscilloscope.

Figure 7.6 shows the S-parameters of the second board (IT180-A). The comparison shows that the S21 parameter for the IT968 mainboard is lower than for the IT180-A board.

Using the S-Parameter S21, the transmission of a signal over the system can be simulated. To accomplish such a simulation, Cadence Microwave Office was used. The S-parameter file gets imported and connected to two mode-conversion blocks (single port to differential port conversion).

Figure 7.5: S-Parameter representation of the measurement results for the IT968 mainboard.

Figure 7.6: S-Parameter representation of the measurement results for the IT180-A mainboard.

The simulation software can calculate an eye diagram with the imported S-parameter information. Therefore, various combinations of a digital bitstream are generated by the simulation software and then used as an input signal. This signal was transformed using the S-Parameter, and the result shows how the output signal would look according to the simulation. For the simulation, a 10 GBit/s digital signal with a rise and fall time of 20 ps was considered. The amplitude of the signal is normalized to a magnitude of one.
Figure 7.7 shows the eye diagram simulating the S21 of the IT968 mainboard. Figure 7.8 shows the eye diagram simulation of the IT180-A mainboard.

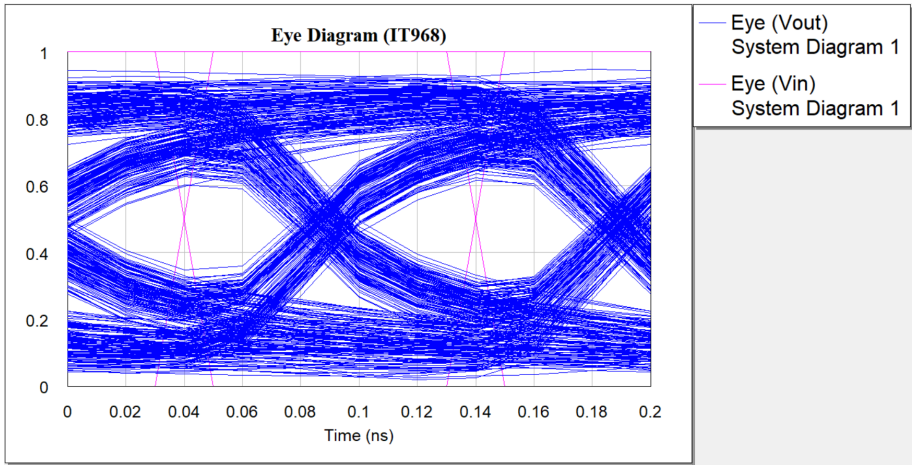


Figure 7.7: Cadence Microwave Simulation result for an eye diagram simulation with the S-parameters of the IT968 mainboard.

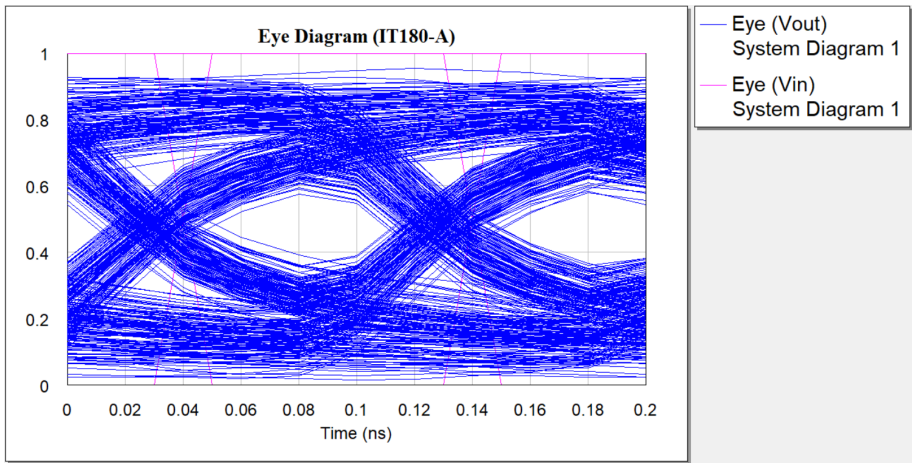


Figure 7.8: Cadence Microwave Simulation result for an eye diagram simulation with the S-parameters of the IT180-A mainboard.

7.2 Xilinx Gigabit Receiver Measurement

A TDR-based S-Parameter measurement is performed to characterize the receiver of a Xilinx gigabit module. Figure 7.9 shows the gigabit receivers frontend circuit provided by Xilinx in the FPGAs datasheet [39]. The two 50 Ω termination resistors are calibrated according to Xilinx. The measurement does not include the two 100 nF series capacitors drawn in Figure 7.9. The measurement is performed without any external circuitry and with the Xilinx FPGA in an unpowered state.

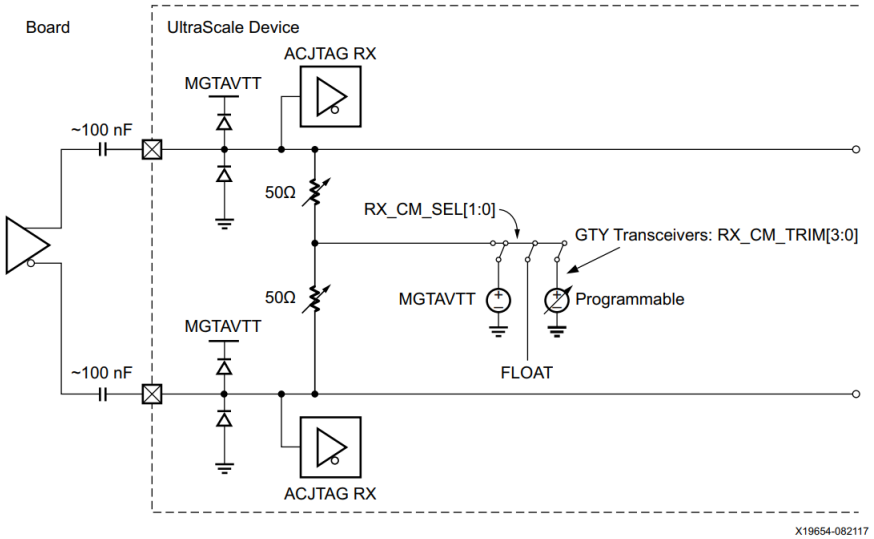


Figure 7.9: Analog front end of the Xilinx GTY receiver [39].

Figure 7.10 shows the schematic representation of the setup used for the S-Parameter measurement. The Xilinx FPGA is assembled on a PCB that can be connected via PCB connectors. A special adapter board is used to interface this board. This adapter board allows the FPGAs gigabit transceiver to be conducted via a 2.92 mm coaxial connector.

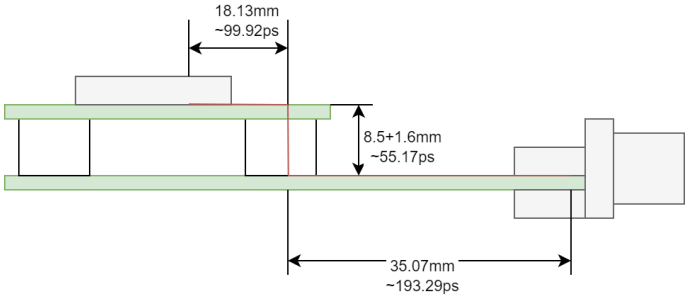


Figure 7.10: Schematic representation of Measurement setup. A 2.92 mm connector (grey) interfacing the FPGAs receiver via a carrier PCB connected through a board-to-board connector(white).

Figure 7.11 shows the final measurement setup that is used in the laboratory.

Figure 7.11: Picture of the measurement setup in the laboratory.

The result of the TDR is presented in Figure 7.12. Similar to the mainboards' TDR measurements, the transition from the adapter board to the PCB carrying the FPGA can be seen very well. At a time of 800 ps to 900 ps, an impedance change indicates the board-to-board connector.

Figure 7.12: Screenshot of the TDR measurement showing the impedance trace for the measurement setup and the FPGAs gigabit receiver.

At about 1.47 ns, the transition from the PCB to the FPGA can be seen. By limiting the TDR recording time, it is possible to get only the characteristics of the receiver front end.

The recording scope was set to record only the time window of the transition from the PCB to the FPGA and the FPGA itself. Figure 7.13 shows the according time window.

Figure 7.13: Screenshot showing the time window of the TDR measurement used for getting the receiver characteristics.

With this TDR recording, the S11 parameter of the gigabit receiver can be calculated and provided by the oscilloscope. The S11 parameter imported into Cadence Microwave Studio can be displayed as a Smith chart. Figure 7.14 shows the resulting Smith chart. The chart shows a very centered spiral. This behavior means that the matching is relatively good. There is no tendency in a single direction. So, no purely capacitive or inductive mismatch can be detected.

7.3 Discussion

The TDR measurements in Section 7.1.1 show how important careful impedance matching is. Figure 7.6 shows a significant impedance mismatch due to a changed dielectric constant. This mismatch demonstrates the importance of knowing which material is used for PCB production. Also, it is essential to see that if a material change is necessary, the transmission line dimensions must be adapted, too. This mismatch's impact on a signal can be seen in Figures 7.7 and 7.8. Figure 7.7 shows the eye diagram for the setup with the IT968 mainboard, and Figure 7.8 shows the eye diagram for the IT180-A mainboard. The eye-opening for the IT180-A mainboard with a significant impedance mismatch is only 10 % to 15 % of the initial signal. On the other hand, the eye diagram of the IT968 mainboard has a larger opening. For this mainboard, the eye-opening is over 20 % of the initial signal. Figures 7.15a and 7.15b show the eye diagrams with the JESD204B receiver

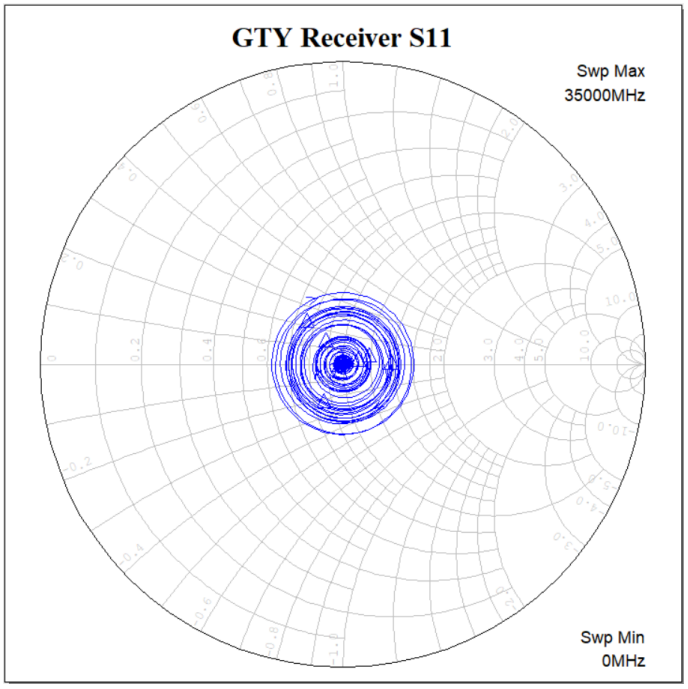
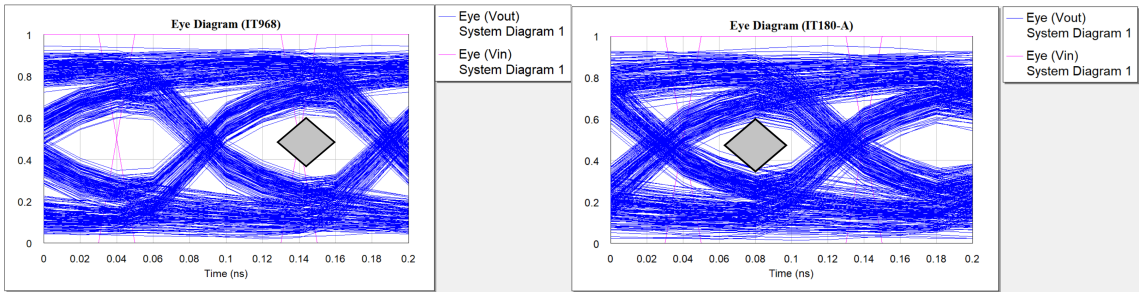


Figure 7.14: Smith-Chart showing the measured S11 parameter of the FPGAs gigabit receiver from 0 to 35 GHz.

eye-mask as an overlay. It can be seen that for the IT968 mainboard, which has a correctly matched line impedance, the mask fits into the calculated eye diagram. The eye diagram calculated for the IT180-A mainboard does not fit into the JESD204B receiver mask. So, the impedance mismatch of the transmission line on this board is a problem for the data interface.

Another remarkable understanding is that the characteristic impedance can change significantly even for two equivalent designs. In Figure 7.3 the section from about 100 ps to 700 ps and the section from about 1850 ps to 2900 ps are the two adapter boards. The transmission lines on both boards were designed with the same dimensions and ordered with the same dielectric material. So, this variation between the two impedances must be caused by some difference in the production of the PCBs. Further analysis is necessary to determine if the mismatch is due to a different material or tolerances in manufacturing the boards. For instance, an X-ray can be done to check if the microstrip line and the layer stack dimensions are correct.
Also, these measurements can show the impact of transmission line coupling on the line impedance. The measurement screenshot in Figure 7.5 highlights that at the very beginning, there is a peak of about 110 Ω. This peak can lead back to the uncoupled part of the line that connects the two coaxial connectors to the differential line.

For the characterization of the Xilinx gigabit receiver, an input impedance of 100 Ω is expected according to Figure 7.9. According to the time domain measurement (Figure



(a) Cadence Microwave Simulation result for an eye diagram simulation with the S-parameters of the IT968 mainboard.

(b) Cadence Microwave Simulation result for an eye diagram simulation with the S-parameters of the IT180-A mainboard.

Figure 7.15: Simulated eye diagrams with JESD204B receiver mask overlay.

7.12) the input impedance of the receiver is about 84 Ω to 90 Ω. What can be seen in Figure 7.12 is the common-mode signal (green line). This signal indicates a mismatch between the two paths of the differential line. The asymmetrical behavior can occur due to the missing supply of the gigabit receiver. Since the measurement is passive, without supplying the measured device, the diodes at the receiver's input can show different behavior for the positive and the negative input pins. To analyze the receiver in the frequency domain, the s-parameter S11 is plotted into a Smith chart (Figure 7.14). There, it can be seen the receiver matches very well to 100 Ω for high frequencies. For lower frequencies, the receiver's impedance is slightly mismatched. Still, the deviation in the Smith chart is symmetrical around the center. This centered position means no pure inductive or capacitive mismatch. The mismatch is assumed to be created through parasitics from the package and the via used to connect the FPGA ball.

Chapter 8

Conclusion

This thesis addresses various methods to assess, avoid, and locate signal integrity issues at high-speed PCB interconnects. It is shown that simple calculations can already help to estimate specific impacts on the signal integrity. For instance, the attenuation on a signal line can be calculated rather well with basic mathematics. Also, simulation helps to assess issues like cross-talk. A simple simulation using a 2D solver gives already reasonable estimates about the impact that can be caused by cross-talk between transmission lines.

On the other hand, there are also parameters like the characteristic impedance of a transmission line. One can calculate and even simulate a perfectly matched transmission line, but in the end, there will always be tolerances in the manufacturing process. So, the impedance of a microstrip line can only partially be controlled. Up to 10% impedance variation is possible only due to production tolerances. Additionally, some parameters can not be verified directly, such as the correctness of the material's dielectric constant. This is hard to prove if the manufacturer uses the wrong materials in production. However, there are tools to verify how well the manufactured designs match the parameters intended by the design. For once, the physical structure can be checked by creating profiles of manufactured PCBs. The time domain reflectometry shown in Chapter 7 is a second and more powerful way to verify produced hardware. This measurement allows recording the impedance progression with a precision of less than 1%. The TDR measurement shows how well the line impedance matches the requirements and localizes impedance changes with an accuracy of a few millimeters. Additionally, information about the used components can be gathered using this tool. For instance, the impedance of a data receiver can be determined very precisely.

In this thesis, the question is answered how it is possible to design interfaces that work at data rates of multiple or even tens of gigabits. The best way to do so is to put much effort into the design phase before production. The approaches made in this thesis, like impedance calculation and simulation of cross-talk effects, aim to avoid signal integrity issues already in the design phase. After manufacturing a design, there are rarely options to fix signal integrity issues. These are mainly caused by the interconnect design, which cannot be changed afterward. So, it is essential to be prudent when designing high-speed interconnects. It is necessary to use specific calculations and simulations to get the design

right. Also, creating test designs for critical components in the design and verifying them using the mentioned tools (e.g., TDR measurement) can bring significant benefits.

If there is an issue in the PCB design that significantly impacts the signal quality, this can be seen on a test board (e.g., poorly designed footprint). In such a case, a layout update can reduce signal integrity issues significantly without raising production costs.

For further investigation on this topic, several aspects need to be considered. First of all, there is the possibility of 3D EM simulations. Software packages like Cadence Microwave Office or CST Studio provide simulation setups to do 3D simulations of electrical interconnects. Such calculations are extensive and time-consuming, but they give more precise results than the more straightforward approaches used in this thesis.

Additionally, there is the topic of improved PCB materials. With special materials highly adapted for PCBs, further improvements are possible for high-speed PCB designs. Companies like Rogers Corp. are developing various laminates that perform better on high-speed PCB interconnects.

Finally, the design of a high-speed interconnect cannot be achieved by using a single tool or copying a design from an application note. It needs a broad understanding of the various effects causing signal integrity issues and a good overview of the various tools that are available and helpful for designing such systems.

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