Konstantinos Patmanidis, MSc. Aalborg University

Versatile Stress Test System for Dynamic Pulse Based Reliability Assessment of Discrete Power Devices

DOCTORAL THESIS

to achieve the university degree of
Doktor der technischen Wissenschaften
submitted to

Graz University of Technology

First Reviewer
Univ.-Prof. Dr. Annette Mütze
Electric Drives and Machines Institute, Faculty of Electrical and Information Engineering

Second Reviewer
Dr. Roberto Petrella, Associate Professor
Polytechnic Department of Engineering and Architecture, University of Udine

Graz, November 2021

AFFIDAVIT

I declare that I have authored this thesis independently, that I have not used other than the declared sources / resources, and that I have explicitly indicated all material which has been quoted either literally or by content from the sources used. The text document uploaded to TUGRAZonline is identical to the present doctoral thesis.

Graz, November 2021
Place, Date

Signature

Contents

Acronyms

ADC analog-to-digital converter

AGD active gate drive

ALC auto level control

APC active power cycling

BJT bipolar junction transistor

CGD conventional gate drive

CSGD current source gate driver

CTE coefficient of thermal expansion

DA dynamic avalanche

DAC digital-to-analog converter

DfR design for reliability

DP double pulse

DPT double pulse tester

DUT device under test

EL electronic load

EMC electromagnetic compatibility

EMI electromagnetic interference

ESR effective series resistance

FLIR forward looking infrared

GaN gallium nitride

GBP gain-bandwidth product

GS guard switch

HOST host computer

HV high voltage

HVDC high voltage direct current

I^2C inter-integrated circuit

ID inner diameter

IGBT insulated gate bipolar transistor

KAI Kompetenzzentrum Automobil- und Industrie-Elektronik

KCL Kirchhoff's current law

KVL Kirchhoff's voltage law

LDO low-dropout voltage regulator

LV low voltage

MLCC multi-layer ceramic capacitor

MOSFET metal-oxide-semiconductor field-effect transistor

μ**C** test controller

MV medium voltage

NMOS N-type metal-oxide-semiconductor

NTC negatitive temperature coefficient

OD outer diameter

PC power cycling

PCB printed circuit board

PI proportional integral

PiN positive intrinsic negative

PLC programmable logic controller

PMOS P-type metal-oxide-semiconductor

PoF physics-of-failure

PSU power supply unit

PTC passive temperature cycling

PWM pulse width modulation

RBSOA reverse-bias safe operating area

SC short circuit

Si silicon

SiC silicon carbide

SMD surface-mounted device

SOA safe operating area

SP single pulse

SPI serial peripheral interface

SPICE simulation program with integrated circuit emphasis

STO self-turn-off

TIM thermal interface material

UIS unclamped inductive switching

Abstract

The widespread employment of power electronics in many critical applications, such as automotive, aerospace, power systems and traction, in conjugation with an increasingly harsh environment, is rendering power devices the key reliability factor in terms of operation, safety as well as retention of their intended design functionality throughout their lifespan. Therefore, a thorough study of their potential failure mechanisms is of crucial importance [1].

To this end, several reliability stress test systems are being developed, aiming to emulate either real operating conditions or to focus on specific type of stress, such as power cycling (PC), double pulse (DP), short circuit (SC), unclamped inductive switching (UIS) testing, etc. These reliability tests are usually performed in an accelerated-ageing mode as well as in large quantities for a statistical analysis, provided that out of focus failure mechanisms do not dominate. Nevertheless, a considerable construction effort is needed, since numerous device under tests (DUTs) operated in a parallel mode as well as a sophisticated data acquisition unit, for an accurate post failure analysis, is required.

The primary objective of this thesis is to implement a reliability stress system for discrete high voltage power semiconductors under dynamic pulse testing, such as DP, SC and UIS in accelerated mode. The system's novelty firstly lies in its modularity to perform the case study stress tests, under certain limitations, with a primary focus on DP testing, and secondly in its scalability allowing to rapidly expand it in a multi-channel system. This should be accomplished in a feasible manner in terms of cost, hands-on effort and time to get the final reliability data. Most of the power components should be a fixed part and merely the DUT should be changed for a variety of power devices and stress patterns. Finally, its redundancy is of paramount importance not only in terms of reducing the energy dissipation through a failed DUT, but also to maintain uninterrupted parallel operation for a multi-channel system [2].

In the beginning, several simulation concepts are examined based on the fundamental introduced topology and their benefits and drawbacks are underlined. The next part presents the various hardware prototypes and their sub-objectives toward the fulfilment of the main goal. Several experiments are conducted revealing all the critical performance indicators of the system. Separate chapters are devoted to the magnetics design and the configurable gate driver. The latter is a completely software programmed gate driver offering the possibility to define the gate drive conditions via software.

Acknowledgements

First of all, I would like to greatly say thanks both of my supervisors, the academic one, Mrs. Annette Muetze, and the industrial one, Mr. Michael Glavanovics, for this research opportunity, their support and contribution to the final outcome of this thesis. All the KAI employees, who practically support this project such as, Markus Sievers, Benjamin Steinwender, Sascha Einspieler and Roland Sleik. I cannot forget both students, Tobias Kist and Angelos Georgakas, without their support and contribution the progress of this research would not be remarkable. The determining contribution of the PCB designer, Valentin Nita, in the project completion. Finally, my deep gratitude to people who actually support me psychologically till the end of this project.

This work was funded by the Austrian Research Promotion Agency (FFG, Project No. 884573)

Konstantinos Patmanidis
Graz, 2021

Chapter 1

Introduction

1.1 Motivation

Reliability physics of power electronic components is increasingly becoming a critical research field, especially for newly developed applications due to a constant increase of new requirements. Some of these requirements include higher power density demand, introduction of emerging applications under harsh environments imposing higher package temperatures, new mission profiles for critical applications (e.g. aerospace, automotives, railyway traction, etc.), stricter level failure rates in future products as well as reliability performance challenges for emerging materials (e.g. silicon carbide (SiC) , gallium nitride (GaN) and package technologies [3], [4]. Despite all opposition, the end goal is to predict the reliability, and therefore to achieve cost reduction and enhanced performance for a predefined lifespan of power electronic products.

In order to address such a complex research field, reliability engineering techniques are employed and should be applied in order of priority for cost minimisation and reliable product generation, as analysed in [5]. During the design stage, reliability engineering includes physics-of-failure (PoF), a methodology based on root cause failure mechanisms under given environmental conditions and stressor types and design for reliability (DfR) on a system level [4], [6]. During the operation stage, the reliability can be improved by condition monitoring and active control strategies, as explained in [4], [7]. These techniques are being constantly evolved meaning that in the short term improved power electronic products and systems will be expected.

The root cause of failures of power electronic components is therefore of paramount importance and should be thoroughly studied. To this end, power electronics component manufacturers and their customers start building various reliability stress test setups not only for qualification reasons established by standards, such as JEDEC or AEC, but also on a device and application level for an overall reliability understanding. Such reliability stress test systems constitute a reliability study tool where the PoF or DfR techniques can be applied leading to advanced power electronic components' development.

1.2 Research Scope

In this section, the general concept of the proposed stress test system along with its theoretical design criteria is introduced. Several dynamic stress test methods and the possibility to incorporate them within a unified apparatus by merely changing the most critical parts, e.g. DUT board, etc, without violating the design criteria are initially considered.

In general, reliability stress tests are classified into two main categories, focusing either on device (device-specific test) or the device within its application environment (application-specific test). However, there is another category where the DUT is stressed at the exact application environment, called field-application test. Subcategories of these are determined by the stress level, which can fall into a destructive or a non-destructive test, as explained in [3, 8, 9]. For example, end-of-life tests examine the time to failure, while non-destructive tests examine the ability to pass a predefined stress level after certain number of cycles, as defined in standards. It is worth mentioning that the application-specific test differs from the field conditions, since an extra circuitry is added in order to acquire various online monitoring parameters, altering the topology as well as protection against catastrophic failures.

In this case study, a variety of discrete high voltage power semiconductors and different stress test types are of main interest, such as PC, DP or single pulse (SP), UIS and SC, as shown in Figure 1.1, where the power devices should be evaluated regarding their reliability and robustness. Thus far, most of the traditional qualification standards, developed over the last years, do not usually include hard switching stress test conditions, limiting the significance of test results in terms of application relevance. Nevertheless, a JEDEC standard points out the necessity of a test vehicle with reduced complexity of its actual setup, since the application system may also mask the intrinsic failure mechanisms [10]. The most widespread switching test setup is the double pulse tester due to its simplicity, hence avoiding system related failures from other components [10]. Additionally, it is energy efficient due to lower power handling requirements and preferable especially for a multi-channel stress test bench. Therefore, a design reference is established based on a double pulse setup.

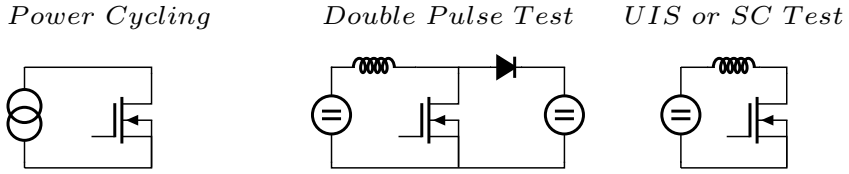


Figure 1.1: Different type of stress tests.

For a meaningful statistical analysis, a multi-channel stress test bench also needs to be constructed. An initial outline of such a multi-channel bench is depicted in Figure 1.2. As can be seen, the system consists of several parts, such as the host computer (HOST), the low voltage (LV) power supply, the backplane board, the stress board, the high voltage (HV) and the medium voltage (MV) power supplies. Within each backplane board, several stress boards are located, featuring certain design criteria. One of these is the modularity, which enables the possibility to perform different stress tests in a configurable way as well as to set them up at faster pace. Therefore, some parts are exchangeable, such as the DUT board, the load board (inductor), and probably the test controller (μC) board. On the other hand, the protection switch, also called guard switch (GS), is a fixed part of the stress board. Another design criterion is the scalability, namely a hardware implementation that easily handles and supports a large number of stress boards. Last but not least, redundancy plays a significant role, since destructive tests can result in a DUT failure. After such an event, the failed DUT should be immediately disconnected by the GS turn-off so that nearby stress boards can continue their operation without being interrupted.

Concerning the HOST, its purpose is to communicate with the local μC of each stress board and to collect in-situ data from the condition monitoring circuitry of the DUT for a subsequent post failure analysis (e.g. on-state voltage, junction temperature estimation, load current, etc). It should also have access to the power supplies for setting the dc voltage and current level of the stress test conditions

under study. This is realized through an Ethernet communication, as shown in Figure 1.2.

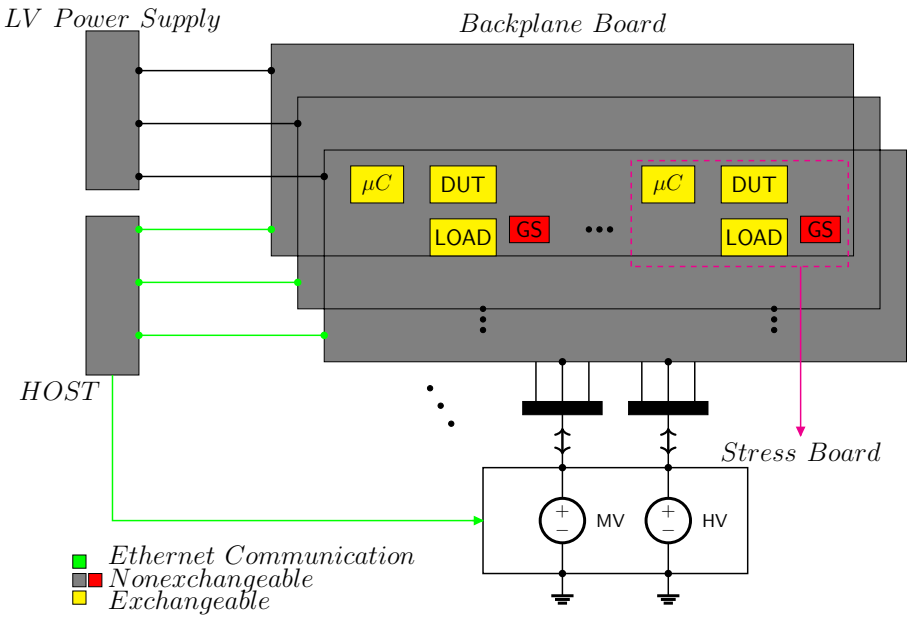


Figure 1.2: Stress test system architecture.

Even though the DUT energy losses are relatively low, an effective cooling interface is still required. From stress test point of view, it is also necessary to adjust the DUT case temperature in order to emulate different ambient conditions for worst case scenarios or accelerated wear-out purposes. One approach is to place the whole system inside a climate chamber with the penalty of heating-up all the system, and, as a result it is possibly to influence its performance and reliability. Alternatively, an active cooling interface dedicated to the DUT can be placed where the case temperature can be adjusted, hence avoiding temperature swings within the whole system.

In a nutshell, this thesis casts light on a stress test setup development serving as a reliability study tool for discrete high voltage power semiconductors. The possibility of applying the aforementioned stress tests is examined and the associated limiting factors are highlighted.

1.3 Stress Test Requirements

It should be stressed that this thesis is realized in collaboration with a research institute, named Kompetenzzentrum Automobil- und Industrie-Elektronik (KAI), located in Villach, Austria, working on modular stress test concepts, which are particularly elaborated in [9]. As a result, existing features from previous projects, implemented at KAI and explained in [9, 11, 12, 13], are partly or completely utilized by this project. This includes the modular architecture concept, the communication between the HOST and the μC board as well as certain subcircuits for condition monitoring. Furthermore, the stress test requirements stem from the research institute's experience and its industrial activity.

Consequently, this project aims to fulfil certain practical requirements, apart from the general research scope, as explained previously. One of these requirements is to investigate the possibility to stress devices up to 1.7 kV peak voltage, across the DUT, and peak current up to 400 A depending on the DUT. Additionally, gate voltages up to 24 V and down to -15 V should be programmable via the μC, as required for different DUTs. Another crucial topic is to study the possibility of setting the gate

drive conditions of the DUT via software without manual intervention by soldering external resistors. Lastly, the stress board should be kept within specific limits in order to fit within an 19 inches rack system, thus complexity and space should be also considered.

1.4 Achievements

In the context of this thesis, two master theses were realized to assist in the the hardware development as titled below:

1. Design of an Intelligent Current Controlled Gate Driver for Flexible Stress Testing of Discrete High Power Semiconductors [14].
2. Development and Evaluation of a Reliability Stress Test System [15].

During the former thesis, Tobias Kist implemented the hardware of the first prototype including a current source gate driver (CSGD) as well. In the latter case, Angelos Georgakas developed a backplane board accommodating up to four stress boards. Furthermore, the stress board was designed with the invaluable assistance of a layout designer. The author contributed to the design phase in both projects.

1.4.1 Author's Contribution

Three scientific papers were published by the author as titled below:

1. Modular Dynamic Pulse Stress Test System for Discrete High Power Semiconductors [1].
2. Configurable Gate Driver for a Stress Test Bench of Newly Developed Discrete Silicon Power Devices [16].
3. Scalable Multitasking Dynamic Pulse Based Reliability Stress Test for High Voltage Discrete Semiconductors [2].

The scientific analysis and methodologies are part of the author's contribution. In particular, this includes circuit design, analysis and improvement, concept development, design of magnetics and DUT boards.

1.5 Thesis Outline

This thesis is classified into seven chapters. The introductory chapter formulates the research objectives, as already shown. The second chapter presents already existing setups on the field of reliability stress systems as well as the different failure phenomena that can be studied with the proposed stress test setup, as found in literature.

Chapter 3 introduces the new flexible circuit concept of the stress test system and the modular way to execute the different stress tests. The pros and cons of each configuration as well as the emerging hardware trade-offs are pointed out. Moreover, computer-aided simulation tools, such as PLECS® and SPICE are employed for an improved comprehension. Chapter 4 discusses the hardware prototypes constructed through the course of this thesis and their purpose to the final goal. Different experiment examples and design decisions are elaborated.

In chapter 5 the load interface realization and the different inductor design options, which were considered through this thesis, are shown. Chapter 6 analyzes the configurable gate driver, developed based on an open loop current source approach. Its limitations and possibilities are recorded based on various experiments and simulation tests for different DUTs.

Finally, chapter 7 discusses potential new features and incomplete topics of this project together with a summary of the research outcome.

Chapter 2

Background

2.1 Introduction

Lifetime models of power electronic devices are an essential part of the reliability engineering. In order to predict their lifetime, several techniques are combined, such as numerical solutions, the Coffin-Manson technique, handbook based failure rate models and experimental accelerated tests for validation [4]. Therefore, reliability stress test systems are being developed for increasing the statistical significance. This chapter presents a short overview of some of the currently published stress test benches in conjugation with the particular failure mechanisms under study. It is also worth mentioning that stress tests must be carefully applied so as to avoid any unintended failure mechanism excitation.

As the content of this thesis deals with the development of a reliability stress test system, dedicated to study the long-term aging mechanisms, mostly intrinsic failure phenomena of power electronic devices are of main concern. Even though extrinsic causes inadvertently contribute to the final outcome, they are not discussed. The intrinsic failure mechanisms are the result of a prolonged exposure to certain stressors, such as temperature gradients, voltage, humidity, or pollution [4], leading to the final wear-out of the devices. Then depending on the stress test type, which can be a robustness or accelerated-ageing test, different failure modes are finally manifested. Therefore, the second part is devoted to briefly show some of the potential failure phenomena that could be studied by the proposed reliability stress test setup for different power semiconductors, as found in literature.

2.2 State-of-the-Art

2.2.1 Power Cycling Stress Test Setups

Generally speaking, PC testing is classified into active power cycling (APC) and passive temperature cycling (PTC), as denoted in [4, 17]. Particularity, the APC methods also split into the conventional method, by applying a pulsating dc current, and methods emulating realistic operating conditions. It should be noted that PTC can introduce significant test errors, since self-accelerating mechanisms are not triggered, as explained in [18].

Based on the prior state-of-the-art, it is evident that most of the projects focus on APC. The opposition method was initially employed in [19] as an APC technique for emulating realistic operating conditions, since the DUT operates under pulse width modulation (PWM) scheme. Advanced results of this method for insulated gate bipolar transistor (IGBT) modules are presented in [20], in which the

stressing conditions can be easily adjusted, e.g. through the switching frequency. Another advantage of this method is that the overall system losses are retained low enabling the possibility to carefully increase the stress level. The aging indicators are the on-state voltage and the indirect junction temperature measurement.

An advanced accelerating PC test for three phase applications, emulating field conditions, is presented in [21, 22, 23]. Various stressing conditions can be applied by adjusting the output frequency, the modulation index, the switching frequency, the output current and voltage as well as the power factor. This stress test setup also incorporates in-situ on-state measurements for detection of associated failure modes, e.g. bond wire lift-off. A considerable increase of the on-state voltage, as a result of the bond wire lift-off, can be detected and can be set as a failure criterion. Finally, the junction temperature is estimated in-situ by employing the I-V characteristics of the DUT.

A PC ageing test bench dedicated to photovoltaic applications has been published in [24]. The authors highlight the importance of relevant mission profiles, since accelerated tests might introduce not relevant degradation mechanisms compared with the actual field conditions. Based on photovoltaic data from the field, namely rms output current and ambient temperature, they estimate the losses by characterizing the DUTs. Subsequently, they identify the thermal model via the intrinsic body diode of the DUT and based on that they estimate the junction temperature. This test bench combines passive and active cycling so as to emulate the ambient conditions as well. Finally, they perform intermediate stops for re-characterization of the DUT and monitor several aging indicators, such as the leakage currents, threshold voltages and input-output capacitances.

In the case study of [25], a PC test apparatus has been implemented for high power IGBT modules based on dc pulse current injection (conventional method). This stress system is able to stress up to 10 samples. Different on-state voltage measurements are shown in conjugation with the validation method. The benefits of such an approach include less noise in measurements, absence of overvoltages and high dc-link voltage.

An APC test bench for SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) is introduced in [18]. The DUT operates in linear mode by regulating the drain-source voltage whilst a dc current is injected through the channel, in contrast to the method presenting in [23] where the source current is controlled. However, it should be noted that such methods might cause instability due to thermal runaway [26, 27] and should be cautiously applied as stressed by the authors as well. Furthermore, the stress test conditions should be carefully selected, as pointed out, since numerous different failure modes appear and each of them is associated with several stressors. Some of the most frequent failure modes encountered by encapsulated power semiconductors are bond wire lift-off, bond wire heel-cracking, brittle cracking, gate oxide time dependent breakdown, etc. Finally, they present how to select ageing indicators for end-of-life criteria based on economical constraints, as a large scale testing is necessary.

2.2.2 Double Pulse Tester Setups

The most widespread setup for power electronic devices' switching characterization is the double pulse tester (DPT). Such a setup is necessary in order to record the dynamic transient behavior of the devices under various conditions, such as dc-link voltage, switching current, gate and ambient conditions. Efficiency and electromagnetic interference (EMI) performance is of great importance for almost every application, meaning that such test becomes a valuable tool for power electronic systems design [28].

In [29], an automated DPT for testing devices up to 1000 V, 60 A and 250 °C, also consuming less space, is introduced. The setup is composed of different modules for increased flexibility. Instead of

using a high voltage power supply, they employ an ac/dc converter, connected into a power outlet, and subsequently by another dc/dc converter to scale the dc-link voltage according to the test conditions. Logic circuitries are employed in a closed loop configuration which in turn automatically decide the pulse duration. The feedback signals are captured via oscilloscope probes and the settings are given via a graphic user interface. Similar automated DPT with different heating method is proposed in [30] for TO-247 power devices. On the contrary, this automated test uses a power supply unit (PSU) and focuses more on the importance of the parasitic loop inductance.

DPT focusing on the characterization of SiC devices and their challenges are presented in [28, 31]. Special attention is paid to the parasitics of the printed circuit board (PCB) and the proper probe selection, since these types of devices show high dv/dt and di/dt transient behavior. Equivalently, DPTs for GaN devices are analyzed in [32, 33]. GaN devices exhibit dynamic on-state resistance, owing to trapping phenomena as described, which need to be measured for further investigations, and for that reason, different measurement methods are proposed by the authors. Additionally, these devices also require the implementation of special PCB layout due to their superior properties.

From stress testing point of view, the DPT is getting more attention not only for wide bandgap devices as shown in [10, 34, 35], but also for silicon (Si) devices, since different failure modes related to hard switching events can occur, as will be shown shortly. The necessity for a test vehicle able to perform repetitive hard switching tests is also pointed out by a JEDEC standard for GaN devices [36].

2.2.3 Short Circuit Stress Test Topologies

SC ruggedness is of crucial importance for power electronic devices, e.g. in motor applications [37], and their ability to safely turn off such events under different ambient conditions. There are three different SC types that a power device can experience, as reported in [3, 38]. In brief, these are classified into SC type I, when a device directly turns on into a SC condition, SC type II, when a device experiences a SC event during the on-state phase, and SC type III, which occurs across the load the moment of freewheeling diode conduction. Therefore, meticulous study of such detrimental events should be examined in terms of robustness and reliability.

Several setups are realized to achieve this and a few examples are given here. In [38], a simple setup has been realized to test discrete IGBTs under different SC type events and different case temperatures through a hotplate where the dominant failure modes are presented. In [39], the SC robustness of high power IGBT modules is investigated, where special care on the design of low stray inductance busbars is shown. The short circuit characteristics of SiC and how they are influenced by different case temperatures are analyzed in [40], using a similar setup as the previous study.

2.2.4 Avalanche Stress Test Topologies

Avalanche robustness of power electronic devices plays a significant role, since several industrial applications can experience such events while some other applications, e.g. automotive, are designed to withstand this phenomenon in a repetitive mode during their operational life [41, 42]. Especially large parasitic loop inductances can provide sufficient energy to the device during inductive switching which can cause the device to enter in avalanche mode [43]. Therefore, single pulse and repetitive avalanche ruggedness should be studied on the design stage of the power devices, which is becoming even more critical for emerging devices because their reliability is still to be proven in the development process.

The conventional UIS circuit for single pulse avalanche is described in [44]. However, several laboratories and research institutes follow different approaches. In [42], an extra fast switch together

with a freewheeling diode is employed so as to define the avalanche energy by excluding the effect of input power supply voltage. This test bench studies 1.2 kV SiC MOSFETs under single pulse or repetitive avalanche mode. The overall execution process is highly automated where different inductors and case temperatures can be selected. Ageing indicators, such as threshold voltage, drain leakage current, on-state resistance and gate-source leakage current are measured when the device is cooled down after certain thousand cycles. One of the downsides of this setup is the inability to adjust the gate resistance and the turn-off gate voltage. Finally, the authors present several methodologies for ageing mechanism comprehension.

In [45], an auxiliary 3 kV IGBT is connected in parallel to the DUT in order to avoid the self-heating during the current increase through the inductor, as it happens in the conventional setup. The DUT is a SiC MOSFET with voltage rating of 1.2 kV and current rating of 42 A. A programmable pulse generator is used for setting the pulse width for the different study scenarios. Single pulse and repetitive tests are conducted, in which ten seconds off-period is set for proper cool down.

Another avalanche stress test bench focusing on SiC MOSFETs is shown in [46]. In this research only single pulse events are carried out in order to estimate the avalanche energy that the DUT can sustain before failing. A series high voltage IGBT (3 kV) and a limiting current resistor are connected to the DUT. The adjustable parameters are the dc voltage and the pulse duration of the IGBT. Consequently, the avalanche current or the avalanche duration is controlled, as explained.

The last example shows a study for automotive applications where Si MOSFETs are used [41]. In this stress test bench many devices can be stressed under repetitive avalanche in parallel mode. Various inductors from 2 µH to 100 mH can be selected and the peak current can be set up to 250 A. The DUTs are placed within a climate chamber in which the temperature can be regulated from $-40\,^{\circ}\mathrm{C}$ to $150\,^{\circ}\mathrm{C}$. The statistical significance is improved, since many DUTs are simultaneously stressed, as highlighted.

2.3 Failure Phenomena under Study

2.3.1 Avalanche Breakdown

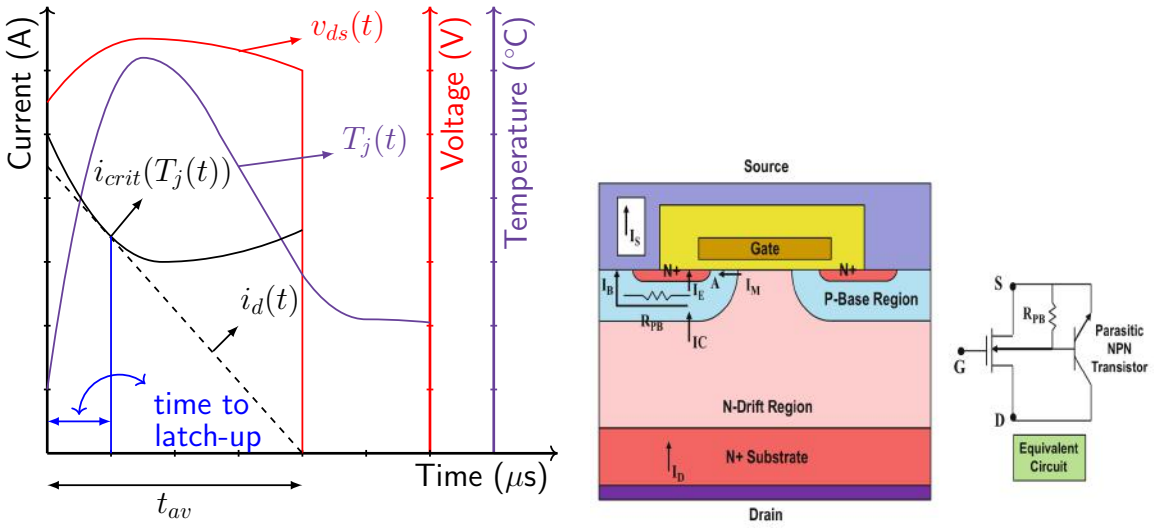
The avalanche mode is activated when high electric fields are induced inside the power semiconductor's structure in excess of a critical electric field. This high electric field in turn causes free carriers to accelerate and receive sufficient energy so that electron-hole pairs are released via impact ionization. This phenomenon can lead to an uncontrollable situation and subsequently to catastrophic failure. It should be pointed out that single pulse avalanche failure mechanisms are mainly latch-up and thermal runaway, while the dominant repetitive avalanche ageing mechanism is related to hot carriers trapping into the gate oxide [42, 47]. This causes a cumulative damage and can be observed by monitoring representative ageing indicators, because they drift over the stressing period, as stated previously.

Latch-up

The catastrophic failure through the latch-up event can be described based on the graph shown in Figure 2.1. Within a MOSFET structure, a parasitic bipolar junction transistor (BJT) is formed between certain p- and n-doped regions. When the avalanche current starts flowing through the device and combined with the high electric field, it can create high current densities along the base of the parasitic BJT structure and possibly cause its activation. In this case an uncontrollable situation is developed leading to final destruction. The parasitic BJT activation is described by a critical current as given in Equation (2.1). The level of this critical current shows the minimum instantaneous required current for the activation. As the temperature rapidly increases the critical current decreases, because

the base resistance substantially increases, making the device more vulnerable to latch-up especially at the beginning of the avalanche pulse [48]. It is also worth noting that different technologies have their own structural features, for example high voltage power devices which can significantly affect their latch-up robustness [49, 50].

$$i_{crit}(T_j(t)) = \frac{V_{BE}(T_j(t))}{R_{PB}(T_j(t))} \tag{2.1}$$



(a) (b)

Figure 2.1: (a) Latch-up due to critical current, (b) parasitic bipolar transistor in a power MOSFET [51].

Thermal runaway

A more commonly experienced catastrophic failure is the thermal runaway due to high energy avalanche pulses. Under these conditions the junction temperature of the device approaches the intrinsic temperature of the semiconductor material which eventually leads the device to losing its properties [48]. The carrier density is dominated by thermal generation, and thus the temperature increase has a positive feedback effect, and, as a result the device is driven to destruction. However, it should be highlighted that the associated mechanism is quite important, since for example SC events can also lead to high temperatures without failure [3].

2.3.2 Short Circuit Testing

SC events constitute an extreme operating condition for the power electronic devices, because concurrently high voltage and current are present, resulting in high power dissipation and temperature gradients. The most frequently appearing failure modes of discrete power devices up to 1.2 kV are analyzed in [52, 53, 54, 55] and reproduced in Figure 2.2. There are four distinctive points where a catastrophic failure can occur as listed below:

(α) This failure mode might happen when a high dc-link voltage is present and is probably a power limited fail.

(β) This failure mode occurs when high energy is dissipated through the device causing the junction temperature to reach its intrinsic value and finally thermal runaway occurs.

(γ) This destruction occurrence is experienced during SC turn-off and resembles a dynamic latch-up.

(δ) This mode happens several microseconds after a successful turn-off attributed to device's leakage current. A positive feedback phenomenon develops inside the device leading to thermal runaway.

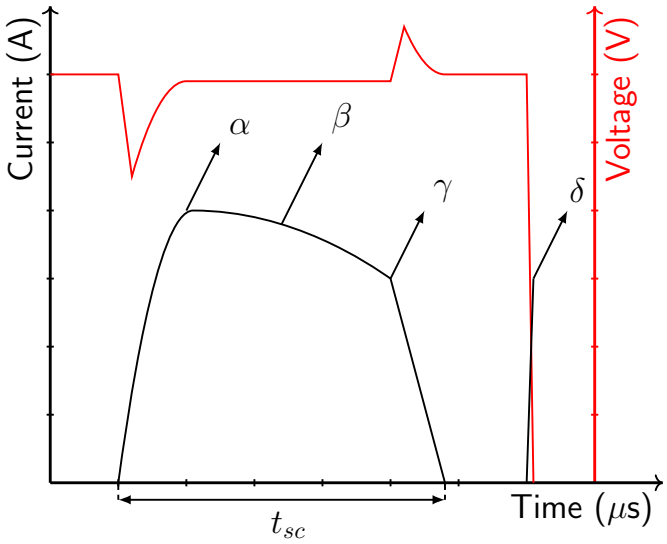


Figure 2.2: Different locations of the SC failure modes.

Every device presents a critical energy level (E_c), which distinguishes the failure modes appearing from β to δ. This critical energy depends on the ambient conditions, the dc-link voltage, the SC duration and the SC current level. When the applied energy is well above the critical energy the failure mode β is manifested. On the other hand, when the energy is below the critical energy, the failure mode γ occurs. The latter case allows the device to handle more than one SC events acting as accumulated damage leading to the final failure. In case of failure mode δ, the applied energy is close to the critical energy and the device fails, after the first pulse with a delayed failure mechanism. It is also worth mentioning that IGBTs with higher voltage rating, e.g. above 3.3 kV, present different trends in regard to their SC robustness which can vary under different dc-link voltages [3, 56].

2.3.3 Double Pulse Testing

As technology advances, a lot of applications require not only increased power density due to miniaturization and compact design, but also increased product reliability [6]. To keep up pace with this demand, extensive research is being conducted in the field of emerging devices as well as structural improvements to existing Si devices [57, 58]. However, these technological improvements might trigger different failure mechanisms that need to be thoroughly investigated and explained.

Newly developed IGBT devices can achieve superior balance between switching losses and on-state voltage drop, and thus enhanced power density [57]. It has also been proven that high current

and voltage gradients can result in dynamic avalanche (DA) during commutation and a potential long-term drift in their switching behavior [59, 60, 61]. In addition, the DA phenomenon causes current filamentations and eventual destruction, as analysed in [62]. In [63], a comparison between two different IGBT structures and their impact on both on and off long-term switching behaviour under DA is presented, highlighting the importance of repetitive pulse testing. Finally, a study in [35] evaluates the reliability of 1.2 kV-rated positive intrinsic negative (PiN) vertical GaN diodes under hard switching conditions through DP testing, in which trapping mechanisms lead to wear-out.

2.3.4 Power Cycling Testing

The main goal of the APC is to study the thermo-mechanical effects between the interconnected materials within the power electronic packages. Every interface material presents its own coefficient of thermal expansion (CTE) and due to repetitive PC, thermo-mechanical stresses are induced by contraction and expansion of the attached substrates, leading to their wear-out. In particular, in APC tests the heating source is the semiconductor die itself, and therefore interconnections in the vicinity of the die are mostly stressed, such as bond wires and solder joints. The most frequently manifested failure mechanisms are solder cracks, bond wire lift-off and bond wire heel-cracking [4]. It is also worth mentioning that at high temperatures (e.g. above 125 °C) different failure mechanisms can occur, for example, the increased degradation pace of encapsulation materials [4]. Last but not least, a study in [64] shows that in SiC MOSFETs a die related degradation mechanism dominates over the bond wire lift-off due to threshold voltage shift, pointing out that emerging devices can exhibit non-standard failures.

To model such effects several empirical models have been developed over the years utilizing Coffin-Manson and Arrhenius models. Modified models have also been created by taking into account other effects, such as the heating time, the bond wire effects, or the voltage class [4]. In [65], it is stated that short heating pulses stress the die itself and the nearby connections, while longer heating pulses allow the development of creep or reconstruction to occur, highlighting the impact of the heating time. However, the nature of the empirical models is statical, meaning that they are inadequate to describe the actual deformation mechanisms under complex thermal loadings and sometimes lead to doubtful extrapolation results. To overcome this, physics-based models are being developed, giving better understanding of the actual ageing mechanisms, and thus gaining additional ground [4].

Chapter 3

Stress Test Concepts

3.1 Introduction

As has been previously pointed out, this project examines the feasibility of performing different stress tests within a unified stress test bench with the prospect of being scaled. By considering this goal, this chapter introduces the fundamental circuit architecture of the stress board and the modular way to perform the case study reliability tests, as introduced in Figure 1.2. Subsequently, based on this topology, different stress test concepts are evaluated in terms of performance and practical realization effort. It should be also stressed that the final outcome of this chapter is closely related to the development of the hardware prototypes.

In order to illustratively indicate the location of the case study stress test types within the safe operating area (SOA) of a typical power device, an area graph is portrayed in Figure 3.1. It is noteworthy that certain type of tests are performed outside the SOA with the view to examine the ability of the devices to withstand such temporary or constantly applied events. For example, there is a stress type called in literature ”switching cycle”, applied especially in SiC MOSFET devices in order to assess their robustness outside their SOA by examining potential new failure mechanisms, as shown in [66, 67]. This type of test is essentially a SP test but a DP test could be examined as well.

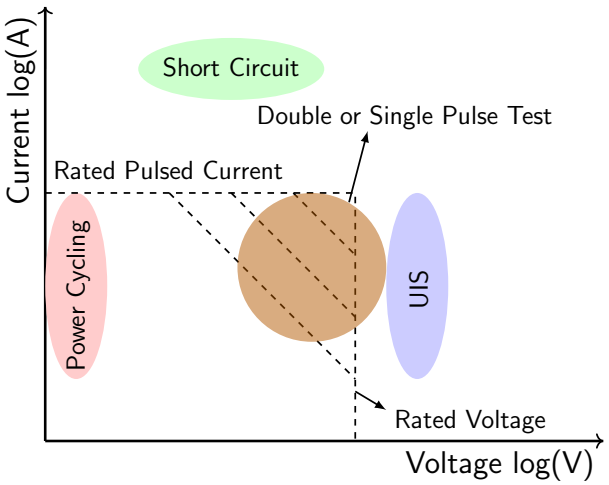


Figure 3.1: Case study stress test types related to SOA of a typical power device.

The simulation analysis largely focuses on the DP and PC testing by examining alternative concepts with the use of the PLECS® tool. Since the SP is a subcategory of the DP test, it is not covered. The stress tests locating outside the SOA, namely SC and UIS, are studied with the assistance of the SPICE simulation tool.

3.2 Stress Board Block Diagram

The fundamental element of this stress test system is the stress board. The generic block diagram as developed in its final form is illustrated in Figure 3.2. It is composed of a full bridge, and capacitor banks both at input and output (C_{in} and C_{out}). The left branch of the full bridge consists of two parallel connected protection switches, named GS, and their freewheeling diode (D_1) whereas on the right-hand side of the bridge is the DUT board, holding the DUT and its clamping diode (D_2). Additionally, there is a Hall-based current transducer, in between the transducer and the DUT board a configurable load (inductor) board can be also connected. This setup offers the flexibility to exchange different DUT boards, loads and power connectors so that different stress tests can be modularly configured.

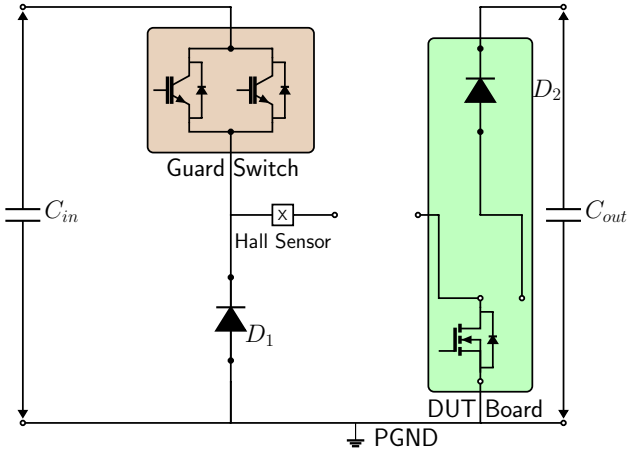


Figure 3.2: Dynamic pulse stress test system block diagram.

3.2.1 Modularity of the Introduced Concept

Figure 3.3 demonstrates how the stress board can be configured in various ways so that the case study stress tests can be realized. It is obvious that this introduces several trade-offs in terms of their effective application, as will be discussed.

The most distinctive stress test of this project is the DP test, which can be realized in two different ways. One way is to bridge the output to the input side for the standard DP setup (Figure 3.3a). Another way is to connect the HV rail at the output and the MV at the input and to perform a discontinuous PWM boost operation (Figure 3.3b). One of the main objectives of the DP stress test is to apply high electric fields during the hard switching events, accomplished by introducing the HV rail.

As far as the PC is concerned, the attention is toward the conventional method with a dc pulsed current. Therefore, the input supply should provide sufficient current in order to meet the stress conditions. Furthermore, in this case the load is substituted with a jumper cable or board that just bridges the two ends (Figure 3.3c).

Another stress test category includes the UIS in which the DUT is exposed to repetitive avalanche events. As can be seen in Figure 3.3d the clamping diode D_2 is not employed and thus the load's energy is dissipated through the DUT. The UIS test can be executed in two different ways. The simplest one is just to ramp up the current through the inductor and then turn off the DUT. However, when the breakdown voltage of the DUT is close to the supply voltage, then the use of the GS and lower freewheeling diode D_1 is advantageous.

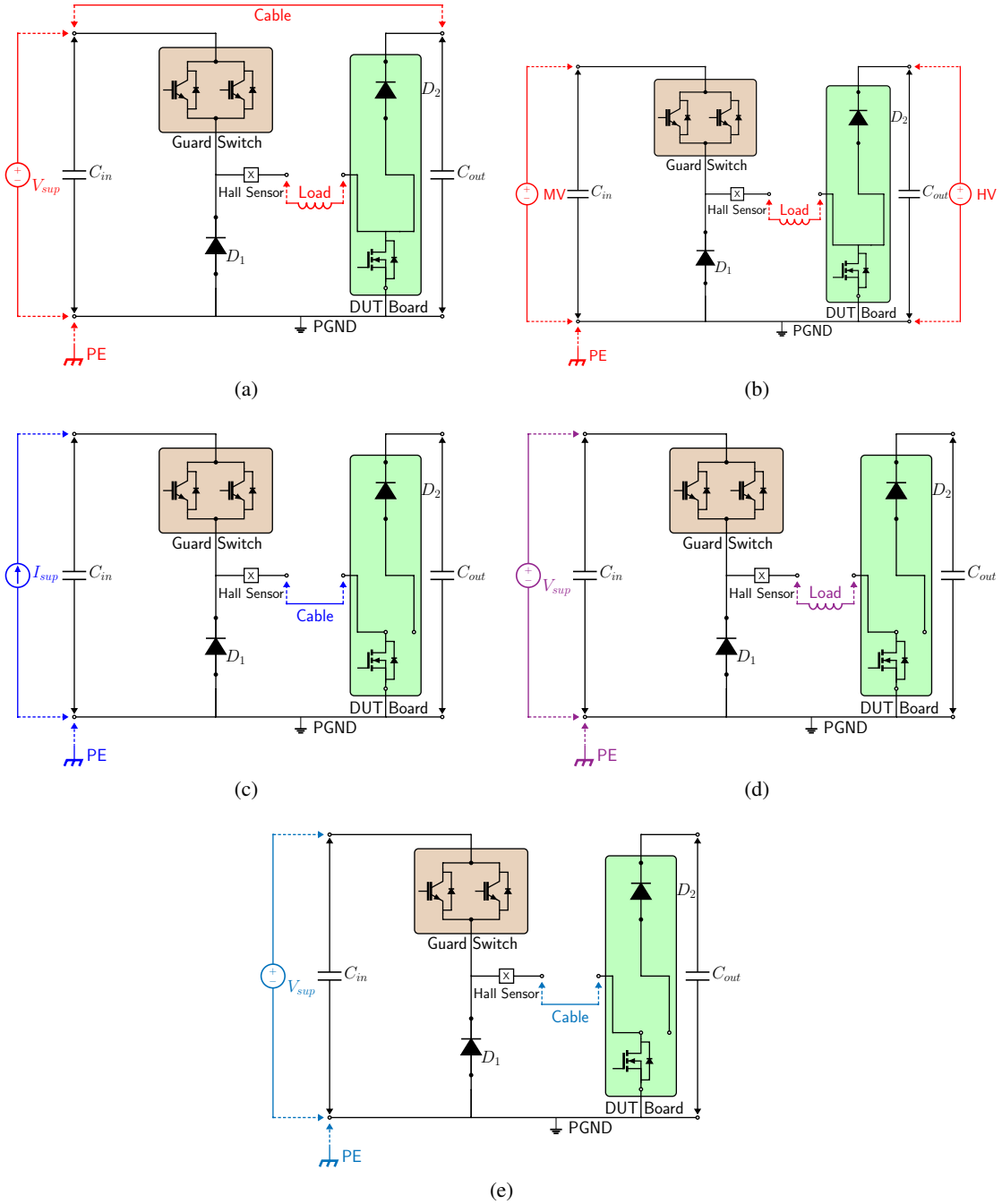


Figure 3.3: Block diagrams of the configured stress tests: (a) standard DP test, (b) discontinuous DP boost test, (c) PC test, (d) UIS test, (e) and SC type I test.

Finally, this setup allows to perform SC type I where the load is exchanged with a short cable as that for the PC. As will be shown later this particular test poses a limit to the minimum achievable loop inductance.

3.2.2 Protection Scheme

One crucial requirement of such a system is to guard itself in case of destructive stress testing or unexpected DUT failure. Consequently, a fast reacting protection circuit is required not only to reduce the energy dissipation through a failed DUT for a post failure analysis, but also to maintain uninterrupted parallel operation for a multi-channel system. This is accomplished by introducing the left branch of the full bridge to the stress board as its main protective circuit. The feedback signal of the Hall sensor is employed to turn off the GS, as will be explained in chapter 4. However, this branch can also be actively utilized to execute certain tests, in the view of achieving specific objectives, e.g. performing tests in a faster repetition mode.

3.3 Concept Simulation

3.3.1 Power Cycling

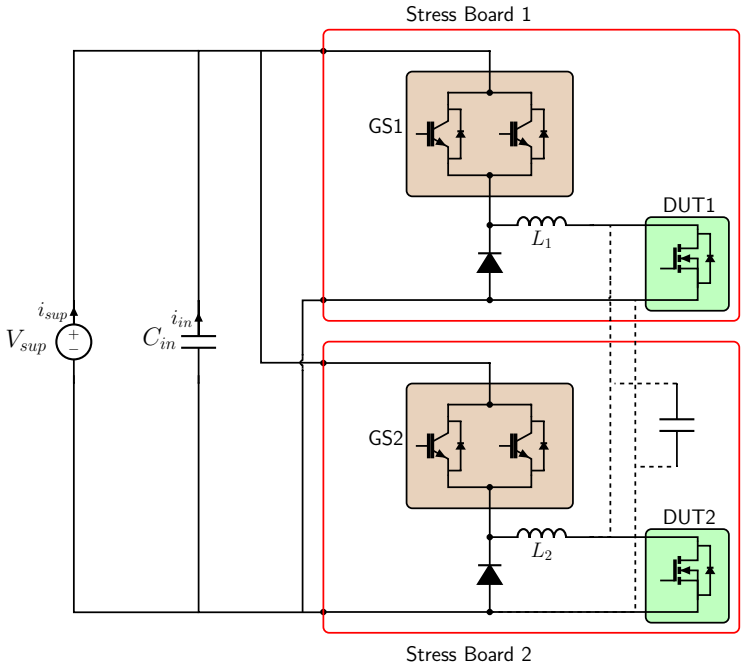


Figure 3.4: APC concept by employing the left half bridge, single phase buck converter (solid line), two phase buck converter (dashed line).

As already mentioned, the APC splits into two categories, from which the conventional method is only considered in this research. The objective of the PC is to study the ageing mechanisms of the power devices packages due to the thermo-mechanical stresses. The development of a multi-channel stress test system for this particular type of test requires a dedicated PSU capable of providing high

currents at low voltages. On the other hand, the other types of tests are related to constant voltage PSU, in which high voltages are necessary and anticipated on the dc-link to occur. In the market, it is quite difficult to find a single PSU that can accomplish such a complex mission profile. Furthermore, the use of two different PSUs could be an option, however it imposes constraints in terms of cost and preparation.

Additionally, the industrial requirements for this particular test are not strictly defined offering the flexibility to investigate alternative concepts. It should be also noted that the stressing profile is of paramount importance, since the final result is highly affected. For example, [68] highlights the importance of temperature swing duration for the final number of cycles required to reach the end-of-life criterion, focusing on intelligent IGBT power modules. Another study in [69], focusing on IGBT power modules, indicates that short load durations are more representative for die and bond wires related failure mechanisms, however, longer pulse durations are appropriate for failure mechanisms related to creep or reconstruction of metal layers and solder interfaces. Hence, the actual mission profile is of paramount importance and especially for discrete packages several discrepancies versus modules are expected mainly due to their size and structure.

By taking into consideration these facts, this section discusses a concept with voltage-based PSU, in which the left half bridge of the stress board can be actively utilized. The degradation of the reliability stress test system is highly significant fact for its long-term functionality, since it has to sustain loads with less degradation than the DUT itself. Figure 3.4 shows the proposed concept where the left half bridge functions as a buck converter by regulating the injected current to the DUT. The dashed lines indicate the possibility of connecting two stress boards and a filter to remove high frequency noise, and thus forming an interleaved topology for improved reliability. Another option is to place two DUTs in series within one DUT board or to connect two DUT boards in series separately.

Interleaved topologies bring about certain benefits, such as current ripple reduction both at input and output leading to less frequency harmonic content, reduction of energy losses, both conduction and switching losses on the GS and its freewheeling diode since the current decreases to half, the inductor losses are reduced as well, the sufficiency of filters with less attenuation capability and the possibility to avoid potential hotspots on the PCB boards [70].

Besides the benefits, it should be emphasized that this concept can be applied in fast PC stressing scenarios, meaning that the PC period (T_{PC}) has to be relatively low as well as the duty cycle. The inability of the voltage-based PSU to provide high currents in conjugation with the limited input capacitor bank can pose an upper limit.

The following subsections discuss simulation examples by using some parameters related to the subsequent hardware prototypes. Table 3.1 lists the simulation parameters of the PLECS® model.

Table 3.1: PC Simulation Parameters

$I_{sup,max}$	30 A	Switching frequency	40 kHz
Capacitor bank	800 µF	Ambient temperature	25 °C
L_1,L_2	50 µH	ΔT	75 K
DUT	MOSFET	D_{PC}	0.2
T_{PC}	1 s	V_{sup}	12 V

This type of PSU can deliver up to 30 A maximum current at lower voltages. As for the capacitor bank, the system can also include the output capacitor and thus double the total capacitance. The value of the inductor is explained as part of the design in chapter 5. Concerning the DUT, a discrete superjunction MOSFET, rated at 700 V and 75 A, is simulated, which has been electrically charac-

terised in the SPICE simulator and afterwards its thermal model is imported in PLECS®. The DUT during these simulations is considered to be connected to an ideal heat sink at 25 °C. Finally, the switching frequency of the buck converter is set to 40 kHz.

Single Channel Operation

In this case a single channel is examined by using the two phase interleaved buck converter. The two phases are operated at a 180° phase shift. The supply voltage is set to 12 V while the voltage across the DUT reaches a peak around 3.2 V (a lookup table is used to reproduce the on-state voltage based on the DUT's current and temperature). Figure 3.5 depicts the junction temperature swing together with the corresponding currents. For each buck converter the reference current is set to 42 A, and, as result the DUT's current rises up to 84 A. It should be noted that the waveforms of Figure 3.5a associated with the current are downsampled, and thus their actual ripple is not displayed. The actual current ripple is shown in Figure 3.5b, it is evident that the current ripple of the DUT is smaller and its harmonic content less than that of the individual converters. For this scenario the duty cycle of the buck converter is around 0.34 and as it increases, the current ripple of the DUT decreases. In [71], the output current ripple of a two phase interleaved buck converter normalized in regard to the single phase buck converter is provided, indicating that for the case study duty cycle a reduction of roughly 50 % is achieved. The analytical expression is given in Equation (3.1).

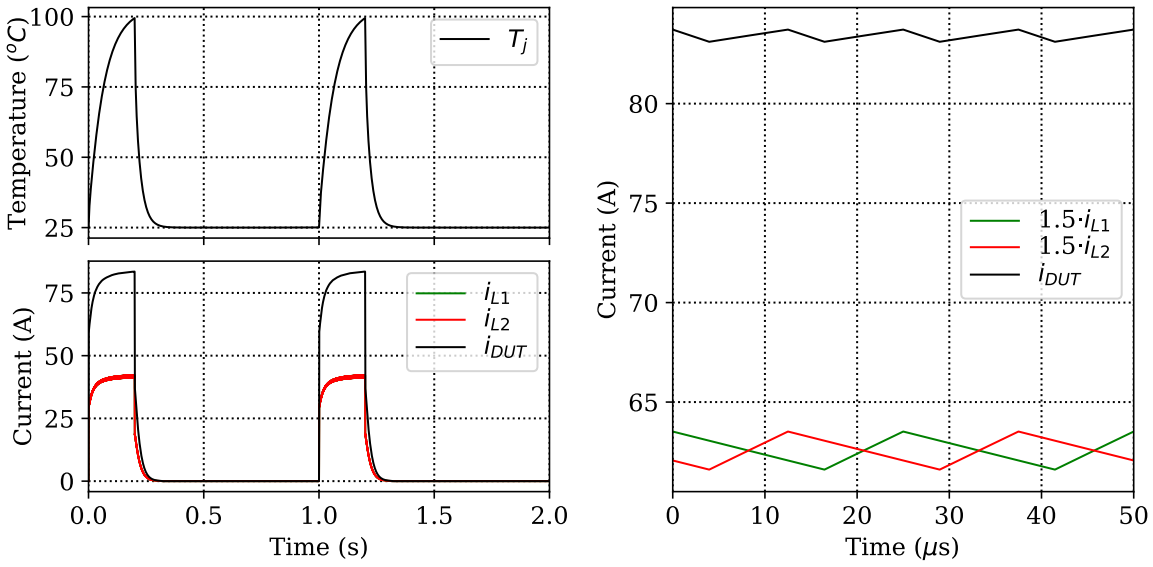


Figure 3.5: Two phase buck converter PC simulation example: (a) junction temperature swing and current evolution, (b) actual current ripple (the load current of each converter is scaled for illustrative reasons).

$$\frac{\Delta i_{DUT}}{\Delta i_{L_1,L_2}} = \begin{cases} \frac{1-2D}{1-D} & D \leq 0.5 \\ \frac{2D-1}{D} & D > 0.5 \end{cases} \tag{3.1}$$

This particular superjunction MOSFET can withstand pulse currents higher than the rated one (as stated in data-sheet), allowing to perform PC above its nominal value. The supply voltage is selected at this value in order to intentionally increase the duty cycle, and thus reduce the output current ripple. However, this might be not necessary since the high frequency accumulated damage may not cause significant influence on the final outcome. It is also worth mentioning that further duty cycle increase by reducing the supply voltage can lead to unstable situation, because the input current will start rising, as given by the product of the duty cycle and the output current ($D \cdot I_{DUT}$). This is an inherent limitation of this concept and can be partially compensated by adding more capacitance to the system or by increasing the supply voltage, as illustrated in Figure 3.6. It can be seen that an increase in the duty cycle of the PC results in limited temperature swing, which can be resolved by either increasing the capacitor bank to 1.3 mF, Figure 3.6a, or by increasing the supply voltage to 14 V, Figure 3.6b. The increase of the supply voltage causes a drop to the duty cycle, which, in turn reduces the input current. Nevertheless, this scenario affects the dynamic response of the system with a slight modification to the junction temperature transient swing. To sum up, it can be observed that this type of concept relies on the energy stored at the capacitor bank and the ability of a high voltage buck converter to operate reliably at lower voltages.

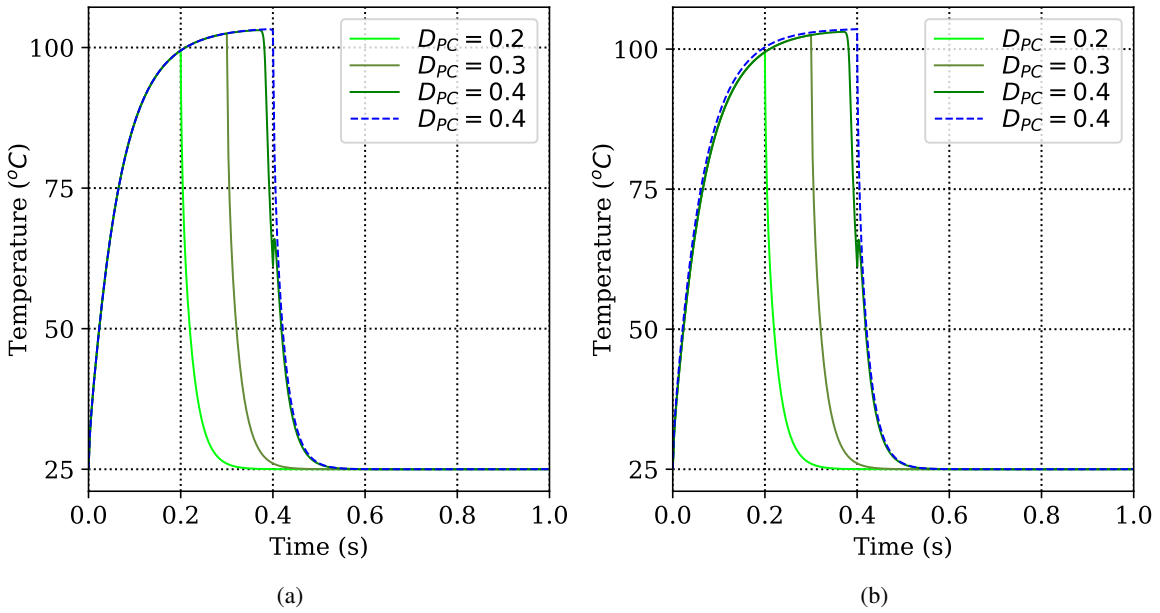


Figure 3.6: Junction temperature swing for different PC duty cycles: (a) solid lines refer to Table 3.1, whilst dashed line has a C_{in} = 1.3 mF , (b) solid lines refer to Table 3.1, whilst dashed line has V_{sup} = 14 V.

Multi-Channel Operation

The last example examines a multi-channel scenario, in which there are two interleaved buck converters operating in parallel mode. Each interleaved buck converter has a load of two series connected DUTs. The supply voltage is increased to 42 V and the PC duty cycle is set to 0.4, whilst the remaining parameters are the same as that of Table 3.1. The simulation result is depicted in Figure 3.7. It can be seen that the temperature swing is slightly higher than 75 K and the on-state voltage goes up

to 6.7 V, as the sum of both on-state voltages. Therefore, the duty cycle is lower than the previous simulation example, close to 0.175, and as a consequence, the current ripple increases, as shown in Figure 3.7b.

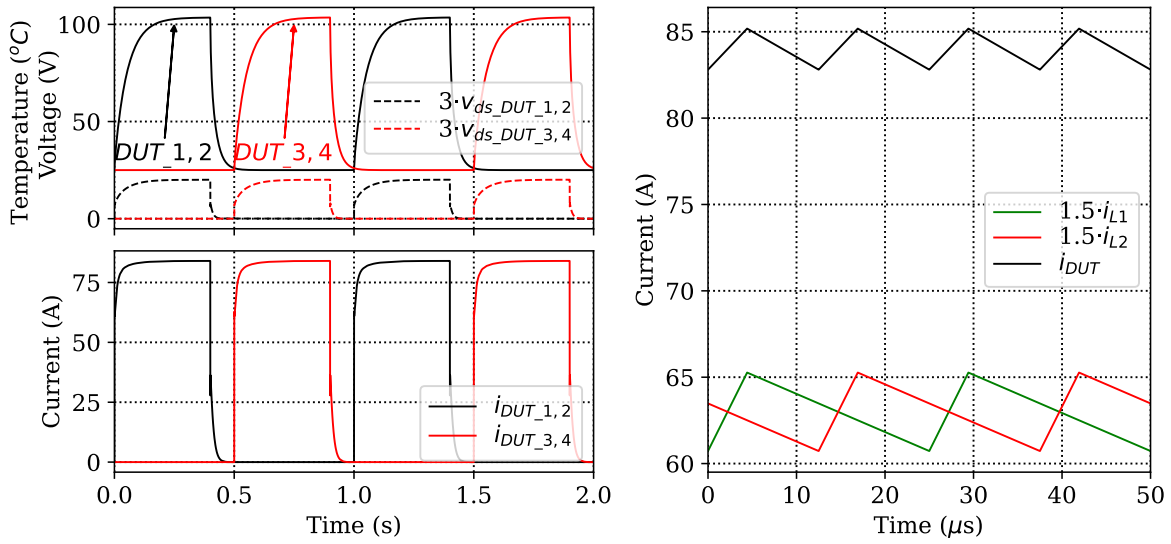


Figure 3.7: Multi-channel PC simulation example of two interleaved buck converters: (a) junction temperature swing and current evolution, (b) actual current ripple (the load current of each converter is scaled for illustrative reasons).

3.3.2 Double Pulse Testing

Among the reliability stress tests presented in this dissertation, the most distinctive one is the DP testing which is also the primary focus. Three different ways of realizing a repetitive DP in conjugation with their benefits and drawbacks are presented. Two concepts are performed with the arrangement of Figure 3.3a and the last one with the arrangement of Figure 3.3b. The following subsections analyze each topology separately.

Discontinuous DP Boost Test

In order to facilitate the analysis a simplified symbolic DP waveform, which can be applied repeatedly with certain duty cycle and repetition frequency in a discontinuous mode, is illustrated in Figure 3.8. During the execution of this test, the GS is constantly on and is turned off in case of DUT failure. The input voltage is set to the MV level and the current is ramped up to a desired current level I_1 with certain slope, determined by the load (inductor). Subsequently, the DUT is switched off and the current flows through the D_2 and the HV, which is practically an electronic load (EL). Depending on the voltage difference between the MV and the HV rail as well as the value of the inductance, the current can experience different negative slopes, which might not be acceptable, as denoted in Figure 3.8. During the next time interval (t_{r2}), the DUT is turned on again and the current rises. The duration of this interval should be adequately long enough to fully turn on the DUT, and finally, the DUT is turned off and the current falls to zero.

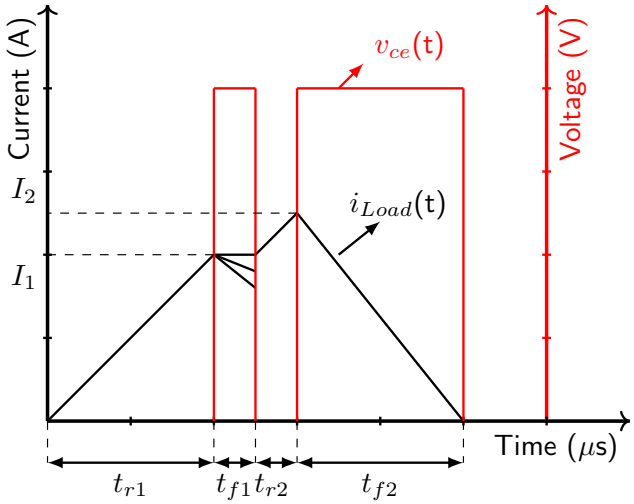


Figure 3.8: DP symbolic waveform.

By using a simplified approach, the load current can be calculated in Equation (3.2), where V_{in} is the MV supply voltage and V_{out} is the HV rail. Any voltage drops across resistive components, power devices, etc are neglected, leading to linear expressions.

$$i_{load}(t) \approx \begin{cases} \frac{V_{in}}{L}t, & 0 \leqslant t \leqslant t_{r1} \\ I_1 + \frac{V_{in}-V_{out}}{L}(t-t_{r1}), & t_{r1} \leqslant t \leqslant t_{r1}+t_{f1} \\ I_1 + \frac{V_{in}-V_{out}}{L}t_{f1} + \frac{V_{in}}{L}(t-t_{r1}-t_{f1}), & t_{r1}+t_{f1} \leqslant t \leqslant t_{r1}+t_{f1}+t_{r2} \\ I_2 + \frac{V_{in}-V_{out}}{L}(t-t_{r1}-t_{f1}-t_{r2}), & t_{r1}+t_{f1}+t_{r2} \leqslant t \leqslant t_{r1}+t_{f1}+t_{r2}+t_{f2} \end{cases} \tag{3.2}$$

The main rationale behind this circuit architecture is that the MV rail can be designed with lower voltage power devices, e.g. 600 V voltage class, whilst the HV rail can handle higher voltage class power devices, and dissipate the energy through the EL, functioning in constant voltage mode. However, this arrangement introduces certain implications in terms of performance. The most important one is the DP profile and how much the current is allowed to drop. Normally, during a standard DP the current should preferable present negligible decrement for a proper switching loss characterization. From stress testing point of view, the long-term drift is expected to be examined, and therefore high current gradients with minor current drop would probably be preferred. Another possibility is to let the current drop in a more realistic way such as in a real application, namely 5 % to 20 %. Therefore, the inductance of this setup can be estimated in Equation (3.3), where ΔV is the voltage difference between the two rails and α is the percentage of the current drop.

$$L \approx \frac{\Delta V t_{f1}}{I_1 \alpha} \tag{3.3}$$

Four parameters determine the size of the inductor, the falling interval which is around 3-6 µs, the voltage difference which can go up to 1 kV and even more, the peak current which can rise up to 400 A and the percentage of current drop.

In order to further elaborate on this concept, a simulation example of four identical DUTs, operating in parallel mode, under the test conditions listed in Table 3.2 is given. The first step is to calculate

the required load based on a predefined current drop, which in this case is selected to 5 %, and, as result the obtained inductance is rounded to 134 µH. The DUT is an IGBT rated to 1.2 kV and 75 A. It should be mentioned that the PSU and EL are considered ideal in terms of modelling, meaning that their dynamic response is not included.

Table 3.2: Discontinuous DP Boost Test Simulation Parameters

$I_{MV,max}$	30 A	$I_{HV,max}$	30 A
V_{in}	400 V	V_{out}	800 V
C_{in}	400 µF	C_{out}	400 µF
L	134 µH †	α	5 %
t_{f1}	5 µs	t_{r2}	5 µs
I_1	300 A	T_{DP}	6 ms

† The series dc-resistance is simulated to 30 mΩ

The PLECS® simulation model also includes the on-state voltage drops of the power devices with look-up tables. These relate to the actual power devices employed in the hardware prototypes, as given by their data-sheets. Likewise, their thermal models are included. However, their accuracy has only been validated with respect to manufacturer data. At the output of each stress board next to the DUT, there is a certain number of ceramic capacitors of X7R dielectric material, assisting to reduce the loop inductance and consequently large overshoots across the DUT, as will be explained in chapter 4. Their capacitance among other parameters is also influenced by the dc-bias voltage. This dependency can be modelled by a mathematical expression, as described in [72]. The model is reproduced in Equation (3.4), and it consists of four coefficients, namely C_o, C_{sat}, V_{th} and V_{tra}.

$$C(V_{bias}) = \frac{C_o - C_{sat}}{2}\left(1 - \tanh\frac{2(V_{bias} - V_{th})}{V_{tra}}\right) + C_{sat} \tag{3.4}$$

In this case the multi-layer ceramic capacitors (MLCCs) are from KEMET and the coefficients can be estimated by employing a non-linear curve fitting solver, presented in [73]. The outcome for a single capacitor is shown in Figure 3.9. It is evident that the real behavior shows certain discrepancy especially at higher voltages, causing the fitting model to deviate.

The next step is to extract the resulting coefficients, and then to substitute them in Equation (3.4). Finally, the model is imported to the simulation model by initializing the lumped capacitance based on the initial voltage. Between the ceramic capacitor arrangement and the output capacitor bank (C_{out}), there is a parasitic loop having certain inductance, which can be estimated via the hardware setup, however, in this case is assumed to 200 nH.

The simulation performance of this type of test is depicted in Figure 3.10. It can be seen that the peak current reaches roughly 290 A by applying a 100 µs pulse. Theoretically speaking, it would be expected to reach close to 298 A, however this is not the case since the voltage across the input capacitor bank drops during this pulse duration. Another minor contribution is from the resistive elements as included in the simulation model. The input capacitance is selected based on the available capacitors in the laboratory, as they were used in the design process of the prototype.

During the DP duration, the input capacitor bank discharges, as shown in Figure 3.10b, determined by the supply and load current given in Equation (3.5), where i_{sup} is the supply current of the PSU and t can be for example t_{r1} or any other time during the DP. The left part of Equation (3.5) is essentially

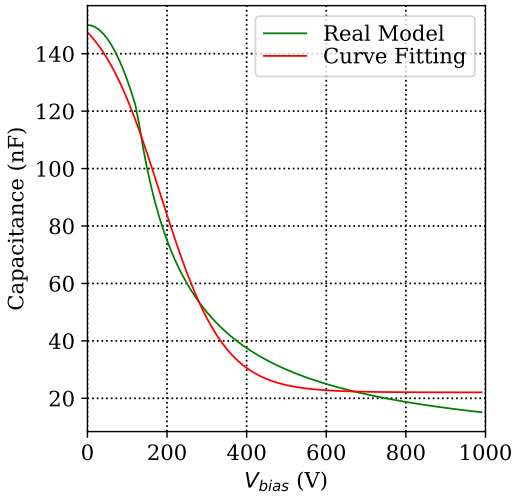
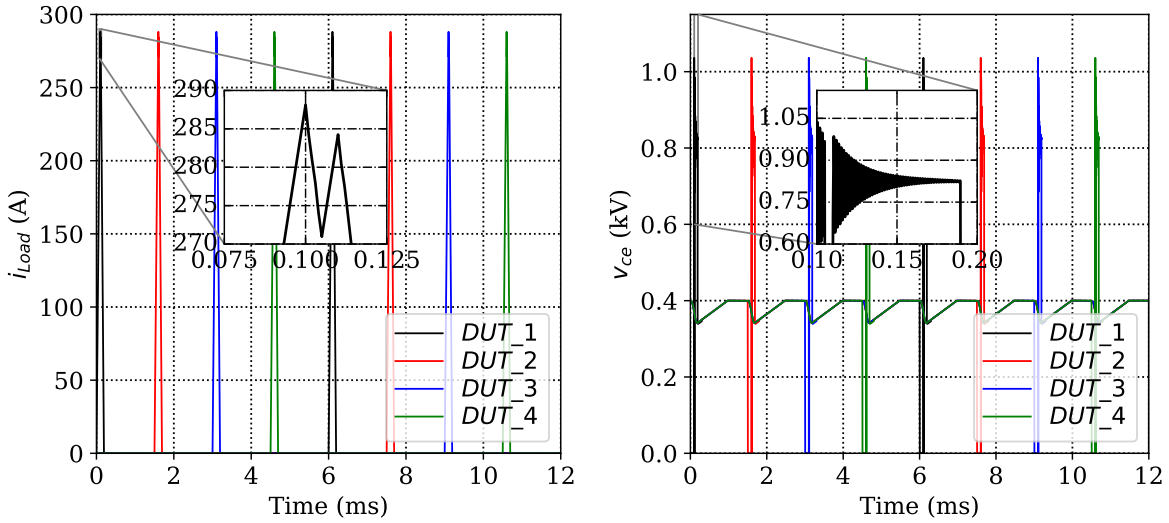


Figure 3.9: Ceramic capacitor's voltage dependence modelled by curve fitting.



(a) (b)

Figure 3.10: Simulation of the multi-channel discontinuous DP boost test: (a) load current of each stress board, (b) collector-emitter voltage of each DUT.

the net charge that the capacitor obtains or releases at the given time interval.

$$\int_0^t (i_{sup}(t) - i_{Load}(t))dt = C_{in} \int_{V_{in}(0)}^{V_{in}(t)} dV_{Cin} \tag{3.5}$$

By substituting in Equation (3.5) the ideal supply current of 30 A, the theoretical peak current of 298 A and the time duration of the first pulse, the capacitor voltage drop can be estimated.

$$\Delta V_{in} \approx \frac{(298 \cdot 0.5 - 30) \cdot 100 \cdot 10^{-6}}{400 \cdot 10^{-6}} \approx 30\,\text{V}$$

By taking the average voltage during this interval, the peak current can be estimated to 287.3 A,

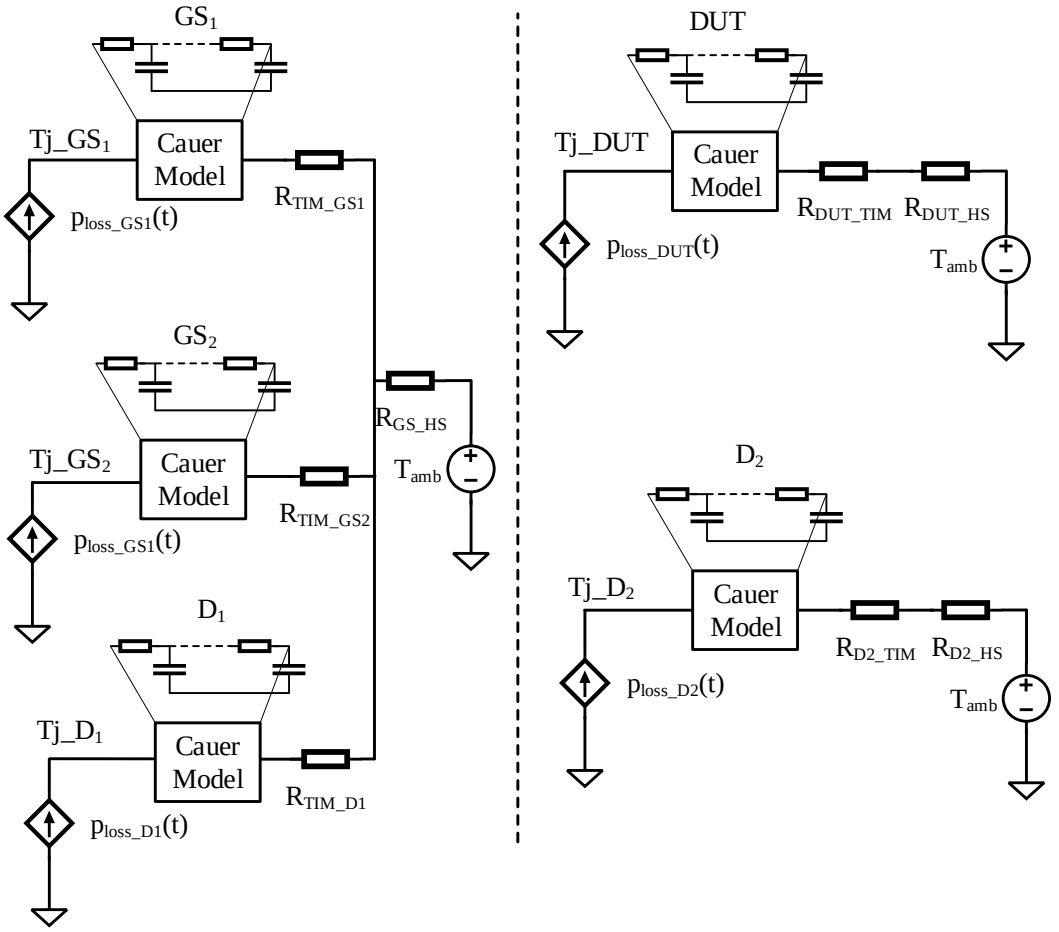


Figure 3.11: Incorporated thermal model for each power component of the stress board.

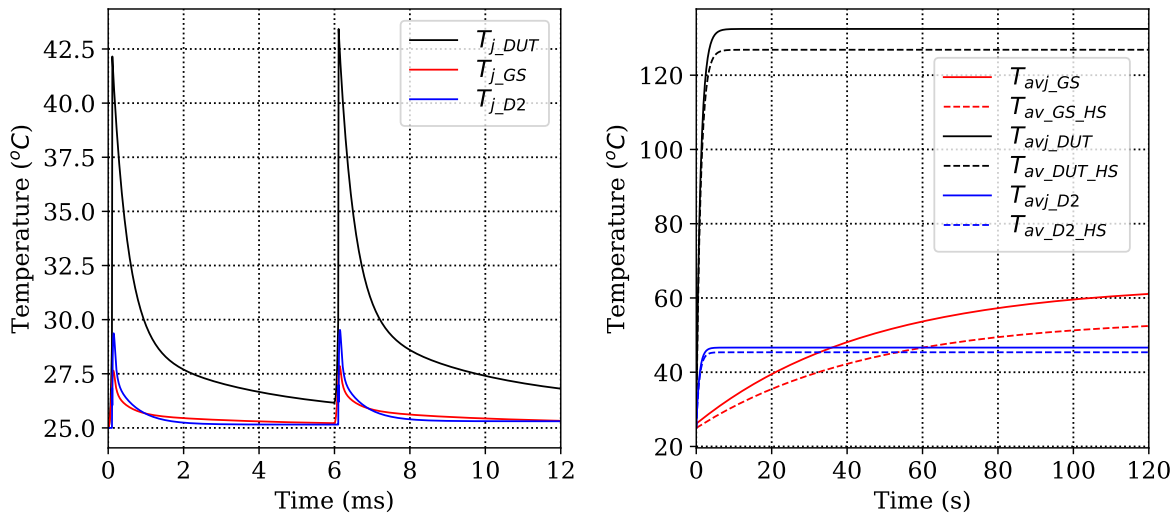
while the actual simulation peak current is 288.1 A. Furthermore, the total voltage drop can be roughly calculated by considering ideal triangular waveform for the load current with the estimated peak current and the total DP duration. The unknown parameter of the DP duration is the second falling time interval t_{f2}, which is approximated in Equation (3.6), yielding 89.5 µs. By repeating the previous step and substituting the total DP duration, the total voltage drop is found to be 56.7 V. The simulation voltage drop is 58.5 V, thus indicating reasonable accuracy. Finally, the recharging time interval can be calculated by substituting the total voltage drop in Equation (3.5), resulting in 756 µs. This result provides an indication when to trigger the DP of the next channel.

$$t_{f2} \approx \frac{LI_{p,est}}{V_{out} - V_{in}(t_{r1})} \tag{3.6}$$

Regarding the thermal performance of this concept, the following procedure is applied to reveal an indicative response. For each employed power device, namely the GS, the diodes D_1, D_2 and the DUT, thermal impedance, on-state voltage drop, and switching losses, as extracted from their data-sheets are imported into the PLECS® model, as described in the manual [74]. The thermal behavior of the heat sinks is modelled with their thermal resistance, as given in their data-sheet, multiplied with a factor of proportion due to forced convection as shown in the manufacturer's manual [75], where the air

flow is assumed to be $2\,\mathrm{m\,s^{-1}}$. The thermal interface material (TIM) is modelled only with its thermal resistance which is assumed to be $1\,\mathrm{K\,W^{-1}}$. The final thermal models are depicted in Figure 3.11, as approximately reflecting these of the final hardware prototype of Figure 4.5. Even though the DUT and the D_2 share the same heat sink, in this analysis their thermal models are separately treated. Nevertheless, it should be pointed out that a more precise approach would be to extract the thermal impedance of the whole system, as shown in [76]. Last but not least, heat spreading effects are not considered which can contribute to the actual temperature evolution.

The final simulation result in Figure 3.12a shows the detailed junction temperature course for each DP at the beginning of the test. The final average temperature, as depicted in Figure 3.12b, is estimated via another simulation model including only the thermal impedances, in which the average losses of the first model are imported. Essentially, the actual temperature will be the superposition of both figures. However, as the temperature rises, the energy losses slightly change, and thus the ΔT and T_{av}. It should be clarified that the accuracy of this thermal model may be limited with respect to parameter uncertainties, but still its contribution of relative temperature rise values strengthens the comparison between the concepts.



(a) (b)

Figure 3.12: Temperature evolution for a single stress board: (a) junction temperature at the beginning of the test, (b) average junction and heatsink temperatures - sum of the average switching and conduction losses (P_{GS} = 15.5 W - both GS, P_{DUT} = 35 W, P_{D_2} = 7 W).

The average losses of the DUT are approximately 35 W, meaning that with this type of heat sink a repetition frequency of 166.7 Hz is the feasible maximum for this mission profile. Another point related to the temperature gradients of the stress board is the load rms current, which in this case is around 31 A. The main benefit of this DP test is that relatively short DPs can be achieved and the ΔT of the GS remains low for its own reliability. On the contrary, some of the drawbacks include the use of the EL which raises the system's cost, the necessity of more PSUs and ELs or potential connection of chokes at the output to dissipate energy, as employed in motor drive applications, if a high number of parallel stressed DUTs is required, since the average input power of this simulation example is 7.7 kW. Finally, some operating points might require high loads which can considerably slow down the accelerating stress test goal, as can be noticed in Equation (3.3).

Standard DP Test

In this section the arrangement of Figure 3.3a is analyzed. Since the output is connected via a short cable to the input, the EL is not required and the total available input capacitance doubles. The GS is maintained in the on-state during the DP as in the previous arrangement. The major difference is that inductor's stored energy is dissipated through the D_2 and GS. Moreover, the left half bridge must now be able to sustain high voltages, because it follows the supply voltage. The benefit of this configuration is that at the first falling time (t_{f1}) the current presents relatively low drop, determined by the voltage drops across the GS, the diode D_2 and the other resistive elements. Furthermore, the inductor's value contributes to the final current rate of change.

The simulation parameters of this scenario are listed in Table 3.3. The load is selected to 50 µH so as to increase the load current rate of change but not too much, since at the second pulse (t_{r2}) the current can go beyond the switching capabilities of the DUT. Therefore, in this case this time duration is reduced to 3 µs.

Table 3.3: Standard DP Test
Simulation Parameters

$I_{sup,max}$	30 A	I_1	300 A
V_{sup}	800 V	T_{DP}	20 ms
C_{in}, C_{out}	400 µF	L	50 µH †
t_{f1}	5 µs	t_{r2}	3 µs

† The series dc-resistance is simulated to 16 mΩ, as roughly derived in chapter 5

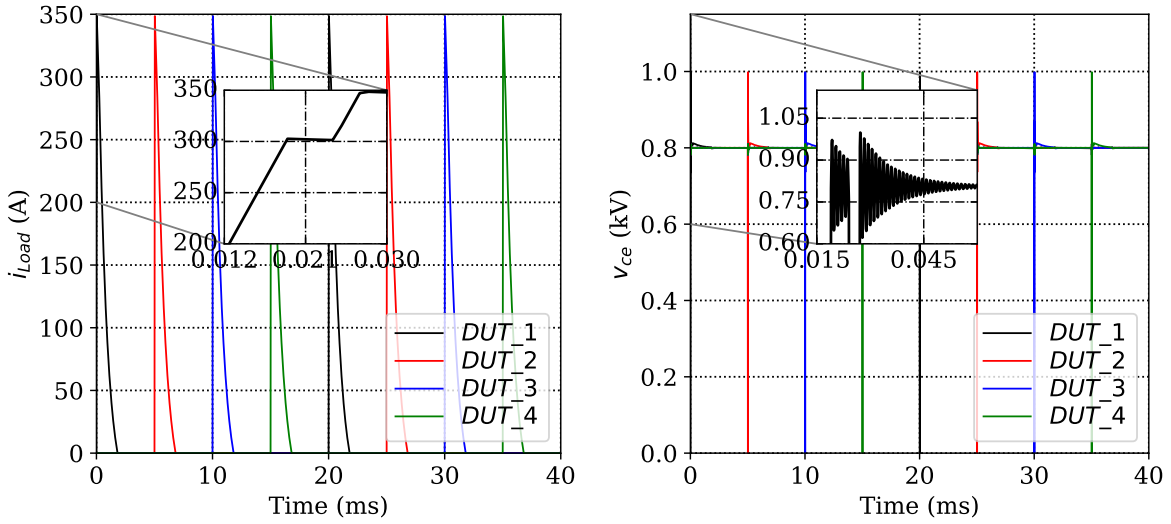
The load current and collector-emitter voltage for each DUT are illustrated in Figure 3.13. The rms current of the load is roughly 49 A, indicating that the stress board might be overloaded leading to higher temperature gradients, even though the repetition frequency is merely 50 Hz, three times less than the previous example. Furthermore, the current at the second pulse goes up to 350 A as another shortcoming. On the other hand, the current during the first falling time exhibits negligible drop of just 2 A.

The thermal performance of this simulation example is presented in Figure 3.14. It can be seen that the diode D_2 takes over the largest burden with the highest average junction temperature and ΔT. These operating conditions reveal that this type of test causes more stressful conditions to the GS and the stress board itself, which might not be in favour regarding the system's reliability.

This DP concept must limit significantly the repetition frequency in order to maintain low temperature gradients based on the given models. However, another type of cooling could be utilized to improve the performance with the penalty of extra cost. One of the benefits is that the PSU output power is relatively low, in this example around 616 W, allowing to parallel more channels with a single PSU.

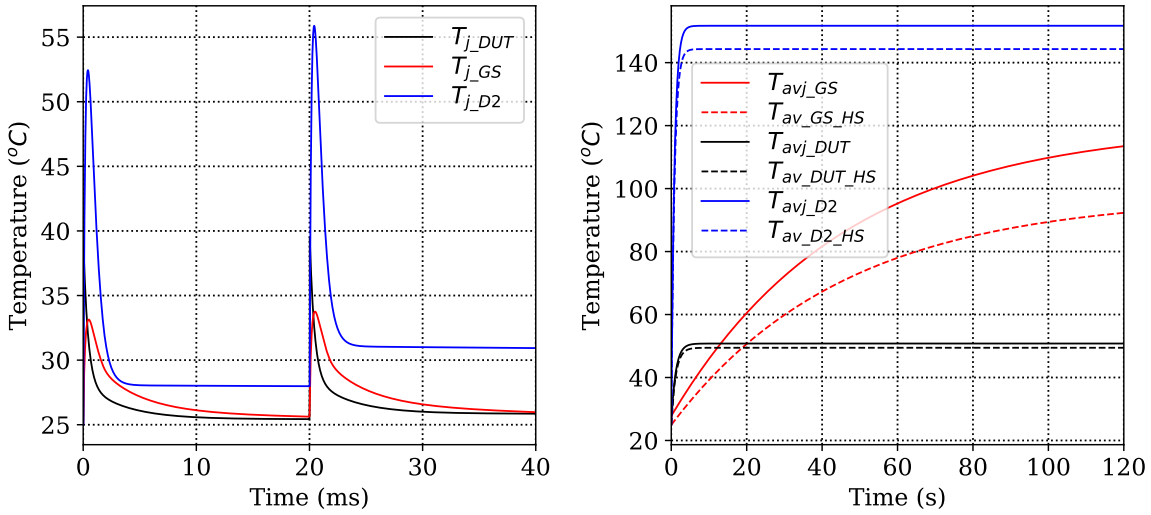
Full Bridge Based DP Test

The last executable DP is realized with the circuit arrangement of Figure 3.3a and its principle of operation is explained in Figure 3.15. In this concept the GS is actively employed in order to accomplish short DPs. Initially both switches are turned on and the current starts ramping up, then the first turn-off time interval occurs, in which the current flows through the GS and D_2. Upon the end of this interval, a concurrent pulse transition is applied so that the GS is turned off and the DUT is turned



(a) (b)

Figure 3.13: Simulation of the multi-channel standard DP test: (a) load current of each stress board, (b) collector-emitter voltage of each DUT.



(a) (b)

Figure 3.14: Temperature evolution for a single stress board: (a) junction temperature at the beginning of the test, (b) average junction and heat sink temperatures - sum of the average switching and conduction losses (P_{GS} = 38 W - both GS, P_{DUT} = 8.4 W, P_{D_2} = 41 W).

on. This moment is very critical for this configuration and is affected by the gate drive conditions and the involved propagation delays. Once the transition ends, the current is directed to D_1 and the DUT. Finally, the DUT is switched off and the remaining load energy recharges the input capacitor bank through D_1 and D_2. It is also worth mentioning that alternative options can be considered, e.g. the GS turn-off can be delayed as denoted with the dashed line or can occur after the DP duration as highlighted with the dotted line. However, these scenarios cause an increase in the energy losses due to the additional current increment.

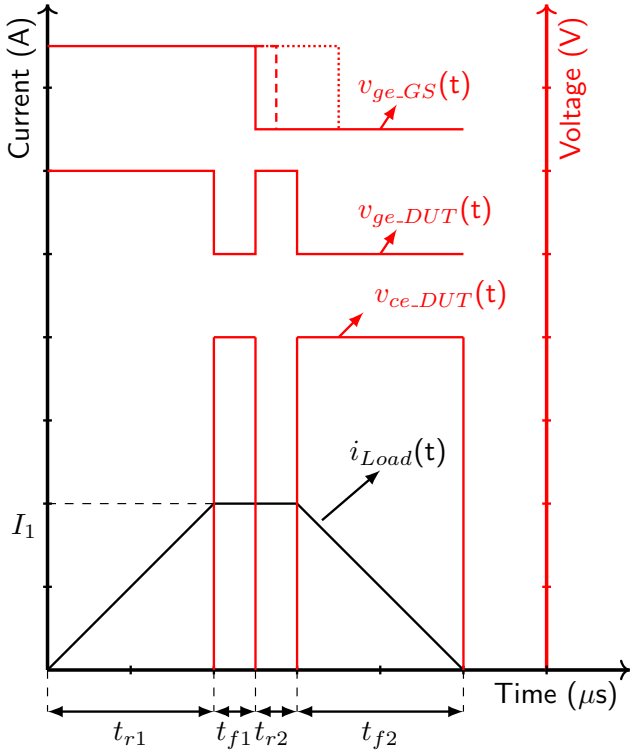


Figure 3.15: Full bridge DP ideal symbolic waveform.

The execution of such a reliability test can have certain limits, one might be the junction temperature of the DUT or the temperature gradients of the stress board together with the mounted components. Therefore, the load rms current can serve as an index concerning the reliability of the stress test system and can be provided as an input. The analytical rms expression of the ideal waveform is given in Equation (3.7).

$$I_{Load,rms} = \sqrt{\frac{1}{T_{DP}} \int_0^{T_{DP}} i_{load}^2(t)dt} \approx I_1 \sqrt{\frac{1}{3} \frac{t_{r1}+t_{f2}}{T_{DP}} + \frac{t_{f1}+t_{r2}}{T_{DP}}} \tag{3.7}$$

Based on Equation (3.7) and a given design limit of the rms value, the maximum repetition frequency can be calculated on condition that the desired junction temperature is not violated, yielding in Equation (3.8).

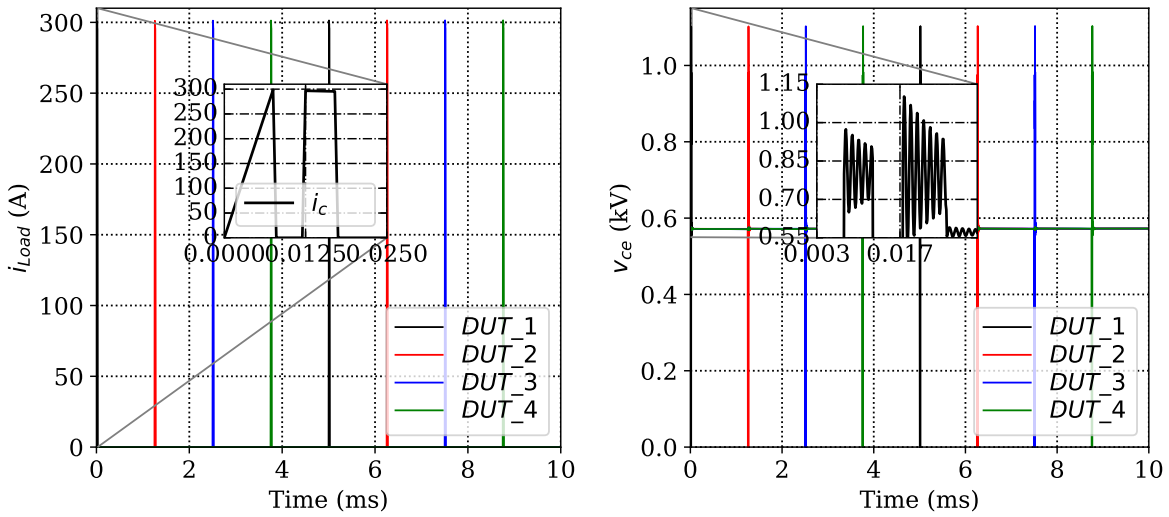
$$f_{DP} \approx \frac{(\frac{I_{Load,rms}}{I_1})^2}{\frac{2LI_1}{3V_{sup}} + t_{f1} + t_{r2}} \tag{3.8}$$

A similar simulation example is given where the theoretical optimal case is presented. The simulation parameters are listed in Table 3.4, where the load is decreased further so as to increase the rise time and to reduce the self-heating effect. Furthermore, the repetition frequency is set to 200 Hz, which is the highest possible among the presented concepts. Figure 3.16 shows the zoomed collector current of the first DUT, where the current rises up to 300 A within 8 µs. During the falling time, the load current drops by about 3 A. In practice, though, the current decrement might be different. In Figure 3.16b, it can also be seen that during the off-state the collector-emitter voltage settles around 570 V, a value determined by leakage currents and high ohmic voltage dividers, which can be significantly different in the actual setup.

Table 3.4: Standard DP Test
Simulation Parameters

I_{sup}	2 A	I_1	300 A
V_{sup}	800 V	T_{DP}	5 ms
C_{in}, C_{out}	400 µF	L	20 µH †
t_{f1}	5 µs	t_{r2}	5 µs

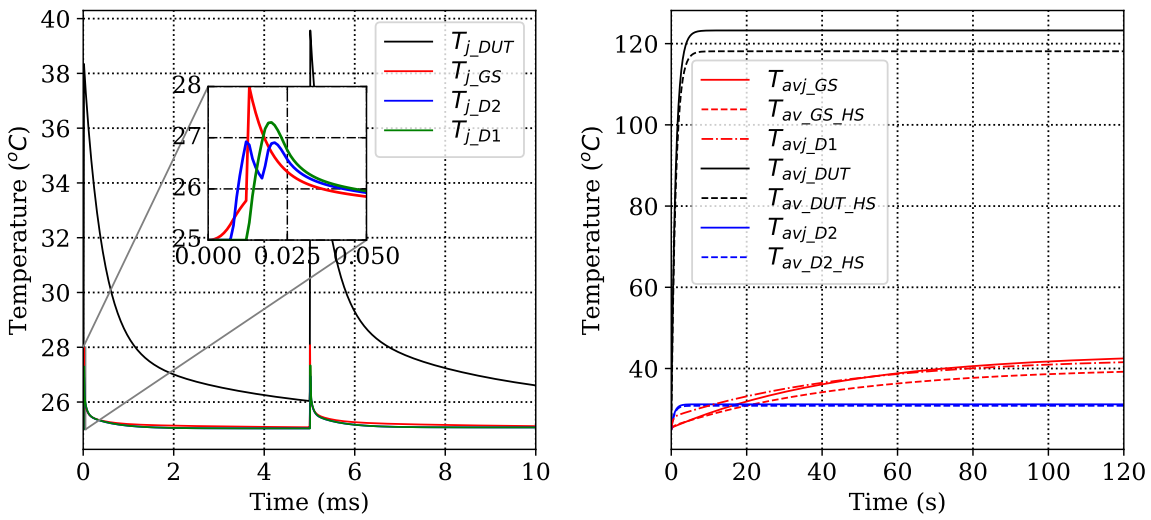
† The series dc-resistance is simulated to 20 mΩ, as roughly derived in chapter 5



(a) (b)

Figure 3.16: Simulation of the multi-channel full bridge based DP test: (a) load current of each stress board - collector current, (b) collector-emitter voltage of each DUT.

The thermal response is depicted in Figure 3.17, it can be discerned for the same cooling capability the temperature gradients are lower than in the previous cases, however as mentioned, the absolute simulation accuracy depends on the provided thermal models. It should be pointed out that the switching losses of the GS are characterized only for the turn-off at room temperature as will be shown in chapter 4. At the point of characterization the laboratory did not have an equipment to attach to the power device so as to apply elevated temperatures. Therefore, a scale factor of 1.5 is used to scale up



(a) (b)

Figure 3.17: Temperature evolution for a single stress board: (a) junction temperature at the beginning of the test, (b) average junction and heat sink temperatures - sum of the average switching and conduction losses (P_{GS} = 6 W - both GS, P_{DUT} = 32 W, P_{D_2} = 2 W, P_{D_1} = 2 W).

the switching losses at 125 °C, adding to the error uncertainties. Additionally, in the simulation the parallel arrangement of the employed devices is considered ideal, which in practice needs certain design measures to be applied to ensure symmetrical stress. Another possibility to improve the thermal response is to apply the projected average temperatures of Figure 3.17b to the full model by setting them as initial temperatures.

The great benefit of this concept is that multiple devices can be stressed in parallel without the use of EL. The input power of this example is just 55 W. It should be mentioned that in the electrical simulation domain, the switching losses are not modelled. Another stress indicator is the load rms current, which in this case is around 16.3 A and can be associated with the PCB and inductor losses. In a nutshell, this concept possessed the most noticeable advantages among the presented solutions.

3.3.3 SC and UIS Testing

In this section simplified SPICE simulation models are presented by giving examples of UIS for a single superjunction MOSFET and SC for a single IGBT. These models can also be useful in terms of comparison between the experimental and simulation results.

Avalanche Testing

Most of the power electronics applications include triangular waveforms, and therefore avalanche stress under similar conditions is more relevant. A symbolic waveform of an avalanche single event is shown in Figure 3.18. The avalanche energy can be calculated in Equation (3.9), where the avalanche duration t_{av} is estimated in Equation (3.10).

$$E_{av} = \int_0^{t_{av}} v_{ds}(t) i_{Load}(t) dt \approx V_{BR(DSS)} \int_0^{t_{av}} i_{Load}(t) dt \approx \frac{1}{2} t_{av} I_p V_{BR(DSS)} \tag{3.9}$$

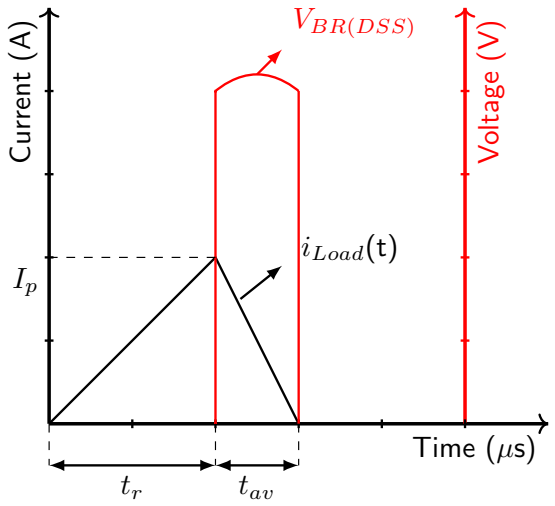


Figure 3.18: Avalanche symbolic waveform.

$$t_{av} \approx \frac{LI_p}{V_{BR(DSS)} - V_{sup}} \tag{3.10}$$

As already mentioned, the UIS test can be executed in two different ways. A simulation example is presented in Figure 3.19 to elaborate on that. The supply voltage is set to 200 V, the employed load is a 30 µH inductor and the repetition frequency is set to 40 kHz. A 3 µs pulse is required to reach roughly 20 A peak current. During the standard avalanche test the GS is in the on-state, and, as a result the avalanche energy and time are calculated based on Equation (3.9) and Equation (3.10), yielding 9 mJ and 1.5 µs respectively. The other way of avalanche testing is by actively employing D_1 and the GS. In this case, a turn-off signal is also transferred to the GS immediately before or after that of the DUT, and thus the effect of the supply voltage does not influence the avalanche energy. Therefore, the avalanche energy is calculated in Equation (3.11).

$$E_{av} = \frac{1}{2} LI_p^2 \tag{3.11}$$

By substituting the case study parameters, this is found to be 6 mJ. The avalanche time is around 1 µs, a difference which can be discerned in Figure 3.19. Moreover, an operator of such a system can also add a snubber, consisting of a series capacitor and resistor, across the load in order to damp oscillations, occurring after the avalanche event. However, the power dissipation of such an approach is of high concern. It should be emphasized that the avalanche breakdown voltage is temperature dependent, tending to vary during the avalanche regime, meaning that an accurate way of calculation is to numerically calculate the integral in Equation (3.9). For low voltage devices the second test might be preferred, since high test errors can be introduced due to small differences between supply and avalanche breakdown voltage.

SC Testing

The last category of applicable tests is the SC in which the inductance is substituted with a short. A trenchstop IGBT is used as the DUT, rated at 600 V and 120 A. The dc-link voltage is set to 400 V and the loop inductance to 200 nH for the purpose of modelling. The loop inductance is largely

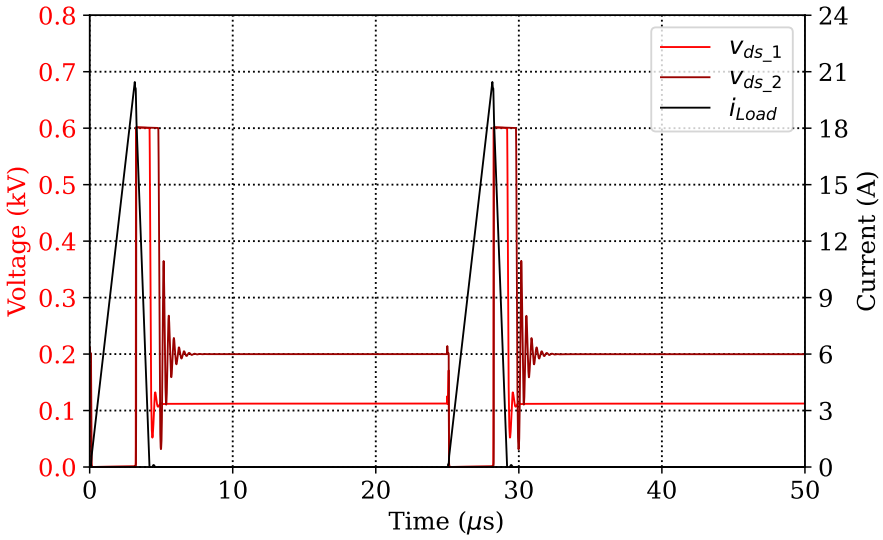


Figure 3.19: Simulation of a repetitive avalanche test using a superjunction MOSFET for two different scenarios. One scenario employs D_1 and a snubber in parallel with the load (v_{ds_1}), whist the other one is the standard avalanche pulse (v_{ds_2}).

formed along the input capacitor bank, the GS, the DUT and the power ground, refer to Figure 3.3e. Additional details will be shown in the experimental results. The gate resistance is set to 20 Ω and the gate voltage is adjusted to three different voltage levels as shown in Figure 3.20. The repetition frequency is chosen to 25 kHz for illustrative reasons, however, in practice will be much lower in order to avoid self-heating and to maintain the rms current at low values. For each different gate-emitter voltage the current saturates at different peak values, as determined by the IGBT characteristic I-V curves. It can also be seen that the employed IGBT's SPICE model does not include any temperature effect, as its current is constant during the saturation.

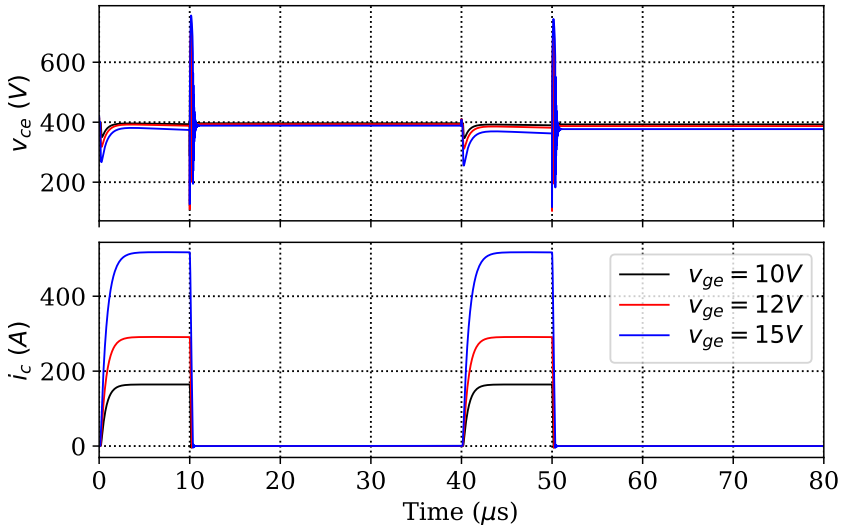


Figure 3.20: Simulation of a repetitive SC of a trenchstop IGBT under different gate-emitter voltages.

3.4 Conclusion

This chapter demonstrates the different relevant stress test concepts that can be realized based on the topology of Figure 3.2, named stress board. The application of all of these concepts increases the system's complexity in terms of selecting components that can fulfil such diverse mission profiles. Theoretically speaking, the reliability of the stress board must be much higher than that of DUT so that multiple DUTs can be stressed. Therefore, the PC concept is excluded, since the switching behavior of high voltage devices under low voltage levels is not efficiently implemented in the proposed environment.

The presented simulation concepts especially those focused on DP testing are linked to the last developed hardware prototype. The majority of used parameters are extracted from the data-sheets of the actual components and are subsequently imported to the simulation models. As far as the accuracy of the simulation model is concerned, its thermal model is simplified and based on data-sheet values only, and further modelling may be required. However, these simulation models comprise the foundations for a future modelling. As an example related to advanced thermal modelling, a study in [77] shows thermal modelling of standard extruded heat sinks by applying different methods which could also be applied here.

Chapter 4

Hardware Implementation

4.1 Introduction

Part of this chapter content is related to the author's publications in [1, 2]. This chapter discusses the different hardware prototype stages implemented over the course of this thesis. In particular, three different prototypes have been constructed serving certain objectives in the comprehension of the system's design and its own reliability. Some of the previously demonstrated stress test concepts are evaluated with a strong focus on the DP testing. In the beginning of this thesis an early stage hardware prototype is developed with the intention of studying early design weaknesses and potential new concepts such as the configurable gate driver, which is explicitly analyzed in chapter 6. In the second hardware prototype, a more compact solution is realized including a thermal management as well, which can fit into a subrack of a 19-inch tower system, highlighting its scalability. A backplane board is also constructed holding the input, output capacitor bank and an electromagnetic compatibility (EMC) filter. Finally, the third hardware prototype incorporates specific design modifications offering less set-up time and adjusted thermal management to allow the execution of the improved DP test based on the full bridge circuit.

An experimental section is undoubtedly part of this chapter, giving a short overview of the actual experimental laboratory setup in conjugation with the employed measuring instruments. Several design topics are analyzed, such as an estimate of the critical loop inductance, consisting of the local MLCCs, the DUT, the D_2 and the PCB tracks, the SC loop inductance, the protection scheme, the proper GS selection and their SC robustness, etc. Apart from the design aspects of the system itself, its performance is also presented by giving plethora of experimental examples and highlighting the key facts.

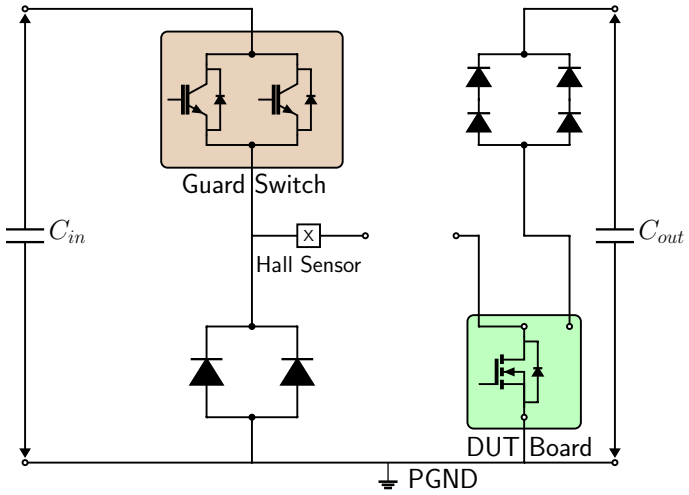
4.2 Hardware Prototype Overview

This section provides a general overview of the different hardware steps followed in a chronological order so that the reader can easily follow the subsequent experimental sections.

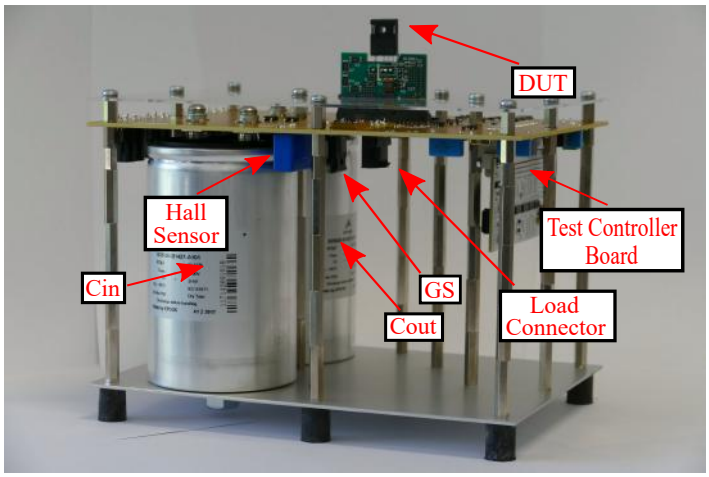
4.2.1 First Hardware Prototype

The block diagram of the first constructed hardware prototype together with the key components of the setup is depicted in Figure 4.1. In this hardware prototype the left half bridge is designed with MV

devices, composed of two parallel connected MOSFETs, and two parallel connected surface-mounted device (SMD) diodes without a heat sink. The GS is connected in a back to back configuration. The input and output capacitor bank are film type capacitors with nominal capacitance of 420 µF. A closed loop Hall sensor is selected to sense the load current for protection, condition monitoring and performance reasons. This type of closed loop Hall sensor offers the flexibility to measure high peak currents, in this case up to 400 A (design limit), by adjusting the output measurement resistance. Additionally, it has a fast reaction time, useful for protection reasons. The load in this prototype can be readily plugged via a cable connector. Concerning the right half bridge of the block diagram, the DUT is plugged through an edge connector, offering power and signal contacts. Lastly, the clamping diodes of the DUT are SMD type and are located on the stress board.



(a)



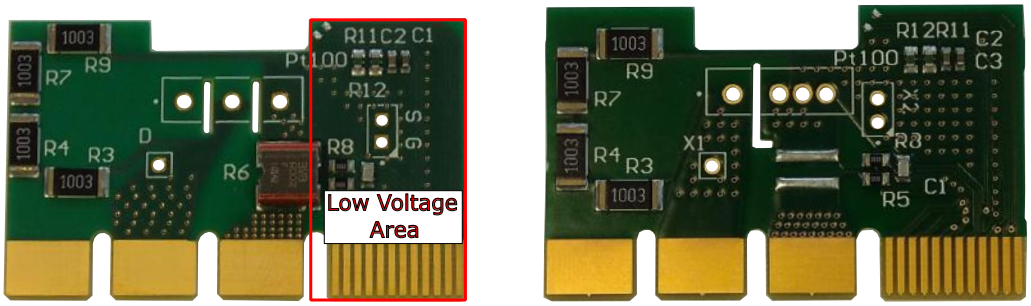
(b)

Figure 4.1: First hardware prototype: (a) block diagram, (b) hardware setup [1].

One of the requirements is to easily adjust the gate voltage of the DUT to facilitate the various stressing conditions. This is accomplished by software programmed adjustable gate voltage rails, as elaborated in chapter 6.

Another integral part of this hardware prototype, which is maintained with minor modifications, is

the DUT board and its interface, providing extra flexibility. The primary focus of this thesis are TO-247 discrete packages, and, as a result dedicated DUT boards are realized, as shown in Figure 4.2. It is also worth mentioning that DUT boards for SMDs could be manufactured. It is evident that a DUT board increases the modularity of the system by bringing about certain advantages, such as mounting different types of devices, adjusting the gate drive conditions by placing different gate resistors (located on the rear side of the DUT board), adding and examining different condition monitoring circuitry which can be connected via the low voltage area through the signal contacts. Particularly, these DUT boards include the gate sensing voltage, the drain/collector sensing voltage, the source/emitter current and the temperature sensor (Pt100 resistor), glued to the front side of the package. These condition monitoring circuitries have yet to be evaluated, however, to large extent the required space has been allocated for this purpose.



(a) (b)

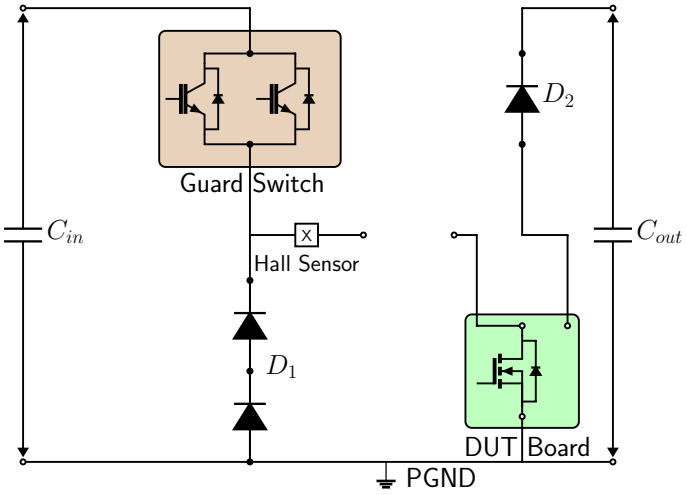
Figure 4.2: DUT boards: (a) front side of a 3-pin TO-247 device, (b) front side of a 4-pin TO-247 device.

In conclusion, this hardware prototype is realized with the goal of testing new concepts and studying early design flaws. This justifies its bulky size which in practice cannot support the requirement of a scalable system. However, it is the preamble of the following prototype versions.

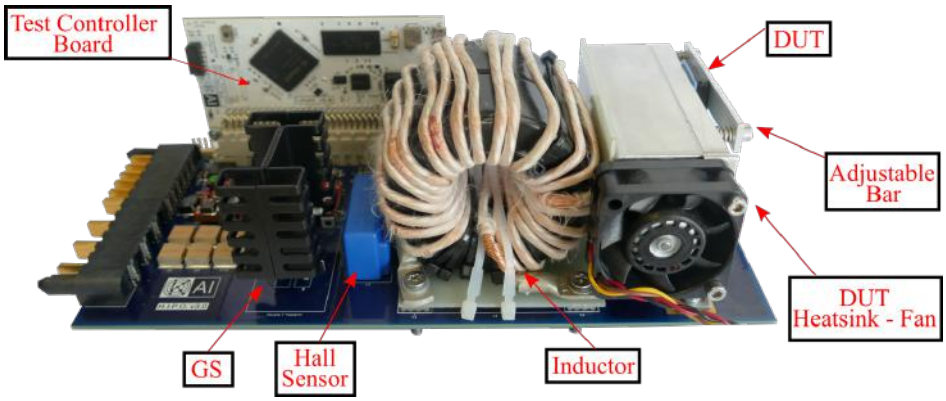
4.2.2 Second Hardware Prototype

The prime goal of the second hardware prototype is to perform the different stress test types in a repetitive manner as well as to shrink its size in order to provide a scalable solution. The fundamental concept is to utilize a subrack system which can be readily inserted into a 19-inch tower system, holding the maximum possible amount of stress boards. Additional fact is that KAI possesses a competence in the design of such systems, offering the flexibility of standardized construction with less cost and effort. The developed hardware prototype with its block diagram is illustrated in Figure 4.3. One of the design criteria is to increase the voltage stress level capability to 1.7 kV peak voltage. To this end, the GS is composed of two parallel connected IGBTs from IXYS rated at 1.7 kV and 75 A at 110 °C in a TO-264 package. Its freewheeling diode D_1 is composed of two series SMD diodes rated at 1.2 kV so that they can sustain higher voltages, located beneath the GS on the bottom layer. Another new feature is the screw-based load interface, in this illustration case a magnetic core inductor is mounted as analyzed in chapter 5. The right half bridge is composed of the DUT board, maintaining the same features as the first hardware prototype, and its SiC clamping diode located on the front and attached to the DUT heat sink. An adjustable spring pressure bar to mount the DUT is also employed. Each channel is rated for 30 A rms current to achieve lower temperature gradients and avoid excessive hotspots. There is also the possibility to mount a dedicated fan to the DUT heat sink. Finally, on

the stress board there is a certain number of ceramic capacitors to assist the hard switching events by reducing the critical loop inductance for each active switch.



(a)



(b)

(c)

Figure 4.3: Second hardware prototype: (a) block diagram, (b) stress board (100 mm × 220 mm), (c) front side of the stress board.

The major advantage of this hardware architecture is that several parts can be modular, such as the DUT board, offering dedicated design for different packaging technologies, the load, and even the test controller board. It should be pointed out that some tests might require higher inductance loads, but the available board space might limit the feasibility of such loads.

The bulky capacitor banks are now shifted to the backplane board accommodating up to four channels for parallel stress test scenarios, as portrayed in Figure 4.4. These capacitor banks are rated up to 1.5 kV, offering higher voltage range than the previous prototype, but on the other hand they provide only about half the capacitance. It should be noted that the capacitor selection is also affected by the market availability. The backplane board also incorporates an EMC filter to cancel out unintentional noise to the PSU. It can be seen that the size of this board is designed in a way to fit into the subrack and subsequently to the 19-inch tower.

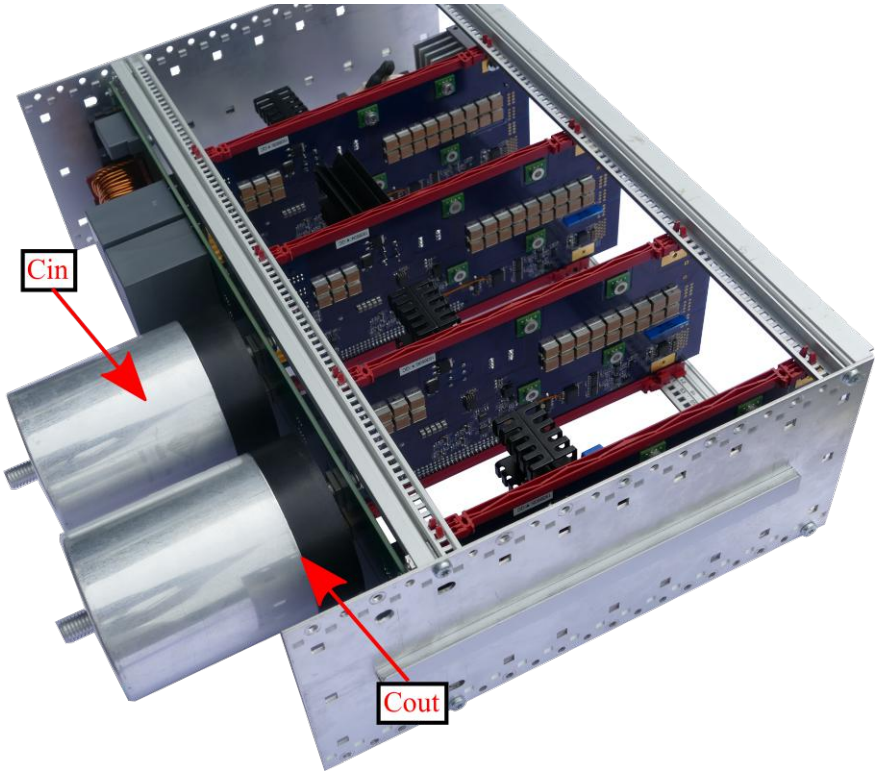


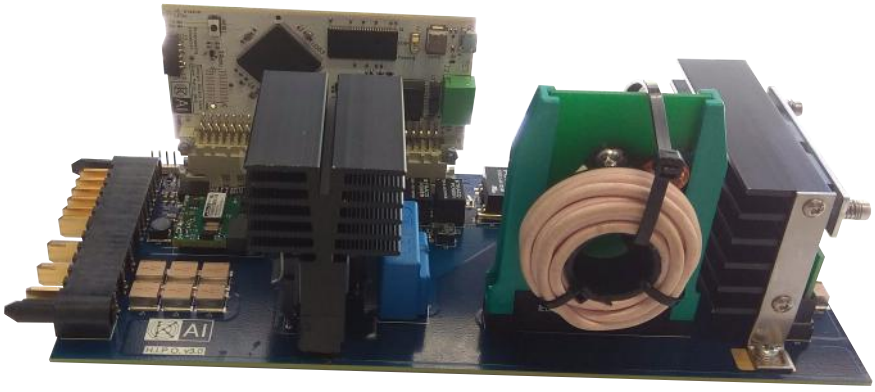
Figure 4.4: Backplane board within the subrack of a 19-inch system.

To sum up, this hardware prototype version consolidates the particular features that can render this reliability stress test system scalable under reasonable size.

4.2.3 Third Hardware Prototype

As far as the third hardware prototype is concerned, there is a series of additional introduced modifications, in the view of enhancing its modularity and performance. Figure 4.5 presents the lateral and front side view of the latest prototype. One of the central changes is the shift of D_2 (see Figure 3.2) on the DUT board, as shown in the front view. Therefore, the system's operator can test different combinations of clamping diodes and DUTs, thus enabling the possibility to resemble realistic application conditions. Furthermore, this shift allows now the DUT's heat sink to a small degree to slide back-

ward or forward along the stress board and simultaneously to maintain its electric potential to power ground, offering extra flexibility in regard to mounting different types of discrete power devices. In order to ensure high voltage functionality (1.5 kV dc-link voltage), the edge connector splits in a way to increase the creepage distance between the high (collector/drain) and low voltage (emitter/source) potential, as related to the rms voltage according to IEC 60664-1. The last modification of this board area is about the critical loop inductance of the DUT where both the DUT and D_2 are placed relatively tight as well as the ceramic capacitors, which are placed directly next to them on the stress board.



(a)

(b)

Figure 4.5: Third hardware stress board prototype (100 mm × 226 mm): (a) lateral side view, (b) front side view.

The next stage including significant amendments is the load interface, which is substituted by an edge connector with card guides instead of the screw-based connection. The main advantage of this approach is the reduced effort of mounting, and, as a result less time to initialize the stress test. Based

on the full bridge based DP concept, the required load inductance can be further reduced, which can assist in the development of compact solution, as shown with the air core coils. Nevertheless, the stray field might couple noise to sensitive surrounding circuitry which needs to be addressed, as further discussed in chapter 5. Moreover, the load's sectioning and the card guides can reduce the mechanical stress and offer better electrical contact especially in case of a horizontal placement within the tower.

In this hardware prototype, the left half bridge is modified in a way to support the full bridge based DP test. Consequently, the freewheeling diode D_1, a through hole TO-247 rated at 1.7 kV and 110 A continuous forward current at 100 °C, is mounted on a different heat sink type than the previous board so that it can dissipate energy in a more efficient way. The other side of the heat sink accommodates the two parallel connected IGBTs, rated at 3.6 kV and 125 A at 25 °C from IXYS in a TO-247PLUS-HV discrete package, offering improved creepage distance. Additionally, based on their reverse-bias safe operating area (RBSOA), they are capable of turning off 200 A each up to 2.8 kV, which is well beyond the design limits and consequently covering the design specifications. A new programmable gate driver, using an inter-integrated circuit (I^2C) communication interface, is employed having an additional redundant protection circuitry, that is the desaturation method. Last but not least, the heat sink orientations are such that the air forced cooling direction is along the air core inductor's magnetic axis. Supplementary holes on the load board could additionally assist in a better-balanced inductor cooling.

The last introduced feature is the fiber optic arrangement, as noticed on the right hand side of Figure 4.5b, providing the possibility to connect adjacent channels in a daisy chain so that they can be sequentially triggered without potential coupled noise issues through standard wired connection.

To conclude, the last hardware version improves the overall thermal management as well as introduces features allowing advanced modularity and configurability of stress tests, reaching the goal of 1.5 kV dc-link voltage.

4.3 Experimental Results

Throughout this section, the most significant experimental results are highlighted, clarifying the design goals and the way toward to achieving them. In particular, a generic description of the physical laboratory environment and afterwards the key design characteristics of the stress test system as developed over the course of the various hardware prototype stages are given. Finally, several examples of stress tests are presented to demonstrate the stress test bench's overall performance.

4.3.1 Summary of Laboratory Setup

The generic view of the HV laboratory setup is depicted in Figure 4.6. This laboratory division is dedicated for HV power electronic applications, used by two projects. In the middle, a rack tower is located holding the PSUs, the HOST, the Ethernet switch and all the functional safety features. Specifically speaking, there is a PSU from Keysight Technologies providing supply voltages up to 1.5 kV and currents up to 30 A, and an EL rated at 800 V and 30 A. Furthermore, their power handling capability is limited to 15 kW and 3.2 kW respectively. Each μC is connected via Ethernet cable to the Ethernet switch and subsequently to the HOST, as also denoted in Figure 1.2. The dc bus voltages can be set and measured through the HOST. As for the functional safety, it is realized via a programmable logic controller (PLC), which monitors the voltages across the HV PSU and the EL. The hardware setup is situated within a safety box, which is locked via a relay mechanism when a predefined threshold voltage is exceeded. The voltage level status is signalled with tower lights.

Finally, the LV power supply provides 24 V for the proper operation of the auxiliary hardware circuits.

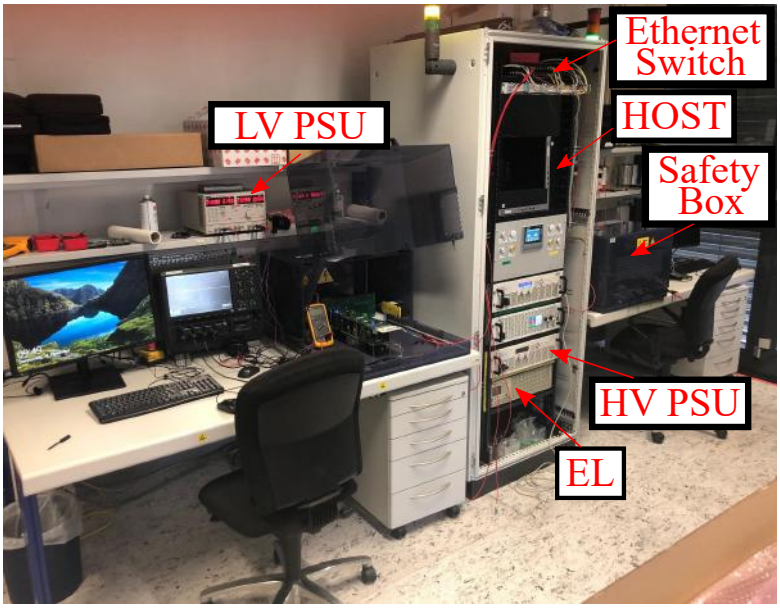


Figure 4.6: HV laboratory setup.

Apart from the requisite safety measures, the laboratory is equipped with measuring instruments necessary for the evaluation of the developed prototypes. All the employed measuring equipment is listed in Table 4.1. For clarity reasons, all the following presented experiments have been conducted at room temperature.

Table 4.1: Measurement Equipment

Oscilloscope	LeCroy HDO6104	Current Probe	LeCroy CP150
Voltage Probe	LeCroy HVD3106	Current Probe	LeCroy CP030
Rogowski Coil	PEM CWT MiniHF 3 - 600 A	Fiber Optically Isolated	LeCroy
Rogowski Coil	PEM CWT MiniHF 06 - 120 A	Voltage Probe	HVFO103

4.3.2 Critical Loop Inductance Estimation

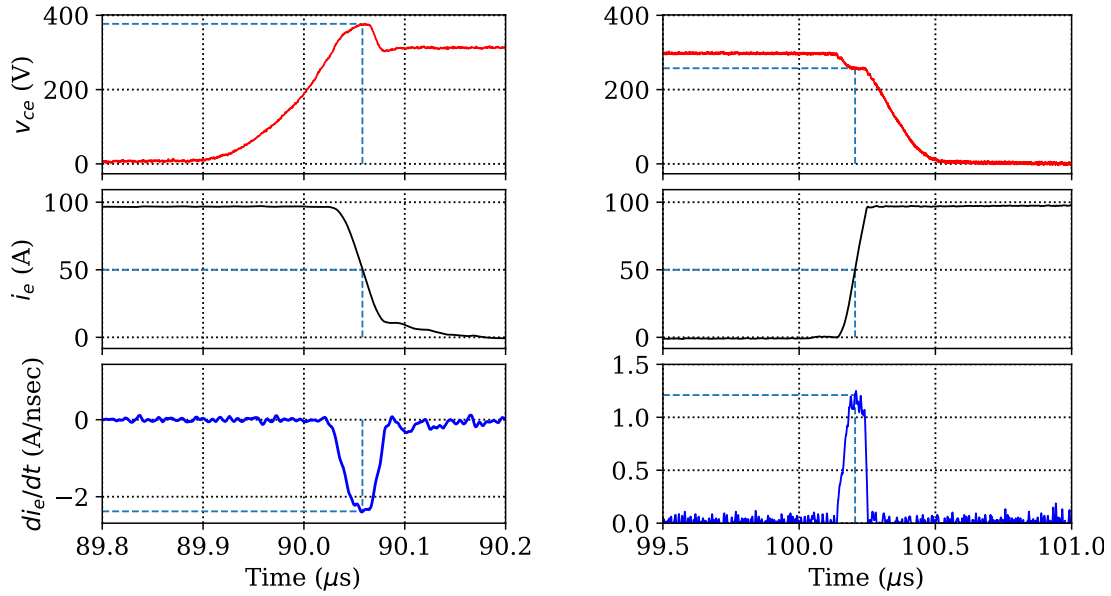
One of the most critical performance indicators of the reliability stress test system is its critical loop inductance. Generally speaking, in a boost type dc/dc converter the output loop presents the largest criticality, since the current does not flow continuously. Therefore, its output loop should be theoretically minimized so that excessive overshoots can be mitigated. In order to estimate the critical loop inductance, an estimation technique is employed in this thesis, as analyzed in [78] where loop resistance errors are eliminated. The advantage of this method is its simplicity and easy applicability. The instantaneous turn-on and turn-off Kirchhoff's voltage law (KVL) equations are combined together for this purpose. By considering the same instantaneous current at turn-on and turn-off and subsequently subtracting them, the loop inductance is estimated in Equation (4.1).

$$L_{cr} = \frac{v_{ce,off} - v_{ce,on}}{\frac{di_{c,on}}{dt} + \frac{di_{c,off}}{dt}} \tag{4.1}$$

A DP is applied to acquire the turn-on and turn-off by using an IGBT in a TO-247 package as the DUT. The voltage drop during the DP is assumed to be negligible and thus its influence is disregarded. The final outcome of the experiments is depicted in Figures 4.7 to 4.9 and their summary is listed in Table 4.2 by explicitly considering each hardware prototype.

Table 4.2: Critical Loop Inductance Estimation Results

Units	First	Second	Third
$v_{ce,off}$ (V)	380	346	372
$v_{ce,on}$ (V)	256	192	253.3
$\frac{di_{c,off}}{dt}$ ($\mathrm{A\,ns^{-1}}$)	2.37	1.8	1.47
$\frac{di_{c,on}}{dt}$ ($\mathrm{A\,ns^{-1}}$)	1.2	0.94	0.85
L_{cr} (nH)	35	56	51

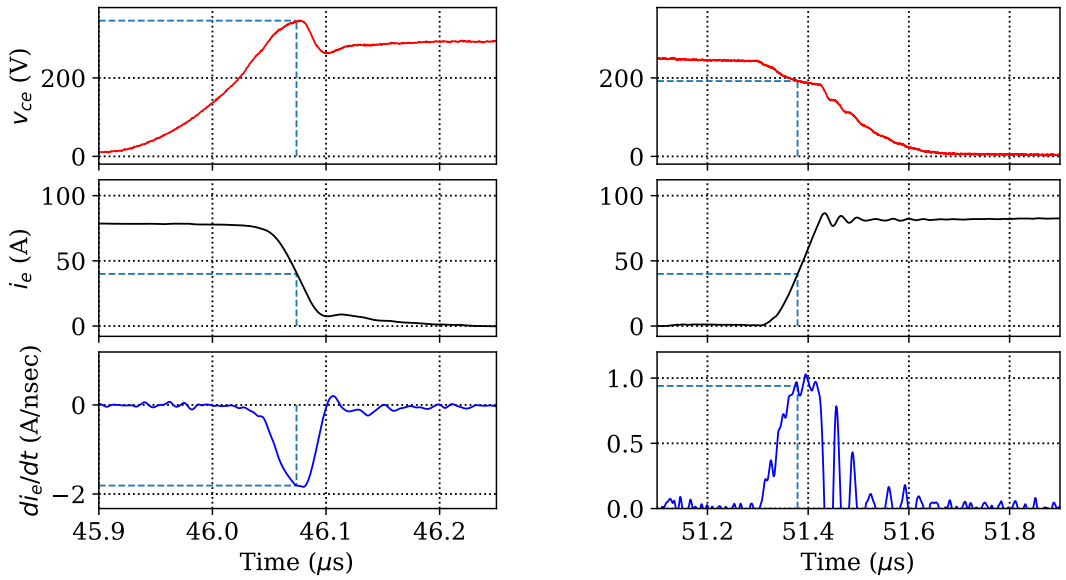


(a) (b)

Figure 4.7: First hardware prototype - critical loop inductance estimation at 50 A: (a) turn-off, (b) turn-on.

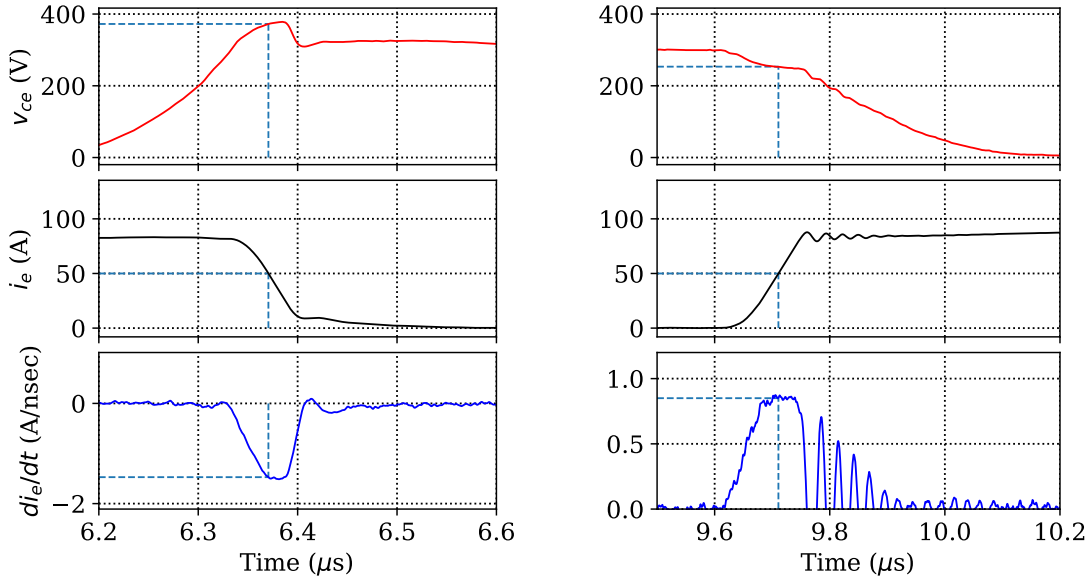
For each case, the numerical calculation of the emitter current rate of change is performed by recording its instantaneous value. The measurements for the first two hardware prototypes are performed without the use of heat sink, while the measurement for the third prototype is executed in its final mounting position, as shown in Figure 4.5b. This has an additional impact on the final outcome. As already mentioned, the first hardware prototype is composed of SMD diodes and ceramic capacitors directly beneath them, hence a shorter loop area is formed. On the other hand, the second and third hardware prototype are tested with a through hole diode which finally increases the total loop area. An SMD diode can also be used on the latest DUT board version, in the prospect of further decreasing the loop inductance. Therefore, the presented example accounts for the worst case scenario. Last but not least, some of the potential error sources of the presented method include the accuracy of

the measuring instruments, their bandwidth, signal processing and read-out errors, parasitic elements of PCBs and involved components, and potential coupled noise on the probes.



(a) (b)

Figure 4.8: Second hardware prototype - critical loop inductance estimation at 40 A: (a) turn-off, (b) turn-on.



(a) (b)

Figure 4.9: Third hardware prototype - critical loop inductance estimation at 50 A: (a) turn-off, (b) turn-on.

4.3.3 SC Loop Inductance Estimation

Another crucial performance indicator is the minimum applicable SC inductance. The smaller the stray inductance, the lower the dc-link voltage drop and thus a potential increase of the thermal stress on the DUT. It should be understood that the modular nature of the system can limit the stray inductance to higher values. Furthermore, the distributed arrangement of the channels can cause impedance modifications per channel.

A simplified curve fitting model is applied to estimate the loop inductance forming along the capacitor bank, the GS, the Hall sensor, the load board, the DUT and the power ground (see Figure 3.3e), as given in Equation (4.2). Even though the actual circuit arrangement is more complex, the circuit simplification provides a quick but reasonable estimation. The unknown parameters R_l and L_l are extracted by applying the non-linear curve fitting solver, described in [73], in Equation (4.2), after conducting a single SC test, using an IGBT as the DUT, by capturing its collector-emitter voltage (v_{ce_DUT}) and the short circuit current (i_{sc}). The supply current is preset to 10 mA, the initial dc voltage is precharged to 800 V and the input capacitance is the rated value of the input capacitor bank.

$$v_{ce\_DUT}(t) = V_{C_{in}}(0) - \int_0^t \frac{i_{sc}(t) - i_{sup}(t)}{C_{in}} dt - R_l i_{sc}(t) - L_l \frac{di_{sc}(t)}{dt} \tag{4.2}$$

The first hardware prototype is excluded from this analysis and only the last two are presented, since they approach the final solution. The final outcome of the experiments is shown in Figure 4.10. Both cases have similar gate drive conditions except their positive gate voltage, which is set to 16 V, see Figure 4.10a and 15 V, see Figure 4.10b. The other conditions are the negative gate-emitter voltage to -5 V and gate resistance to 15 Ω. The summary of the estimated parameters is listed in Table 4.3. It is evident that the third prototype is strongly affected by the new component arrangement, mostly attributed to larger on-state GS voltage drop, the load interface and the new GS spatial arrangement. Therefore, further investigations should be carried out even with the assistance of dedicated software tools, able to extract loop inductances of sophisticated PCB arrangements. For example, a measure that can be applied to reduce the stray inductance is to parallel connect many capacitors [39]. Another helpful measure could be the back to back arrangement of the IGBTs, since their stray field might be partially compensated.

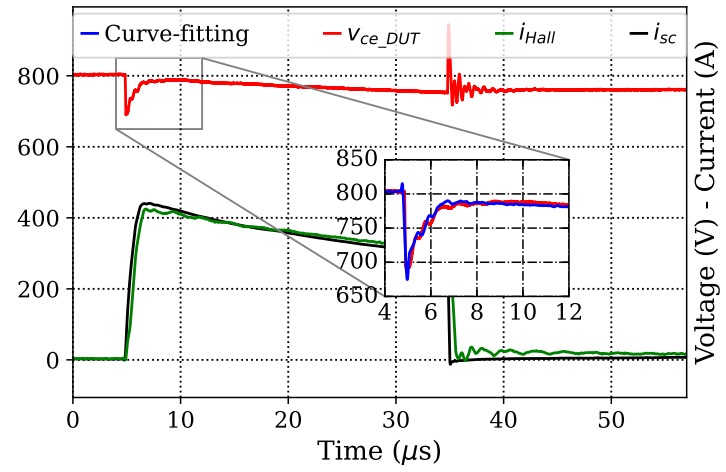
Table 4.3: SC Loop Inductance Estimation Results

Units	Second	Third
L_l (nH)	175	480
R_l (mΩ)	29.5	68

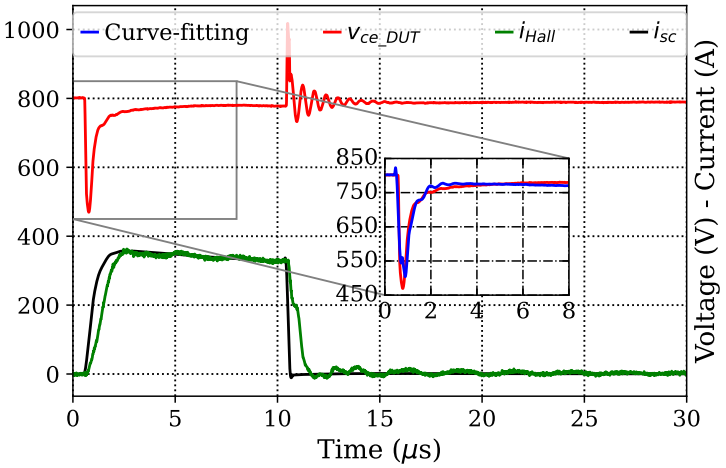
4.3.4 SC - Overcurrent Protection Topology

The output of the closed loop Hall sensor is essentially a current signal, which is converted to a voltage signal by feeding it to a shunt resistor (R_M), named measurement resistor, and tied to the μC ground. This signal is subsequently subject to certain signal conditioning filter stages, as illustrated in Figure 4.11. Finally, the adjusted signal is read by the μC and is also transferred to the overcurrent protection.

The general principles of operation of the closed loop Hall sensors are thoroughly elaborated by the manufacturer in [79]. Some of the advantages include galvanic isolation, fast response time and



(a)



(b)

Figure 4.10: SC loop inductance estimation: (a) second hardware prototype (Hall signal across the measurement resistor), (b) third hardware prototype (Hall signal after the signal conditioning filter circuit).

high accuracy, but, to the contrary, their size is relatively large and they cost more than other technologies. In this specific application, fast response time is of paramount importance for the detection of overcurrents and SCs as already mentioned.

Regarding the signal conditioning filters, a low pass filter is initially placed for the attenuation of potential high frequency noise, meaning that its cut-off frequency is relatively high compared with the transducer's bandwidth. Then a resonant filter is necessary, as the step response of the Hall sensor during a SC pulse causes a resonance, and, as result it can erroneously trigger the protection, as shown in Figure 4.12. This is attributed to the leakage inductance and parasitic capacitance of the sensor's built-in transformer. The introduced resonant filter is tuned in a way to cancel this frequency out, acting as band stop filter. This idea stems from the twelve-pulse line frequency converter used for high voltage direct current (HVDC) applications, in which the current harmonics should be cancelled out, as explained in [80]. The final damped result is depicted in Figure 4.10, as a new introduced

feature of the last hardware prototype. The next stage includes the differential amplifier circuit, which scales the input signal to match with the voltage range of the μC. More specifically, it scales an input signal from 0 A - 500 A to 0 V - 3 V. A small offset is also provided, accounting for potential error drifts of the Hall sensor. Finally, the signal is transmitted to the μC and the overcurrent protection comparator, configured in a active-to-low arrangement. The overcurrent voltage reference ($V_{OC,ref}$) is provided via a digital-to-analog converter (DAC).

Immediately after the comparator, the signal is propagated to the error logic circuit, as meticulously described in [14, 15]. When the comparator's output is set to low, an error signal drives the gate of GS to its off-state.

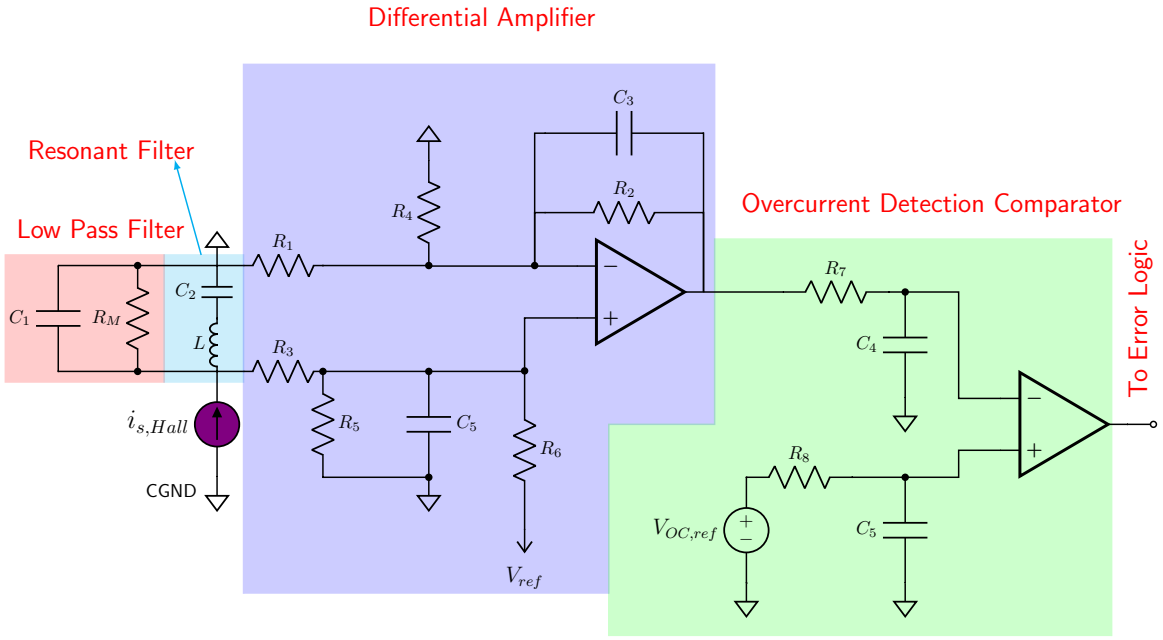


Figure 4.11: Hall sensor's signal conditioning filter circuitry.

As it will be shown shortly, repetitive SC testing can cause a SC type II across the GS when the DUT fails, a quite stressful event for the GS and the D_1. Then the current's rate of change depends on the ratio of the dc-link voltage and the stray inductance, meaning questionable response of the current transducer. Therefore, a new programmable gate driver over I^2C is additionally investigated, offering additional features, such as the desaturation protection method, two level turn-off, soft-off, etc.

The desaturation protection method is not analytically covered here, since it is a mature topic and the reader should refer to [81] for further details. Since the GS is composed of two parallel connected IGBTs, the desaturation method is designed based on the half maximum allowable current, namely 400 A. The total sum of voltages include the on-state voltage drop at 125 °C of the GS, a resistor, and two series connected diodes to the collector of GS. A charging current flows through this path when the desaturation protection is inactive. Utilization of this protection method during repetitive SC testing can be challenging, since the parasitic loop inductance, an unknown parameter during the design, can cause additional issues. Figure 4.13 shows an example of unwanted trigger scenario and how to avoid it by increasing the filter time. The DUT is an IGBT subject to SC pulse. The moment the current rises rapidly, the GS exhibits an overvoltage owing to its parasitic inductance. The desaturation pin of the gate driver includes a zener diode in order to be protected from overvoltages, clamping close to 12.5 V. After the temporary overvoltage, the desaturation pin starts charging, since the GS voltage

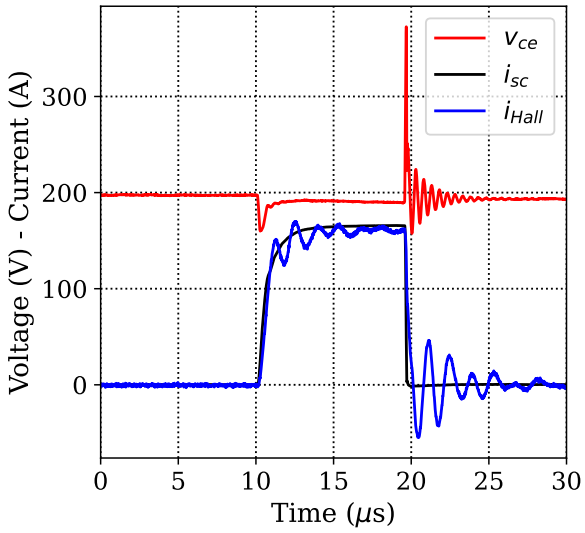


Figure 4.12: SC response of the Hall transducer of the first hardware prototype. The Hall signal is measured across R_M.

is such that sets the diodes to be reverse biased. The threshold voltage is programmed to 9.2 V and the filter time is around 1.2 µs, which eventually triggers the desaturation protection and the GS is turned off. In order to overcome this issue, the filter time is increased by getting the results of Figure 4.13b. However, this filter time increase results in a slower reaction in case of DUT failure.

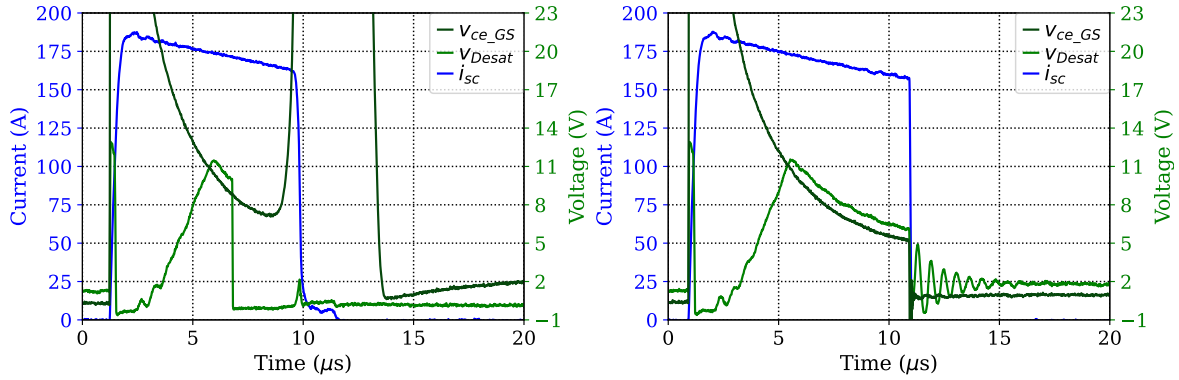


Figure 4.13: Desaturation detection method: (a) trigger scenario, (b) no trigger scenario.

A final example for a 350 A SC pulse with the maximum allowable filter time is depicted in Figure 4.14. It can be seen that the voltage in the desaturation pin is clamped until the voltage across the GS falls allowing the diodes to be forward biased again and consequently reducing the voltage. It is evident that this method under these conditions introduces considerable delays, rendering it ineffective. It should be pointed out that after the high current rate of change, the voltage across the GS would be expected to drop much faster, a phenomenon requiring further research. In a nutshell, this additional protection method can be used as redundant option, since the gate driver can be readily programmed to activate both or either one of the presented protection methods.

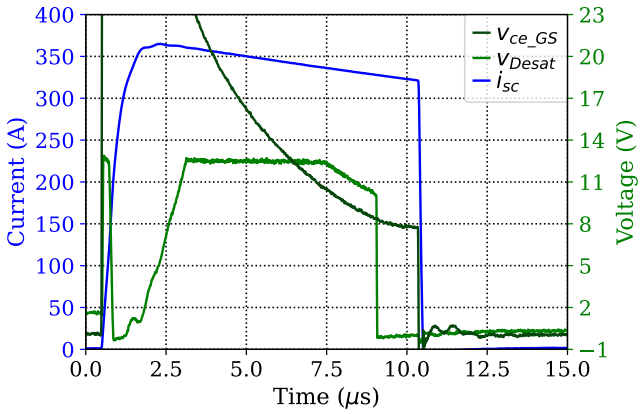


Figure 4.14: Desaturation method response with the maximum programmed filter time.

4.3.5 Comparator Based DP Execution

This section discusses the possibility to use a comparator in the view of executing DPs in a closed loop. The stress board is equipped with a comparator featuring a latch pin, which in turn is connected to a NAND gate. The inverting input of the comparator is tied to another DAC providing the reference signal, whilst the non-inverting input is connected to the current measurement after the differential amplifier, see Figure 4.11. The output of the comparator together with a reset signal coming from the μC are connected to the NAND gate, and subsequently its output is attached to the comparator's latch pin. When the comparator is triggered, its output transitions to the high voltage state, and, as a result the NAND gate latches the comparator's output. Then, this signal can be read by the μC by sending a DP event afterwards. Such a feature has not been practically implemented yet.

An experiment is conducted to indicate the challenges of this approach. Figure 4.15 illustrates an open loop DP under 900 V using a toroidal air core inductor as developed in chapter 5. The trigger level of the comparator is set to 150 A, as denoted by the dashed line. It can be seen that the comparator changes its state approximately 0.6 µs after the actual current reaches 150 A. At the point of comparator's high state, the load current rises up to 180 A indicating that stress tests with small loads are hard to be achieved with this method. On the contrary, scenarios with higher loads can be accomplished, since the current's rate of change is lower.

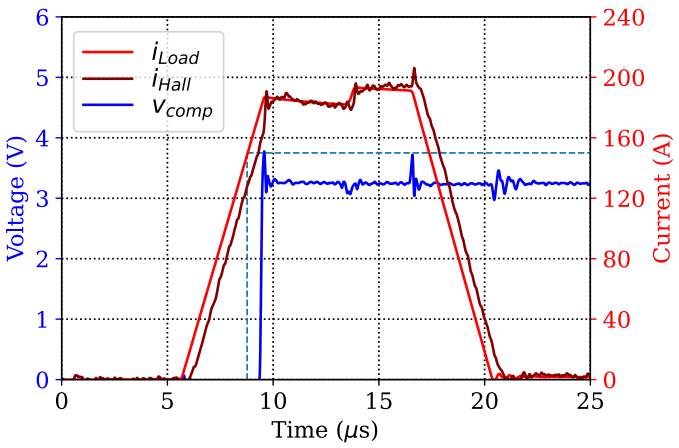
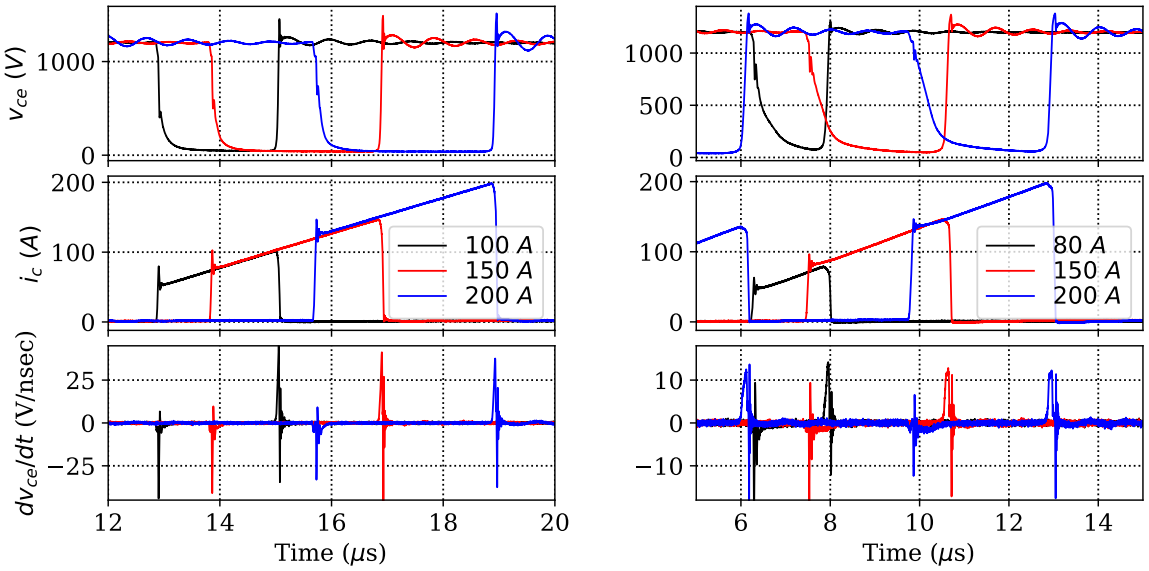


Figure 4.15: Open loop DP and comparator's response.

4.3.6 GS Design Considerations

This section discusses some design considerations of the latest employed IGBTs, fulfilling the target mission of the GS. One of properties of the latest hardware prototype is the full bridge based DP test, in which the GS is required to perform one single turn-off event. From thermal modelling point of view, the turn-off losses are characterized by using the GS as a DUT with its own freewheeling diode D_1. A DP is applied for different current levels and gate resistances at 1.2 kV, as depicted in Figure 4.16. This measurements is taken by using the second hardware prototype. According to manufacturer's data-sheet and application note [82], it is stated that these devices, at that development point, are not yet completely latch-up free at elevated temperatures and their voltage rate of change should be reduced. Therefore, the gate resistance should be increased, as a precaution measure, and as a consequence it causes the switching losses to increase, as listed in Table 4.4. It is decided to increase the gate resistance to 100 Ω in order to confine the voltage rate of change at around 10 V ns^{-1}. It is also clear that at zero current, there is a small amount of turn-on losses, attributed to the parasitic capacitances that need to be charged or discharged. These losses can also be included in the modelling for an enhanced performance, though, in this case they are excluded.



(a) (b)

Figure 4.16: DP execution for GS switching loss estimation - V_{ge} = 15 V, −5 V: (a) R_g = 20 Ω, (b) R_g = 100 Ω.

Some of the potential measurement errors in the switching loss estimation include the delay between the voltage and current probe, which can be deskewed as proposed in [28], and the time-control between the adjacent pulses, especially when the gate resistance increases since extra time is required for the voltage to reach its on-state value. Another effect is the self-heating during the DP, meaning that short pulses should be applied. In these experiments, a toroidal air core inductor is employed, as shown in chapter 5. Last but not least, the parasitic effects of the actual hardware arrangement, as developed in the last prototype, can result in slightly different switching loss profile and the measurements must be repeated again.

A potential research study could also test the long-term behavior of the GSs by using different gate

Table 4.4: Switching Loss Estimation at Different Current Levels

I_c (A)	E_{off} (mJ) - $R_g = 20\,\Omega$	E_{off} (mJ) - $R_g = 100\,\Omega$ †
50	1.38	4.06
80	3.2	7.54
100	4.125	-
120	5.39	13.15
150	7.77	17.29
180	10.38	22.36
200	12	25.82

† Used parameters in the simulation model chapter 3

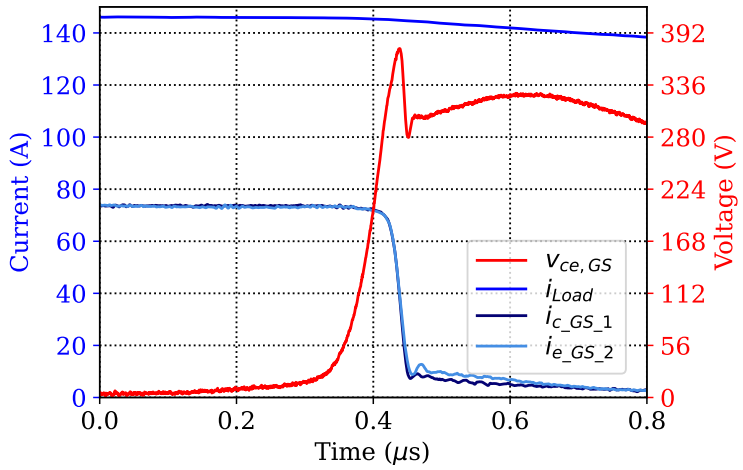
resistors, and their robustness against latch-up. This outcome could lead to further decreasing the switching losses and subsequently the temperature gradients.

The next design consideration is the symmetrical stress of the parallel connected IGBTs. To this end, certain design measures should applied such as, splitting the gate resistors to eliminate the risk of parasitic oscillations, use of a tight thermal coupling interface, and equalizing the parasitic emitter inductances [83]. Furthermore, any mismatches between the IGBT characteristics can cause dynamic current sharing imbalances.

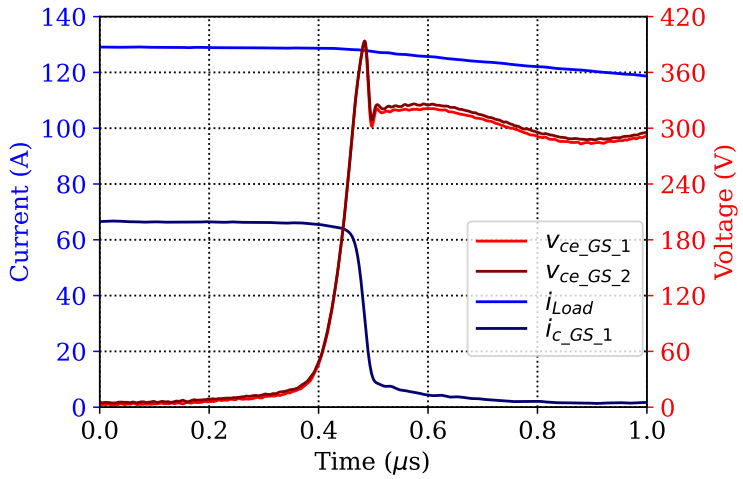
In order to evaluate the layout design in terms of the GS dynamic behavior, two operating points are considered. The first refers to 300 V and load current from 130 A to 150 A, as shown in Figure 4.17, and the second one to higher dc voltage at 900 V and 195 A, as shown in Figure 4.18. It is evident that the dynamic behavior exhibits adequate dynamic response with a minor discrepancy at the last scenario. It can be discerned that there is a slight difference between the parasitic emitter inductances, causing the manifested undershoot difference. Therefore, this deviation should be examined thoroughly, in the prospect of improving the dynamic current sharing during the switching event. Furthermore, additional experiments should be carried out during the practical implementation to test the performance at all possible operating points.

One of the most important tasks of the GS is to reliably withstand SC type II events when the DUT fails. In order to examine the GS behavior under this extreme condition, several destructive experiments take place. Figure 4.19a presents an indicative dynamic response immediately after the DUT's destruction. The measured current via the Rogowski coil is saturated approximately at 800 A due to its range limitations. However, the Hall signal, as measured across the measurement resistor, is able to follow up to the maximum oscilloscope's preset voltage window frame. It is obvious that the current possibly rises even beyond 2 kA, indicating a heavy stress across the GS and then D_1. During this experiment, the overcurrent limit is set to maximum, that is 400 A, and the gate-emitter voltage is reduced to 12 V. The Miller effect causes the gate voltage to additionally increase, and, as a result the current rises further. The trigger event occurs roughly 2 µs after the Hall signal reaches 400 A.

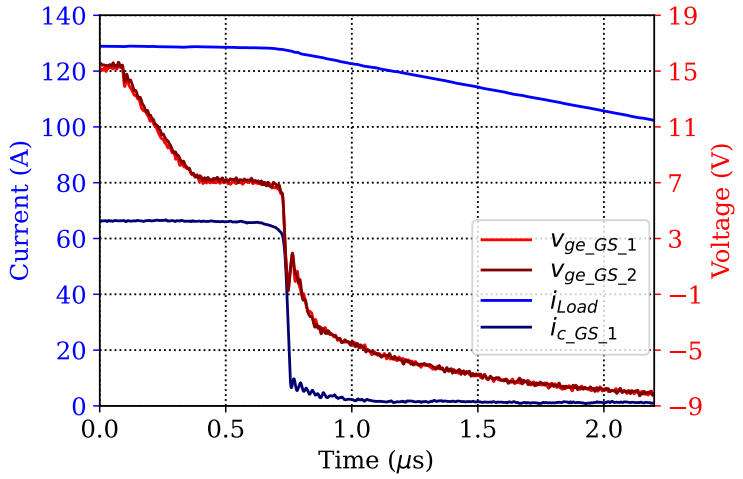
During the development of the last hardware prototype, certain measures are applied in the prospect of alleviating the stress on the GS during such a detrimental event. One major difference is that IGBTs with smaller transconductance are used in the view of getting smaller saturation current. Another feature is the two level turn-off provided by the new programmable gate driver with the intention of avoiding excessive overshoots at turn-off. The last feature is the use of clamping diodes so as to reduce the Miller effect. It is of paramount importance to ensure that the IGBT enters its saturation area first before turning it off, otherwise there is a high risk to cause a latch-up, as meticulously described in [3]. However, it should be mentioned that this phenomenon also depends on the device's technology.



(a)

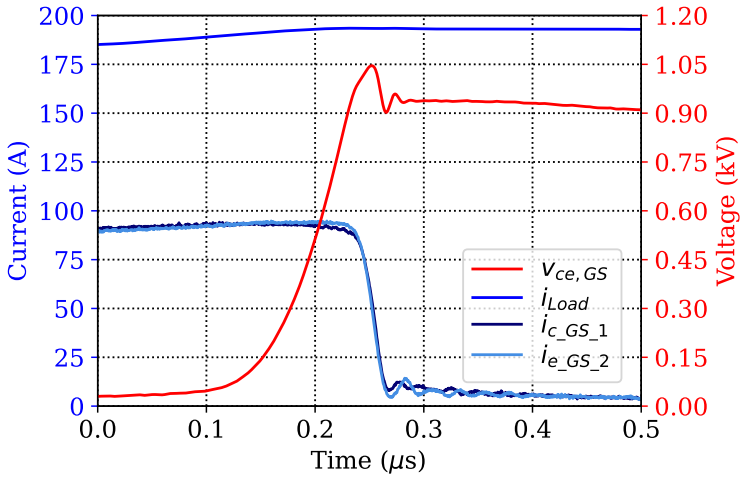


(b)

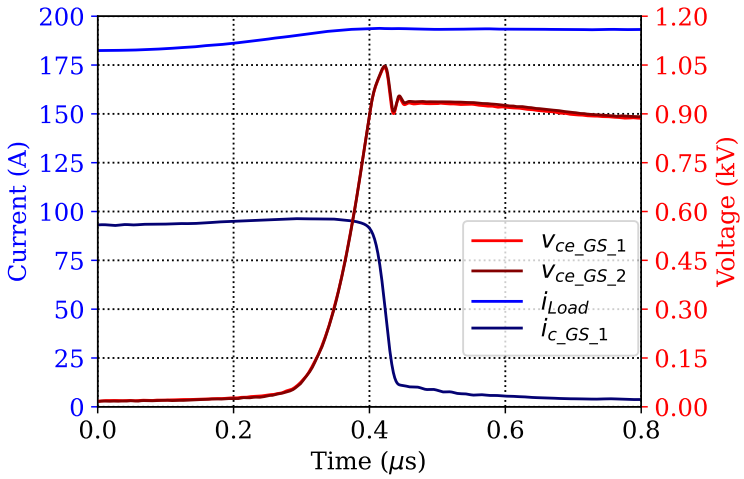


(c)

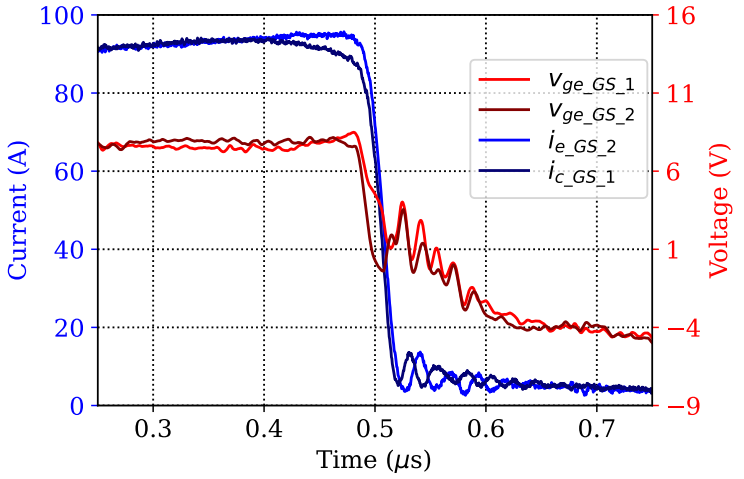
Figure 4.17: GS dynamic turn-off behavior under 300 V: (a) collector and emitter current of each IGBT at 150 A total load, (b) collector-emitter voltages at 130 A total load, (c) and gate-emitter voltages at 130 A total load.



(a)

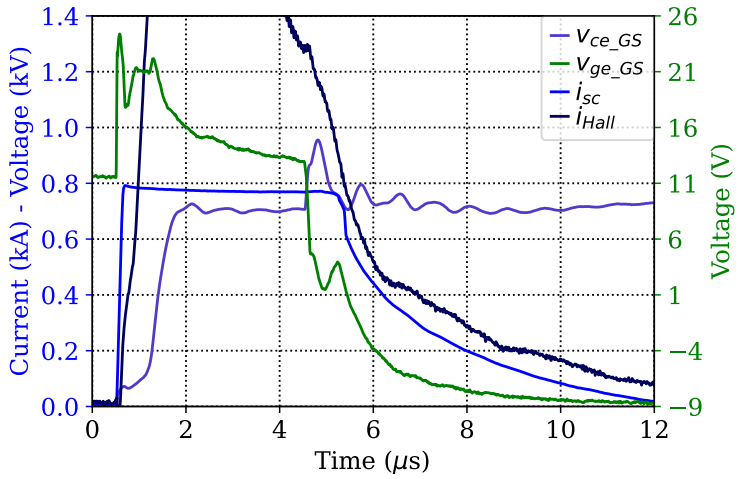


(b)

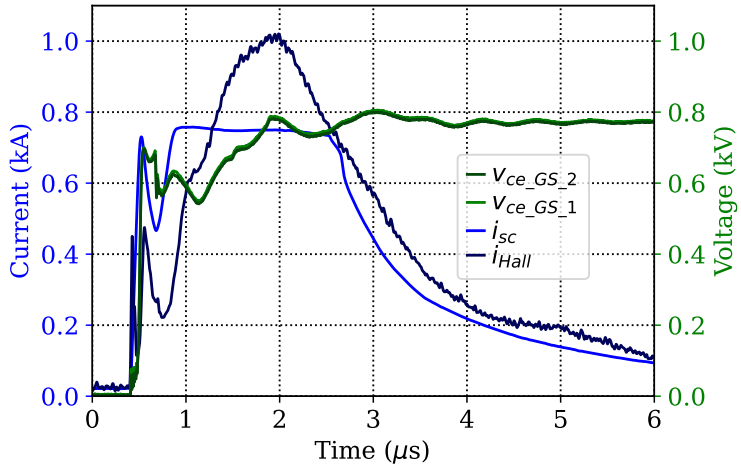


(c)

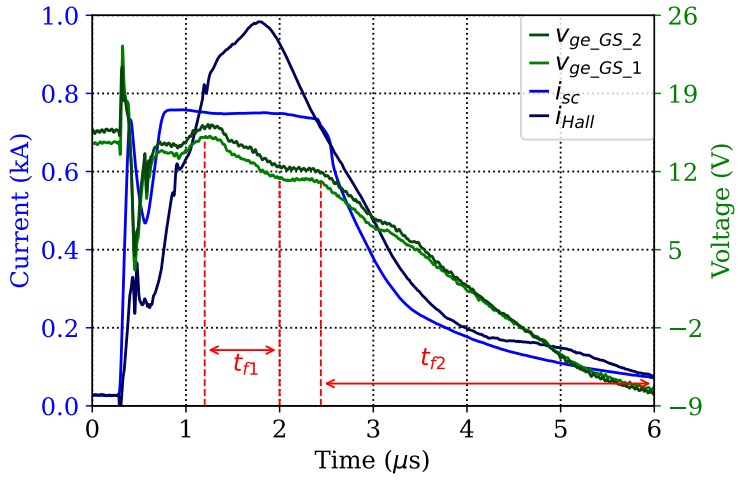
Figure 4.18: GS dynamic turn-off behavior under 900 V and 195 A total load: (a) collector and emitter current of each IGBT, (b) collector-emitter voltages, (c) and gate-emitter voltages.



(a)



(b)



(c)

Figure 4.19: SC type II across the GS at 800 V - Hall current is measured across the measurement resistor: (a) second hardware prototype, (b) third hardware prototype - collector-emitter voltages, (c) and gate-emitter voltages.

By introducing the new features, the SC type II response of the new IGBTs under identical conditions is illustrated in Figures 4.19b and 4.19c. At first glance, it is noticeable that the Rogowski coil (i_{sc}) is saturated again at a similar value. The Hall signal is also measured across the measurement resistor (R_M), showing a peak at roughly 1 kA. As the SC current rises rapidly, the collector-emitter voltage rises under two distinctive steps, as determined by the Miller capacitance. During this time interval, the feedback through the Miller capacitance injects a current to the gate. For this reason, there are clamping diodes provided, connected to the positive gate supply voltage to protect against high feedback gate voltages. However, this circuit also includes its own parasitic inductance, and therefore it needs special design attention. Moreover, ringing phenomena might occur due to the interaction between the parasitic inductances and capacitances, meaning that further research is required. In this case, the overvoltage is confined up to 23 V, which is smaller than the previous case and for shorter duration. At that point, the maximum SC current is also reached, which is not measurable with the employed equipment. Immediately after the collector-emitter voltage reaches its maximum, a short phenomenon occurs, named self-turn-off (STO) as analyzed in [84]. The gate voltages diminish at around 5 V and so does the current. Subsequently, the gate voltages return to their previous levels and the two level turn-off is initiated, meaning that the trigger signal has already transferred. The main objective of the two level turn-off is to initially limit the current to lower value by reducing the gate voltage at the first ramp stage, as denoted with the falling time t_{f1}. Then, there is a plateau region, in this case programmed to 11 V but the actual value is about 11.5 V. Finally, the last ramp stage is activated and the current falls to zero. It is evident that the introduced features improve the SC type II behavior. Last but not least, D_1 has to carry the remaining current when the GS's channel is off, assisting in the overvoltage reduction, and thus with the two level turn-off this burden is additionally relaxed.

Some other important facts regarding these experiments are the use of different DUTs, namely IGBTs of the same voltage class but different capabilities. This can partially affect the total SC impedance and the final response. Another observed difference is the offset between the two gate voltages in Figure 4.19c. This is mainly attributed to the dc gain inconsistency, as detected, of the probes and secondly any potential imbalances in the gate drive unit, which might need further investigation. Although the two level turn-off is fully programmable, the actual response can be affected by the loading conditions, namely gate charge, parasitic inductance, SC current and the gate resistance.

In principle, the use of different voltage class and technology devices can result in a dissimilar SC behavior, as already mentioned in chapter 2 and observed. Therefore, their long-term robust behavior under various operating points should be examined. Since the repetitive SC robustness under SC type II cannot possibly be studied with the present equipment, their robustness under SC type I and single pulse SC is evaluated by using the second hardware prototype, giving an indication of their ruggedness. To this end, two IGBTs are subject to repetitive SC testing and one is subject to single pulse SC test in order to determine its critical energy [53], as will be presented shortly.

4.3.7 Single and Two-Channel Stress Tests

This section demonstrates the prototypes' performance for the case study stress tests under single or two-channel parallel mode operation. Currently, all the condition monitoring is essentially executed off-line in the form of read-outs. All the used DUTs are either TO-247 3-pin or 4-pin discrete packages. Finally, the long-term ruggedness of the complete setup at different operating points is an ongoing procedure which could only partly be covered within this thesis due to limited testing time and resources.

UIS Test

In this section, two experimental examples are demonstrated, as conducted with the second hardware prototype , one for a superjunction Si MOSFET, as shown in Figure 4.20, and one for a SiC MOSFET as shown in Figure 4.21. The single pulse UIS experiments are conducted with a load of 53.4 µH, refer to chapter 5.

As for the Si MOSFET UIS test, the gate resistance is selected to 7.5 Ω and the gate voltage is preset to 15 V and −10 V. Figure 4.20a shows a single pulse UIS test where the input supply voltage is adjusted so as to achieve different avalanche energies, as given in Equations (3.9) and (3.10). By further increasing the energy, the device reaches a point of catastrophic failure as depicted in figure 4.20c. During this event, the peak current rises up to 87 A, after a 10 µs pulse. The overcurrent level is preset to 90 A, leading to 3 µs trigger time, owing to hardware delays. Apart from single pulse UIS tests, repetitive testing can be applied, as it is the main objective of the multi-channel system. A stress test scenario of two DUTs operating in parallel mode with two identical loads of 53.4 µH and 50.2 µH is presented in Figure 4.20b.

Regarding the SiC MOSFET UIS test conditions, the gate resistance is opted to 15 Ω and the gate voltage is set to 20 V and −5 V. The peak current reaches 138 A and the overcurrent is programmed to 150 A resulting in 2 µs trigger time. Such destructive tests not only should be interrupted quickly, but also the dissipated energy through the DUT should ideally be minimised for a post-failure analysis.

The already developed prototypes reveal that the available load space is relatively limited, which, in turn indicates that robustness tests with high loads are most probably ineffective to be achieved with the presented mounting options. They can only be applied externally, which is an unfavorable solution. Therefore, repetitive UIS tests with smaller loads are the most feasible solution. Last but not least, the practical implementation of the test system should include research to define the maximum achievable load given the available space.

SC Test

This section gives an insight about IGBT's SC behavior by utilizing the developed reliability stress test system, in particular the second hardware prototype. An experimental repetitive SC test of two IGBTs, stressed in parallel mode, is presented in figure 4.22a. The gate drive conditions for this example are set to 15 V and −5 V gate voltage and 15 Ω gate resistance. In order to avoid self-heating effects, the repetition frequency is reduced to 0.5 Hz. The SC pulses for each DUT are sequentially generated with 20.5 ms time delay. The overshoot of DUT_1 is larger, since the current is measured with the CP150 current probe, which requires a larger loop for proper connection. On the other hand, the current of DUT_2 is measured with the Rogowski coil. Under these conditions, the peak current reaches 350 A.

Figure 4.22b presents a single pulse SC robustness test where the gate voltage is preset to 16 V and after a successful SC turn-off of 440 A peak current, the device fails with a delayed failure mechanism, as reported and analysed in [53, 55]. The occurrence of this failure mode indicates that the critical energy is close to the applied energy under the specified conditions [53]. Numerical calculation yields approximately 8.2 J.

In order to competently extend the system's robustness to reliably perform repetitive SC tests at dc-link voltages up to 1.5 kV, the third hardware prototype employs IGBTs of higher voltage class, which can additionally support the full bridge based DP, as already mentioned. The IGBTs of the second hardware prototype are rated at 1.7 kV, and their switching capability is limited to 150 A, as stated in their data-sheet based on the RBSOA. Furthermore, their ability to withstand SCs close

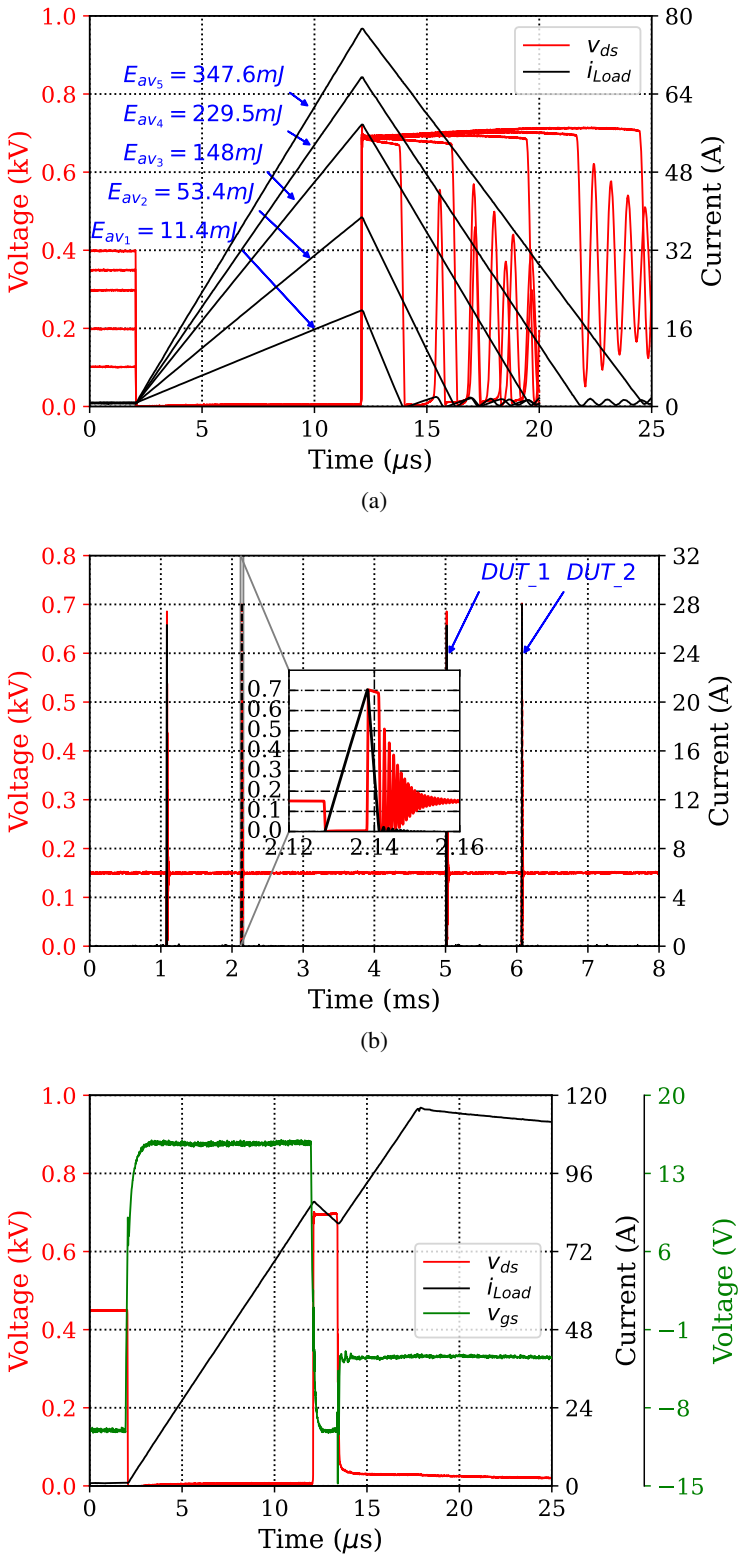
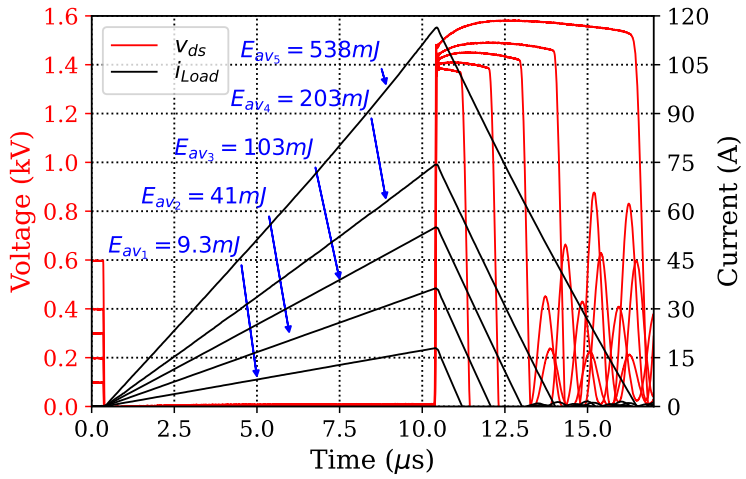
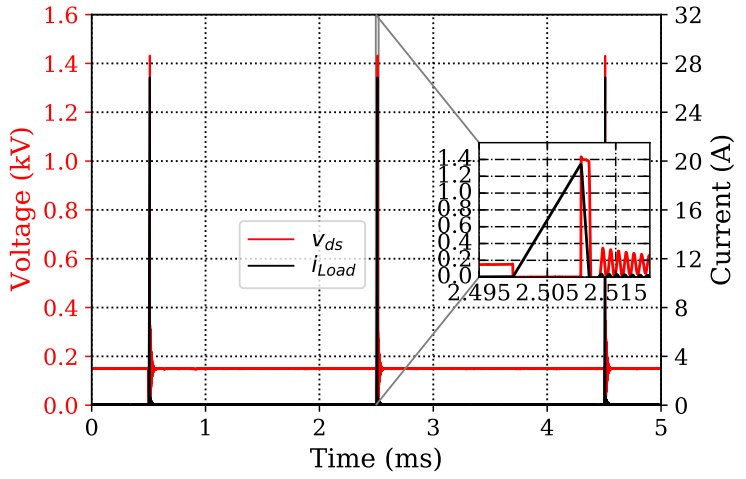


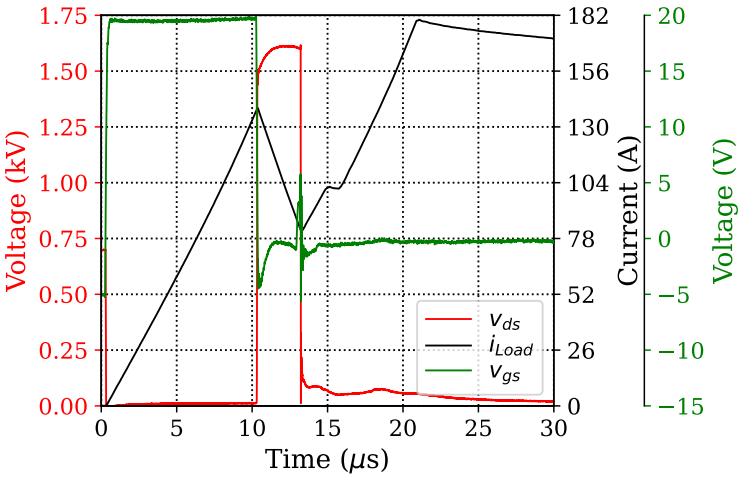
Figure 4.20: UIS test of a superjunction Si MOSFET: (a) single pulse UIS under different supply voltages, (b) repetitive UIS of two parallel DUTs with 250 Hz repetition frequency, (c) single pulse UIS failure.



(a)



(b)

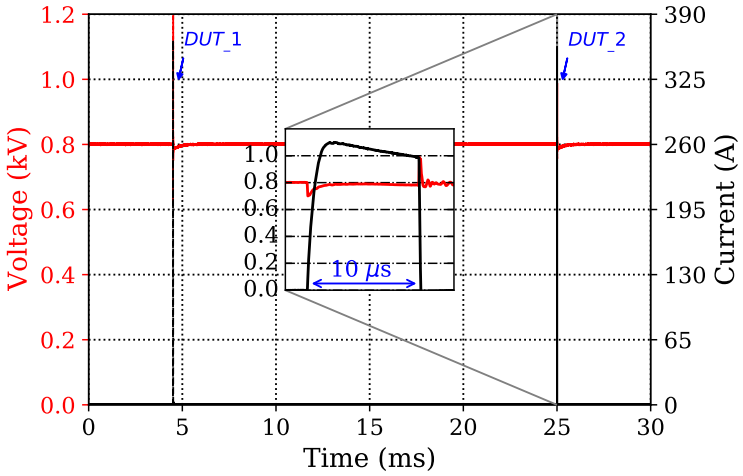


(c)

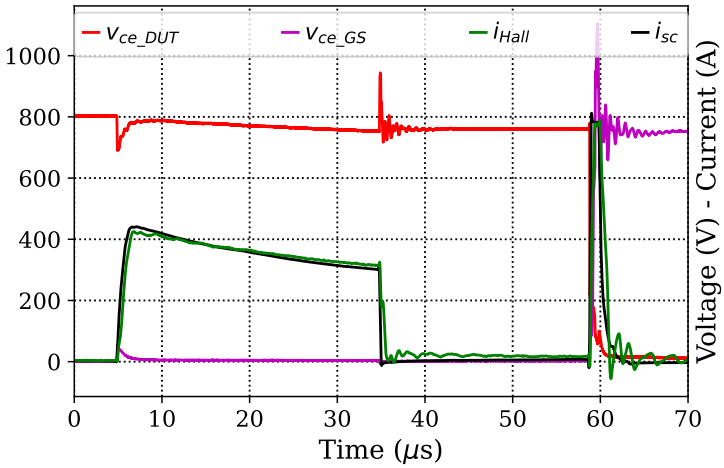
Figure 4.21: UIS test of a SiC MOSFET: (a) single pulse UIS under different supply voltages, (b) repetitive UIS of a single channel DUT with 500 Hz repetition frequency, (c) single pulse UIS failure and protection scheme reaction.

to their voltage limits is highly questionable. An additional fact for this system is that a solution with discrete IGBT packages is preferred over a module one due to its compact design. By taking into account these facts, repetitive SC are conducted for the assessment of the latest IGBTs, at the maximum dc-link voltage (1.5 kV), as shown in Figure 4.23a. The gate voltage is set to 13 V, limited by the current measurement range, and the gate resistance to 100 Ω, for slow switching reasons. The two devices has survived 120000 shorts under these conditions and due to the limited time at that point of the experiment, the test had to stop.

The critical energy for this device is in the range of 18.6 J, as estimated by the robustness test of Figure 4.23b. The IGBT fails after a successful SC turn-off of 40 µs and 480 A peak current. This failure event was not captured, as it happened outside the oscilloscope's time window. Therefore, the dissipated energy during the SC type II should be limited well below the critical energy, for an overall system reliability enhancement. As a last statement, it should be noted that this IGBT belongs to a voltage class above 1.2 kV and their SC capability might differ at different dc-link voltages and thus should be investigated further [3].

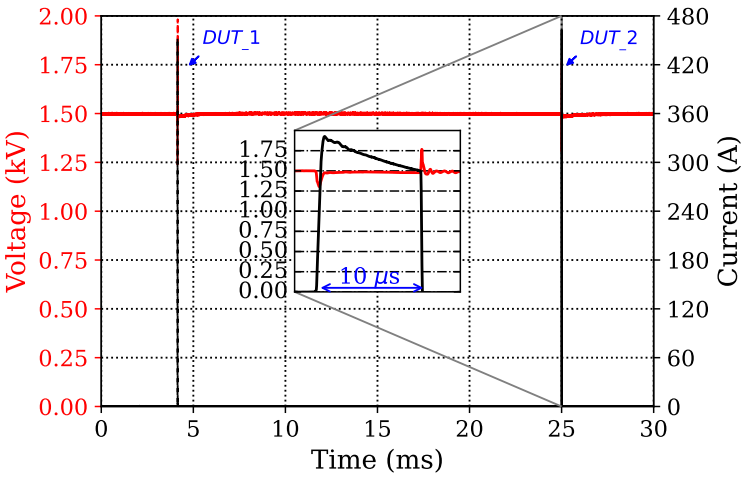


(a)

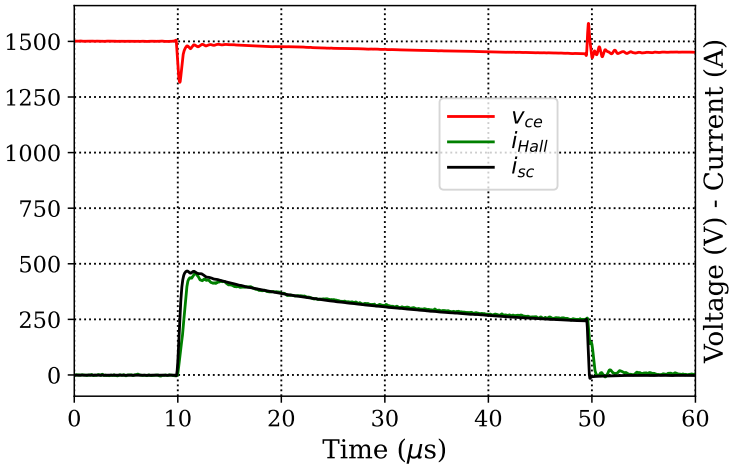


(b)

Figure 4.22: SC test of a 1.2 kV - 75 A IGBT: (a) repetitive SC test with 0.5 Hz repetition frequency, (b) single pulse SC robustness test.



(a)



(b)

Figure 4.23: SC test of a 3.6 kV - 50 A IGBT: (a) repetitive SC test with 0.33 Hz repetition frequency, (b) single pulse SC robustness test.

DP and SP Test

The last experimental section is devoted to repetitive DP and SP tests, as conducted by using the third hardware prototype. This includes the comparison between the standard DP and full bridge based DP, the critical timing issue of the latter concept in terms of proper DUT stress testing, the thermal performance of a two-channel test at higher dc voltage and finally a SP for a SiC MOSFET outside its SOA, as stated in its data-sheet. All the tests are conducted by using a Keysight 33622A waveform generator, since at that point the firmware for the μC was pending.

The first experiment compares the thermal performance between the standard DP and the full bridge based DP for a trenchstop IGBT of 600 V voltage class having a similar rated freewheeling diode D_2. The stress test conditions are selected as follows, the dc-link voltage is set to 380 V and the peak current is ramped up to 300 A using the toroidal air core inductor (see chapter 5) with 50 Hz repetition frequency. As for the gate drive conditions, the gate voltages are preset to 15 V, -5 V and the gate

resistance to 20 Ω. The outcome is depicted in Figure 4.24, the DP time intervals are based on the nomenclature of chapter 3 as follows, $t_{r1} = 15$ µs, $t_{f1} = 4$ µs and $t_{r2} = 3$ µs. All the oscilloscope channels are downsampled for a proper data acquisition and subsequent data processing. The thermal images are captured with a forward looking infrared (FLIR) E8 series camera, placed inside the safety box with no user direct accessibility. Beneath the stress board, there is a fan of sufficient diameter to cool down the board, consuming roughly 12 W. The airflow direction is denoted with an arrow. The load's rms current is already 27 A for the standard DP and 8.2 A for the full bridge based DP test. Therefore, the use of the standard DP causes the load, the D_2 and the GS to be heated up more under the same stressing conditions, validating qualitatively the simulation analysis.

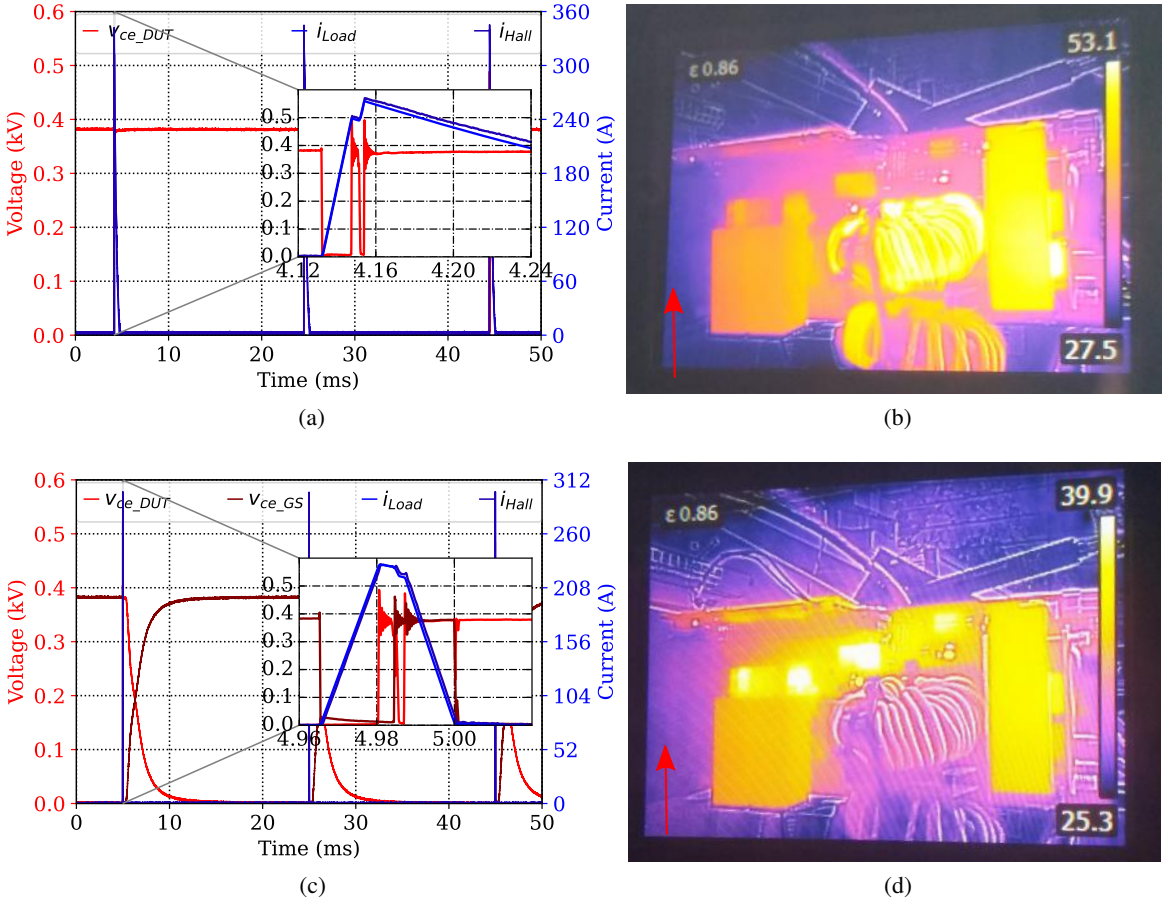


Figure 4.24: Comparison of standard DP and full bridge based DP: (a) standard DP test, (b) thermal image of standard DP test, (c) full bridge based DP, (d) thermal image of full bridge based DP.

Concerning the full bridge based DP test, its critical timing should be noted, that is the moment of turning off the GS and turning on the DUT. In this specific case the current temporally flows through the diodes, which can result in inappropriate stressing. Therefore, certain delay might require to avoid this phenomenon, as shown in Figure 4.25 by increasing slightly the energy losses. Lastly, it can be discerned that when the full bridge is in its off-state, the dc-link voltage is gradually applied across the GS and simultaneously the DUT's voltage falls to zero.

The next experiments are performed at 800 V and 920 V dc voltage under two-channel parallel op-

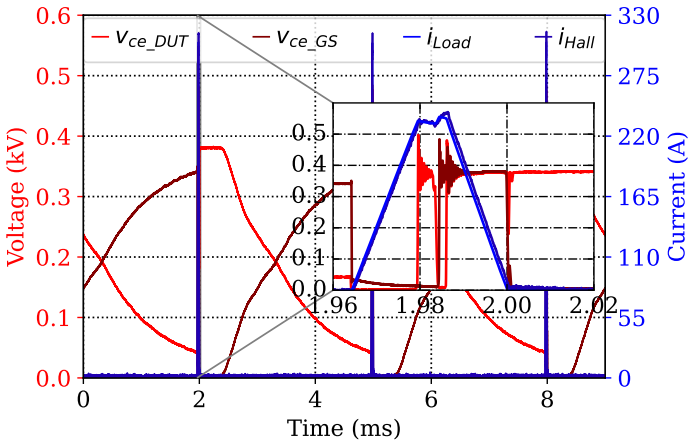


Figure 4.25: Introduction of 1 µs delay to properly stress the DUT.

eration. The results are presented in Figure 4.26, each channel holds a trechstop IGBT rated at 1.2 kV, 75 A and having a similar rated clamping diode. Both tests are executed under 200 Hz repetition frequency. One channel has the air core inductor and the other one the toroidal air core inductor as a load. In the latter experiment case, auxiliary fans are positioned on the DUT's heat sink to enhance the cooling capability consuming roughly 2 W each, as shown in Figure 4.24d. The load's rms current of each case is 13.57 A and 8.5 A, respectively. The positive gate voltage is adjusted to 20 V so that the DUT can turn on properly at high loads. Alternatively, the gate resistance can be decreased. The current decrement during the first falling time is 6 A and 4 A, respectively. The hottest part of the system is the DUT as expected.

The last experiment refers to a SP test of a SiC MOSFET, rated at 1.2 kV, in the view of testing its robustness outside the SOA, as mentioned in chapter 3. In this case study, the dc voltage is precharged to 1.3 kV and the peak current reaches 112 A, which is more than twice its nominal current. The transient response together with the setup temperature gradients, as captured by the FLIR, are illustrated in Figure 4.27. A pulse of 1.7 µs duration is applied to the toroidal air core inductor to reach the desired peak current. The peak voltage goes up to 1.37 kV during the turn-off event. The repetition frequency of this stress test is set to 500 Hz. The temperature gradients seem to be low, and, as a result the repetition frequency can be further increased on condition that the case study failure mechanism is not greatly affected by the temperature rise.

4.4 Conclusion

This chapter summarizes the different design steps and methodologies followed over the course of this thesis, in the view of realizing a scalable stress test system by maintaining a relatively compact design so that it can fit into a subrack system and finally to reap its benefits. However, several trade-offs arise, for example by shrinking the spatial area allocated for the load, there can be a detrimental effect for UIS tests requiring high inductances, but otherwise it can assist in the acceleration of repetitive DP testing as highlighted. Furthermore, reducing the impedance of the SC test needs improved component placement, as emphasized. This might come into contradiction with the modular goal, namely load and DUT interface, impinging another limit.

From performance point of view, it is demonstrated that the system can handle stress tests up to 1.5 kV and 400 A. However, its long-term capability could only partly be assessed over the course of

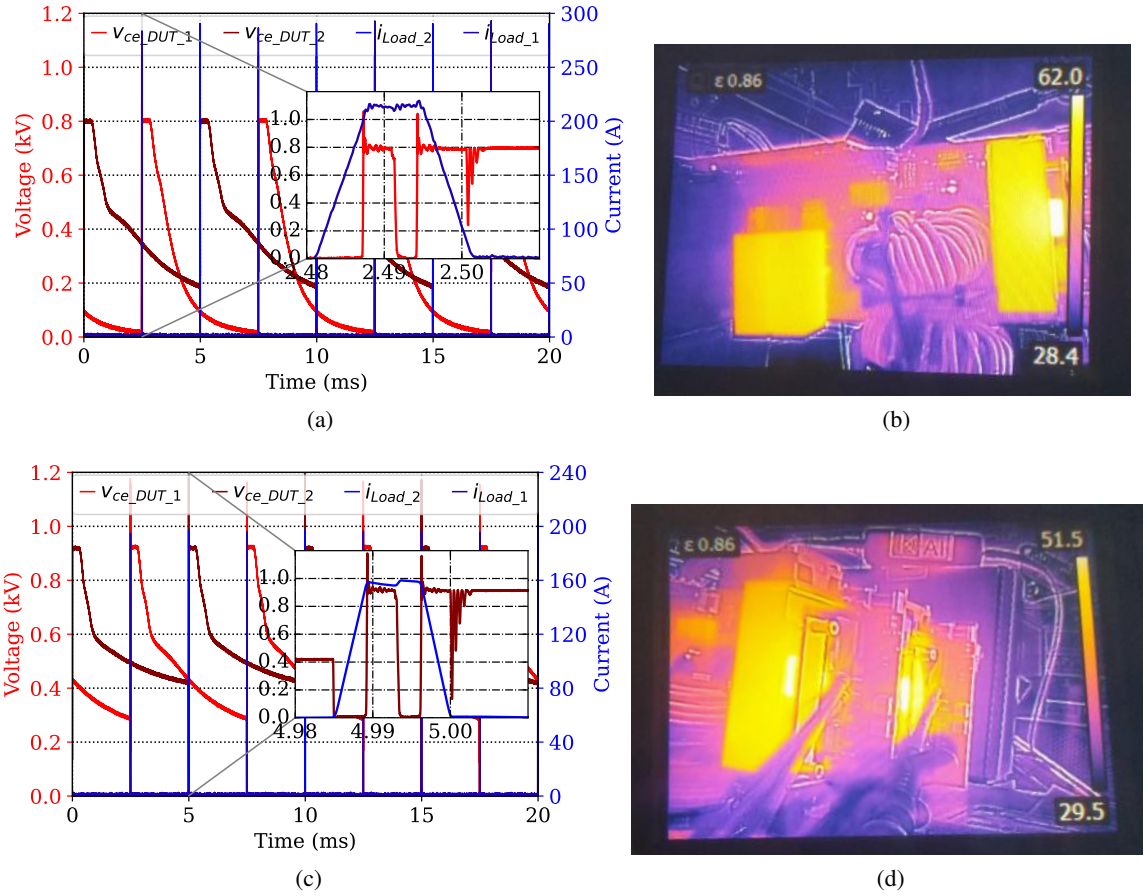


Figure 4.26: Full bridge based DP test ($R_g = 20\,\Omega$, $V_{ge} = 20\,\text{V}, -5\,\text{V}$): (a) two-channel 800 V - 290 A (load current measured with Hall sensor), (b) single channel thermal image, (c) two-channel 920 V - 195 A (load current measured with Rogowski coil), (d) two-channel thermal image.

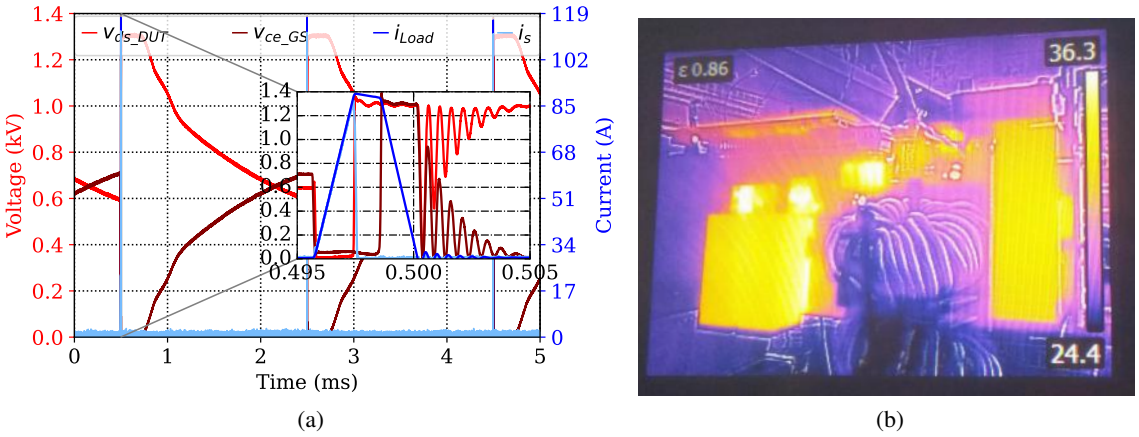


Figure 4.27: SP Test of a SiC MOSFET ($R_g = 20\,\Omega$, $V_{gs} = 15\,\text{V}, -5\,\text{V}$) : (a) single channel transient response, (b) thermal image.

this thesis, meaning that further long-term reliability tests should be applied. It is also of paramount importance to highlight that the introduced DP concept, apart from its valuable benefits, presents a critical point during its execution under the ideal pulse generation. Particularly, in a multi-channel operation, it is more laborious to tune this critical point for each channel due to the involved tolerances. Therefore, the gate drive conditions of both active switches (GS and DUT) should be well modelled in order to accurately turn on the DUT and subsequently turn off the GS and thus to avoid unintended stress test conditions.

Chapter 5

Magnetics-Load Interface

5.1 Introduction

The accomplishment of a given stress profile requires the implementation of suitable loads, namely inductors. Therefore, the development of magnetic components constitute an indispensable part of this stress test system. The design of magnetics mainly focuses on the DP stress test, due to higher challenges such as the high peak currents. In general, several factors of the magnetic components can influence the system's behavior in long or short term, such as saturation, stray magnetic field, volume, dielectric withstand capabilities, parasitics, losses, etc. However, an in-depth analysis is beyond the limits of this thesis and the reader should follow the relevant cited references. Additionally, the connection of the magnetic components through the load interface has an impact on the stress test preparation in terms of time. Therefore, different solutions introduce trade-offs which are discussed and highlighted for further evaluation.

At the beginning of this chapter a mathematical background related to the different inductor solutions is presented. The following sections show the designed inductors for each prototype by pointing out their advantages and disadvantages. Finally, a discussion takes place regarding their utilization within the stress test system and certain emerging research topics are highlighted.

5.2 Mathematical Background

5.2.1 Air Core Inductor

The realization of high peak currents in the range of 400 A in a relatively compact design can be solely achieved by air core inductors. The great benefits of air core inductors are the absence of saturation due to the excitation current and the absence of core losses. On the contrary, the drawbacks are the stray field and the necessity for a higher number of turns for achieving a given inductance which can have an influence on the winding losses and the self-resonance frequency.

The cross section of a multilayer coil wound on a circular bobbin is depicted in Figure 5.1. This type of air core inductor can be constructed relatively easy and its inductance is estimated by an empirical equation, known as the Wheeler's formula, and given in Equation (5.1) [85], where L is the inductance in μH, r, w, and h are the average radius, width and height of the coil in meters respectively, and N is

the number of turns.

$$L = \frac{4000r^2N^2}{127(6r+9h+10w)} \tag{5.1}$$

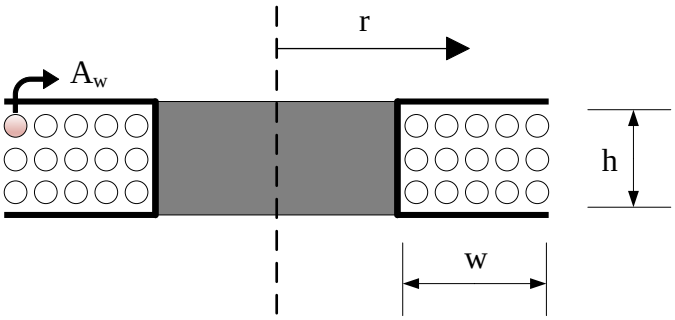


Figure 5.1: Cross section of air core inductor.

Based on the given geometry and a desired inductance, one can set an optimization problem for a minimum dc-resistance, which is solved in [85]. The optimal solution is given in Equation (5.2).

$$\begin{aligned} R_{dc,min} &= \frac{5.395\rho L^{3/5}}{\gamma^{1/5}A_w^{4/5}} \\ l_{min} &= \frac{5.395A_w^{1/5}L^{3/5}}{\gamma^{1/5}} \\ N &= \frac{0.6656\gamma^{1/5}L^{2/5}}{A_w^{1/5}} \\ h &= \frac{\sqrt{10\gamma A_w N}}{3\gamma} \end{aligned} \tag{5.2}$$

Where A_w is the cross section area of the used wire, γ is the winding filling factor, ρ is the resistivity of the wire material and l is the length of the wire (l=2πrN). By substituting the optimal number of turns into the height, it yields in Equation (5.3).

$$h = \frac{0.86L^{1/5}A_w^{2/5}}{\gamma^{2/5}} \tag{5.3}$$

Likewise for r and w in Equations (5.4) and (5.5) entails that r = 1.5h and w=0.9h for the optimum coil geometry.

$$r = \frac{l_{min}}{2\pi N} = \frac{1.29L^{1/5}A_w^{2/5}}{\gamma^{2/5}} \tag{5.4}$$

$$w = \frac{NA_w}{\gamma h} = \frac{0.774L^{1/5}A_w^{2/5}}{\gamma^{2/5}} \tag{5.5}$$

5.2.2 Toroidal Inductor

A toroidal inductor and its geometry are shown in Figure 5.2. The inductance of this type of inductor is calculated by applying the Ampere's law around a circle of radius r as denoted by the dashed line. Then the magnetic flux density is expressed as a function of the radial distance Equation (5.6) [86].

$$\begin{aligned} \oint \vec{B} \cdot d\vec{l} = \oint B \cdot dl = B2\pi r = \mu_o \mu_r NI \\ B = \frac{\mu_o \mu_r NI}{2\pi r} \end{aligned} \tag{5.6}$$

Subsequently, the magnetic flux can be obtained by integrating over the rectangular cross section Equation (5.7).

$$\Phi = \iint \vec{B} \cdot d\vec{S} = \int_{r_1}^{r_2} \frac{\mu_o \mu_r NI}{2\pi r} h dr = \frac{\mu_o \mu_r NIh}{2\pi} \ln(\frac{r_2}{r_1}) \tag{5.7}$$

Finally, the inductance is derived as the ratio of the total flux over the applied current, given in Equation (5.8).

$$L = \frac{N\Phi}{I} = \frac{\mu_o \mu_r N^2 h}{2\pi} \ln(\frac{r_2}{r_1}) \tag{5.8}$$

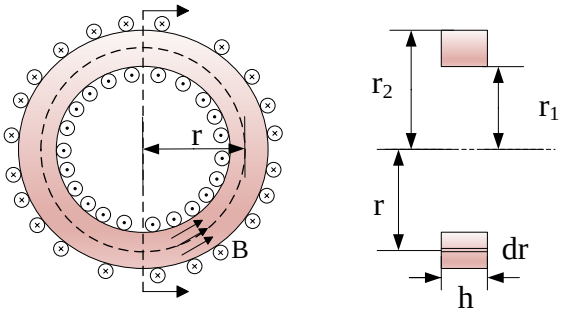


Figure 5.2: Geometry of a toroidal inductor with a rectangular cross section.

A simplified version of Equation (5.8) is employed in many applications, in case $r_1 \gg r_2 - r_1$, yielding Equation (5.9), where A_e is the cross section of the toroid.

$$L \approx \frac{\mu_o \mu_r N^2 A_e}{2\pi r_1} \tag{5.9}$$

5.3 Load Design

For each hardware prototype different inductors has been constructed in order to evaluate the hardware performance. Therefore, each section describes the realised inductors for the case study prototype.

5.3.1 First Hardware Prototype

For the assessment of the first hardware prototype, an air core inductor of 180 µH is set as a design target. An enamelled magnetic wire with cross section A_w= 2.081 mm^2 is employed. By substituting

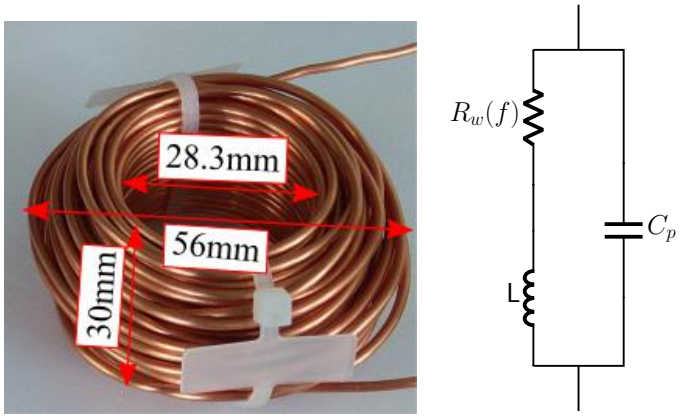
in Equation (5.2) for the optimal solution gives Equation (5.10).

$$\begin{aligned} N &= 72.72\gamma^{1/5} \\ h &= \frac{12.96}{\gamma^{2/5}}\,\text{mm} \\ r &= \frac{19.45}{\gamma^{2/5}}\,\text{mm} \\ w &= \frac{11.66}{\gamma^{2/5}}\,\text{mm} \end{aligned} \tag{5.10}$$

Assuming a filling factor $\gamma = 0.8$ yields:

$$\begin{aligned} N &= 70 \\ h &= 14.17\,\text{mm} \\ r &= 21.26\,\text{mm} \\ w &= 12.75\,\text{mm} \end{aligned}$$

Therefore, the outer diameter is OD=55.27 mm and the inner one is ID=29.77 mm. Based on the available bobbins in the laboratory, the constructed inductor ended with 84 number of turns, by totally filling the bobbin across the height, as illustrated in Figure 5.3a. It is a 5 layer inductor, in which the last number of turns are not distributed uniformly across the height of the bobbin. Based on the obtained geometry, Equation (5.1) gives an inductance of 184.5 µH.



(a) (b)

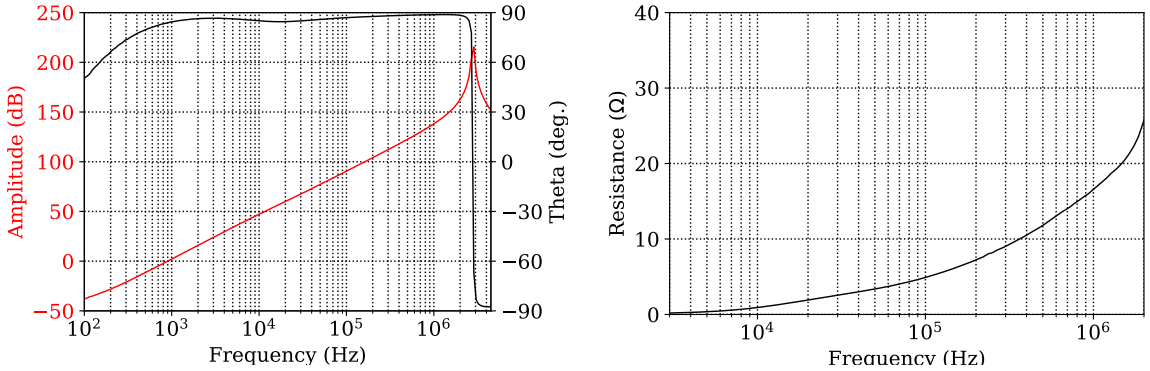
Figure 5.3: First hardware prototype: (a) geometry of air core inductor (r=21.075 mm, w=13.85 mm, h=30 mm), (b) equivalent lumped model [87].

For the measurement of the acquired inductance an Agilent 4294A precision impedance analyzer is employed. The small signal frequency response is depicted in Figure 5.4. The inductance is estimated at low frequencies around 1 kHz where the effects associated with the parasitic capacitance and ac-resistance are negligible, as shown in Figure 5.3b. An inductance of 175.3 µH with a dc-resistance of approximately 95 mΩ is obtained. The parasitic capacitance is estimated based on the self-resonance frequency, occurring at 2.867 MHz. By neglecting the effect of the ac-resistance around the resonance

frequency, it can be calculated in Equation (5.11) [88].

$$C_p = \frac{1}{\omega_{res}^2 L} \tag{5.11}$$

Consequently, it is roughly C_p=17.58 pF. It should be noted that the inductor is relatively loosely wound, due to the fact of increased space between adjacent layers. Furthermore, the majority of stored electric energy is concentrated between successive layers as highlighted in [89, 90], explaining the relatively low acquired capacitance regardless of the high number of turns.



(a) (b)

Figure 5.4: Small signal frequency response: (a) amplitude($|\vec{Z}_m|$)-phase(θ), (b) ac-resistance (Q-factor error influences the accuracy around the self-resonant frequency).

As far as the winding resistance is concerned, it can be extracted from the impedance analyzer measurement following the methodology presented in [88]. The small signal impedance measurement is given in Equation (5.12).

$$\vec{Z}_m = R_m + jX_m \tag{5.12}$$

By substituting the equivalent lumped model of Figure 5.3b and solving for R_w yields in Equation (5.13).

$$R_w(\omega) = \frac{1}{2C_p^2\omega^2 R_m}\left(1 - \sqrt{2LR_mC_p^2\omega^3 - 2R_mC_p\omega + 1}\sqrt{-2LR_mC_p^2\omega^3 + 2R_mC_p\omega + 1}\right) \tag{5.13}$$

The final result is plotted in Figure 5.4b, it can be seen that the resistance increases to a noticeable extent even at lower frequencies in the range of 10 kHz. In principle, the winding resistance's dependency on frequency is attributed to skin and proximity effect, and, as a result the current does not flow uniformly within the wire. The outcome is reasonable since a single magnet wire is used.

The relation between the DP and the introduced energy losses of the load are not covered in this thesis. However, it should be emphasized that the repetition frequency is mostly retained to low frequencies in the range of few kHz depending on the stressing conditions, hence the spectrum of the current is also confined at low frequencies as well as the ac-resistance. Nevertheless, the switching events might cause the development of high oscillations adding some high frequency spectrum components of low amplitude. A potential impact of a high ac-resistance may occur during the DP execution, specifically the moment of the DUT off-state. The time domain effect of the high ac-resistance can

cause larger current drop during this interval. Such an approach is given in [91] for improved time domain transformer models.

5.3.2 Second Hardware Prototype

During the development of the second hardware prototype, it was set as a goal to design 50 µH loads. Two different types of inductors were designed, one with magnetic core and the other one with air core. The design area is confined to 65 mm × 65 mm × 70 mm as specified in the PCB layout. Furthermore, a Litz wire is used in order to reduce the ac-resistance. The following sections discuss the aforementioned solutions.

Air Core Solution

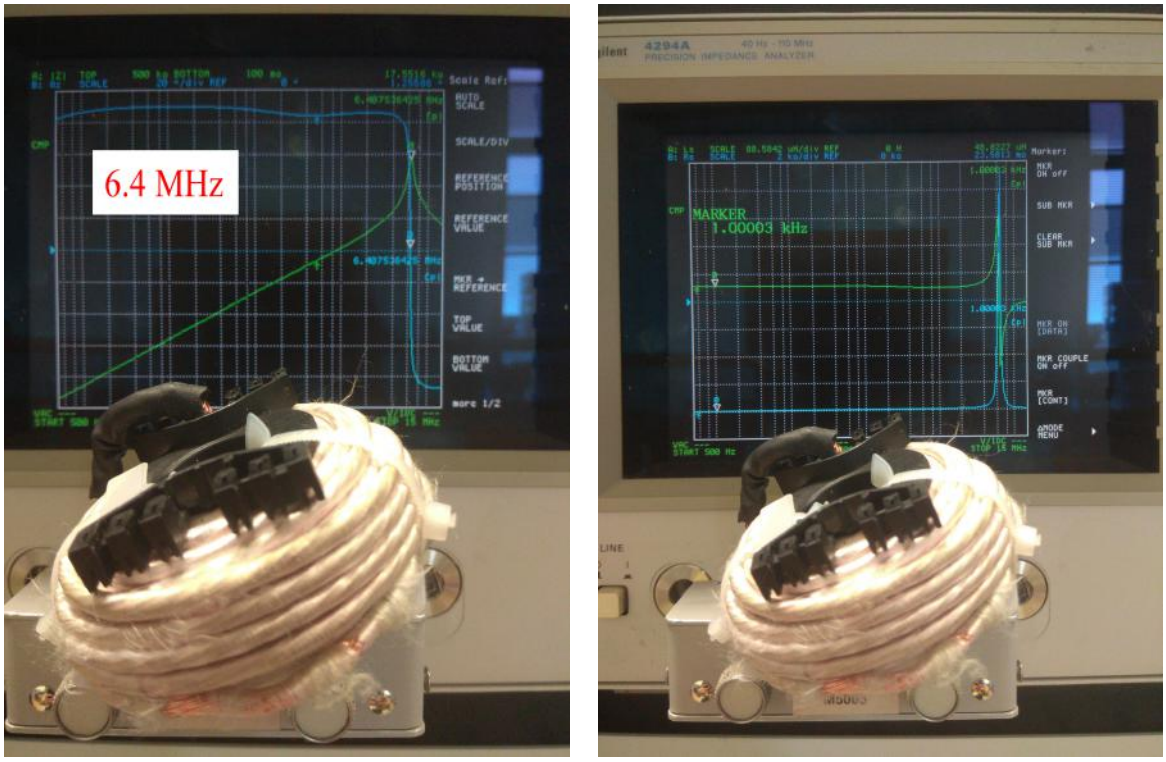
For the construction of the air core inductor an off-the-shelf bobbin together with an available Litz wire in the laboratory is employed. The Litz wire includes 50 strands of 0.355 mm diameter each, and thus A_w = 4.95 mm^2 total cross section area. It is worth mentioning that each strand has its own insulation and the bundling of these strands together leads to a smaller filling factor. The bobbin and the layout area itself impose some dimensional constraints, such as the outer diameter limited to OD = 65 mm, the inner to ID = 23 mm and the height to h = 23 mm. Table 5.1 shows the optimal solution for a filling factor of $\gamma = 0.7$ together with the constructed one. The realized inductor deviates from the optimal owing to imposed limitations. The minimum dc-resistance is calculated by using the resistivity of annealed copper at 25 °C, which is $\rho = 1.757 \times 10^{-5}\ \Omega$mm.

Table 5.1: Optimal and Suboptimal Solution

	Optimal	**Implemented**
N	34	42
h(mm)	16.36	23
r(mm)	24.55	22
w(mm)	14.72	21
l(m)	5.26	5.8
R_{dc}(mΩ)	18.68	20.58

The small signal frequency response of this coil is depicted in Figure 5.5. The self-resonance occurs at 6.4 MHz, from which can be deduced by evaluating Equation (5.11) that the parasitic capacitance is C_p = 12.7 pF. Figure 5.5b shows an $L_s - R_s$ measurement in order to approximate the actual inductance. The outcome gives around L = 48.8 µH and dc-resistance close to 23.5 mΩ.

At this point, some of the potential error sources in the impedance measurement should be mentioned as described by an application note of Keysight in [92]. Initially, an open and short compensation should be applied so that fixture residuals impedances can be deducted from the DUT impedance measurement. For magnetic core inductors an auto level control (ALC) function should be activated because they exhibit non-linear magnetization characteristics, and, as result a constant current is injected through the DUT. Another source of error might occur when the DUT is an air core inductor, resulting in eddy currents in the fixture itself. Last but not least, the Q-factor measurement accuracy is crucial, especially for high Q-inductors which can cause significant deviation of the absolute value. It should be noted that remote data reading for most cases was not possible due to bridge imbalance errors during the reading process attributed to the Q-factor error.



(a) (b)

Figure 5.5: Small signal frequency response of the air core inductor: (a) self-resonant frequency - 6.4 MHz, (b) at 1 kHz, inductance of 48.8 µH and $R_{dc} \approx 23.5\,\text{m}\Omega$.

Magnetic Core Solution

For the design of the magnetic core inductor two different types of magnetic cores from Magnetics® are evaluated. Both types are powder cores with distributed air gap. One of the design criteria is the high saturation flux density leading to high flux (FeSi) and Kool Mμ®(FeSiAl) composition alloys presenting 1.5 T and 1 T saturation flux density respectively. The latter core material is 4-6 times less expensive than the former material according to manufacturer. Moreover, Kool Mμ® shows slightly less core losses than the high flux core. The strongest benefit of the high flux material is its saturation level which is required for reaching high peak currents.

The relative magnetic permeability is selected to μ_r=14, providing the maximum saturation levels. In general the magnetomotive force should be sustained low, meaning that both the current and the number of turns need to be kept low. In this case the number of turns can be reduced by stacking more cores. Therefore, two toroidal cores are stacked together in order to reduce the number of turns and thus the magnetomotive force. The dimensions of the toroidal cores are as follows OD = 63 mm, ID = 31.7 mm and h = 26 mm. The toroid's cross section is not an ideal rectangle, however, the manufacturer provides the cross section A_e = 360 mm^2 and the average magnetic path length l_e = 144 mm. Consequently, Equation (5.8) is not accurate enough to determine the number of turns. Additionally, Equation (5.9) is also not accurate since the thickness of the toroid is by no way smaller than the internal radius. In this case, a more accurate approach is to take the average magnetic path

length, and, as a result the number of turns can be estimated by Equation (5.14).

$$N = \sqrt{\frac{Ll_e}{2A_e\mu_o\mu_r}} \tag{5.14}$$

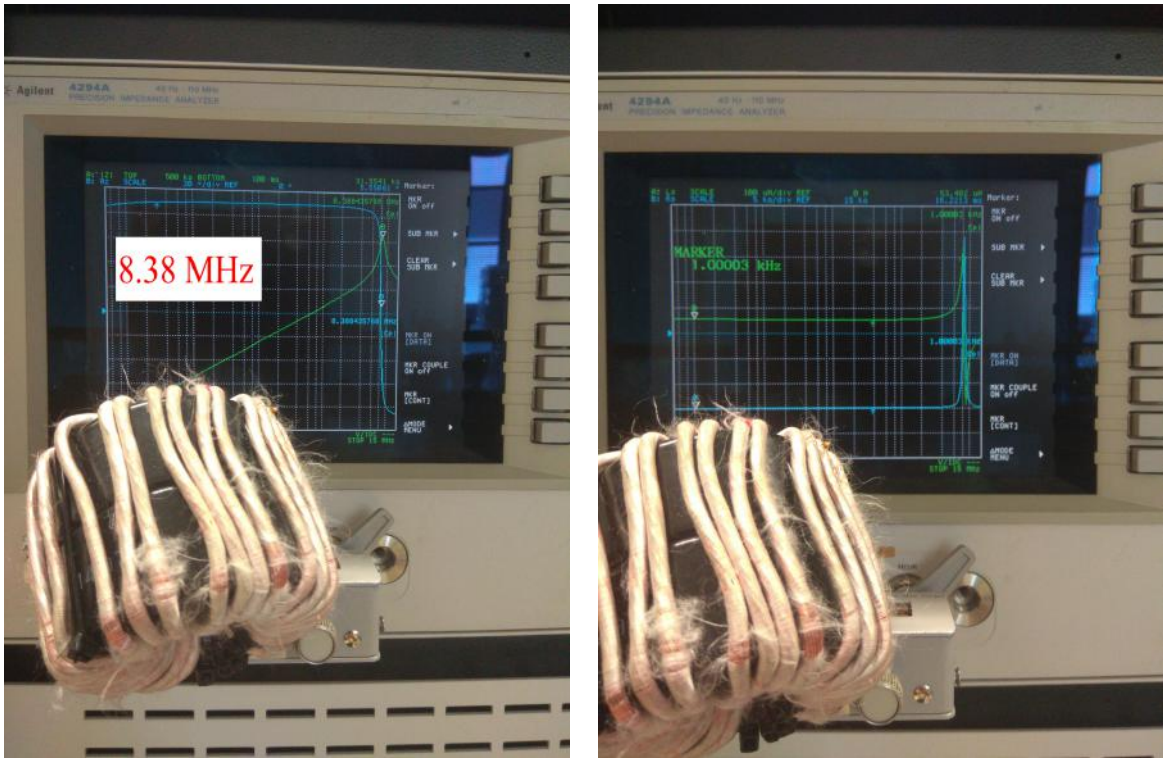
By substituting the known parameters, the number of turns are N $\approx$ 24.

By assuming an ideal winding factor the minimum attainable dc-resistance is calculated in Equation (5.15), where $\rho = 1.757 \times 10^{-5}\,\Omega$mm (at 25 °C), $l_{per_turn} = 135.3$ mm and A_w the same as that of the previous air core inductor design.

$$R_{dc} = \frac{\rho N l_{per_turn}}{A_w} = 11.52\,\text{m}\Omega \tag{5.15}$$

The final design is presented in Figure 5.6 with its small signal frequency response. This inductor is a single layer inductor with self-resonant frequency $f_{res} = 8.38$ MHz, yielding a parasitic capacitance of $C_p = 6.7$ pF. It can be seen that the actual dc-resistance is larger than the minimum one due to the non-ideal filling factor. The initial inductance for this design is L = 53.4 µH.

As for the high flux magnetic core a slightly different approach is followed. Each core is wound separately and then the final two inductors are connected in series. The final design yields an inductor with N = 23 of inductance L = 50.2 µH, parasitic capacitance $C_p = 7$ pF and dc-resistance measured at 1 kHz approximately $R_{dc} \approx 18.5\,\text{m}\Omega$ due to individual winding.



(a) (b)

Figure 5.6: Small signal frequency response of the magnetic core inductor (Kool M$\mu^{®}$): (a) self-resonant frequency - 8.38 MHz, (b) at 1 kHz, inductance of 53.4 µH and $R_{dc} \approx 16\,\text{m}\Omega$.

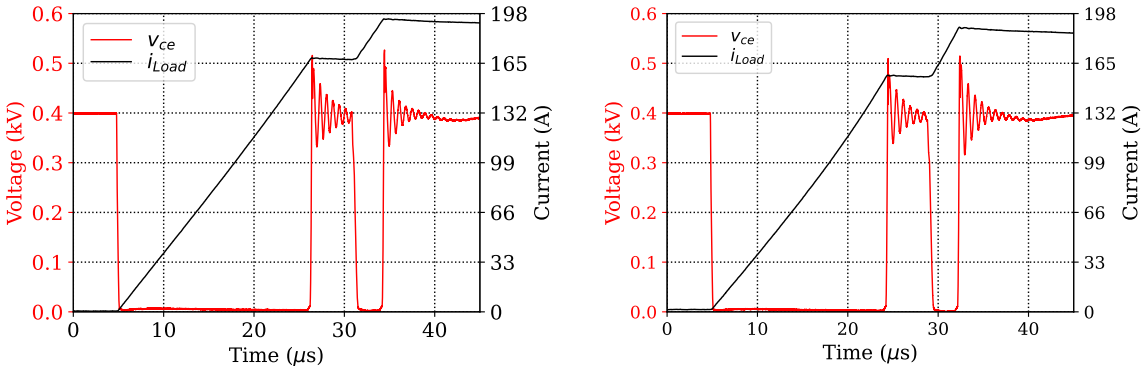
(a) (b)

Figure 5.7: Inductor location on the stress board: (a) air core inductor, (b) high flux inductor (884 g weight).

Pros and Cons of the Implemented Inductors

The location of each inductor on the stress board is determined by the forced air flow (cooling) and the stray magnetic field regarding the air core inductor. Figure 5.7 shows the final location of each inductor on the second hardware prototype stress board. As for the air core, its magnetic flux axis is placed parallel to the board in order to alleviate the influence of the stray field on the PCB and the surrounding components. This orientation offers better cooling capability, since the air can easily pass through the inner of the toroids.

The single layer design compared with the seven layers of the air core gives smaller parasitic capacitance which reduces the stress on the DUT. This capacitance is added to the parasitic capacitance of PCB, diode and DUT which affects the channel current during switching events because of the voltage gradients, as also elaborated in [93].



(a) (b)

Figure 5.8: Saturation current level: (a) high flux inductor, (b) Kool Mμ®inductor.

The magnetic core inductors should be also evaluated in terms of their ability to sustain peak currents without saturation. In order to test it, a single DP is executed at 400 V, as shown in Figure 5.8. Regarding the high flux inductor, the DP includes the following time intervals: 21 µs on-state, 4 µs off-state and 3 µs on-state, while the Kool Mμ®inductor has 19 µs on-state, 4 µs off-state and 3 µs on-state. The inductance is estimated by evaluating Equation (5.16), where Δt is the case study time interval,

ΔI the current difference in the case study time interval, and V_{dc} the applied dc voltage.

$$L \simeq \frac{V_{dc}\Delta t}{\Delta I} \tag{5.16}$$

The dc voltage is assumed to be constant during the DP. During the first on-state the ΔI is 165.2 A and 152 A for the high flux and the Kool Mμ® respectively. Hence, the inductance is estimated to be 50.8 µH and 49.98 µH, indicating that the Kool Mμ® inductor starts saturating. During the second on-state time interval the inductance is estimated to be 46.45 µH and 37.7 µH, demonstrating that the high flux inductor can carry peak currents up to 200 A and the Kool Mμ® up to 150 A before their saturation occurs.

Concerning the ac-resistance of the two coils, it is shown in Figure 5.9 as extracted from Equation (5.13). By qualitatively evaluating the graph, it is evident that the ac-resistance of both coils starts increasing at higher frequencies compared with the first hardware prototype inductor in Figure 5.4b due to the Litz wire. When the proximity losses start dominating, the ac-resistance of the air core inductor starts increasing at lower frequencies, since it is a seven layers coil. On the other hand, the magnetic core inductor exhibits better performance due to single layer construction.

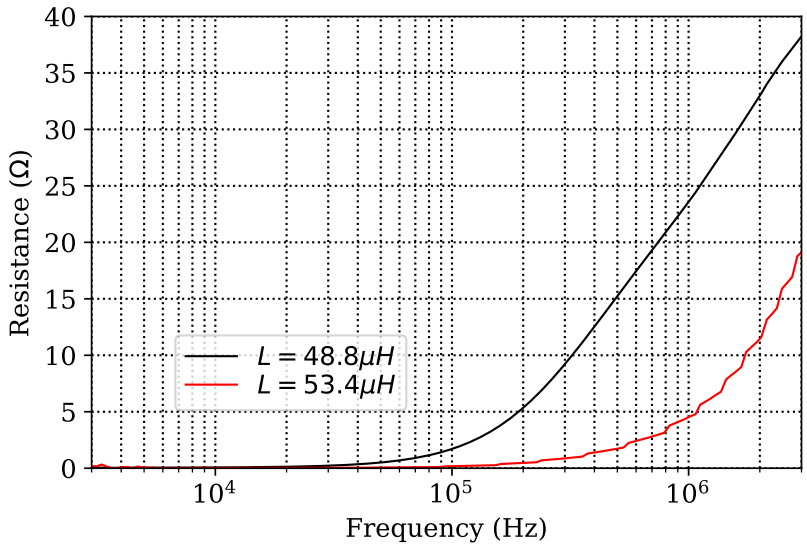


Figure 5.9: Ac-resistance of the constructed inductors.

It should be emphasized that the ac-resistance of the magnetic core inductor includes the core losses, which are reflected in the impedance measurement contributing to the real part, as highlighted in [88], shown in Figure 5.10. Therefore, Equation (5.13) gives the effective series resistance (ESR) for magnetic core inductors. The small signal core losses are estimated with the Steinmetz equation, yielding Equation (5.17), where V_e is the effective volume 51 800 mm^3 [88]. The ac-excitation current is 20 mA and the constants α, β and k are provided by Magnetics®. The accuracy of the Steinmetz model is greatly reduced at low frequencies where the complex permeability model provides more solid results. On the contrary, the Steinmetz model is more reliable at higher frequencies [88]. Last but not least, the core losses in the large signal analysis will have a considerably different profile.

Such an analysis is not covered in the context of this thesis and is left as a future study topic.

$$R_{c,eff} = 4V_e k_1 \hat{I}^{\beta-2}$$
$$k_1 = k f^{\alpha} \left(\frac{L}{N2A_e}\right)^{\beta} \tag{5.17}$$

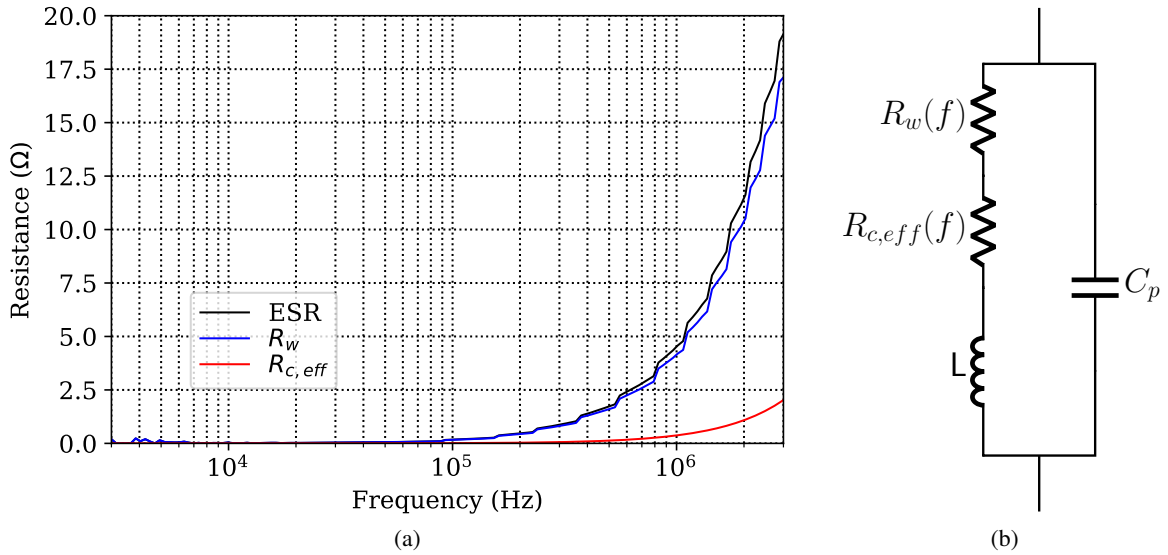


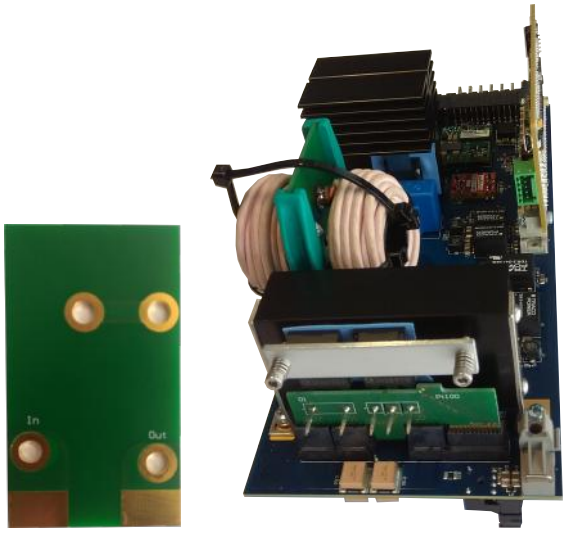
Figure 5.10: Winding resistance of the the Kool Mμ®inductor: (a) ac-resistance, (b) equivalent lumped model including the core resistance (normally represented in parallel, its series reflection to the measurement is highlighted here).

Finally, a crucial topic for a safe design is the voltage difference between adjacent turns. In general, a multilayer inductor can experience larger voltage differences especially between different layers, which has to be withstood by the insulation of the employed wire. For example in [89], different winding schemes are presented where the optimal winding scheme, called bank, minimizes the voltage difference between adjacent turns. Nevertheless, the realization of such scheme is strenuous and can be affected by the core shape as well.

5.3.3 Third Hardware Prototype

As has been already mentioned, the main purpose of the DP stress test is to study the behavior of the power devices under hard switching conditions. Hence, the self-heating effects due to conduction losses should be reduced, ideally minimized. Based on this rationale, the loads should be reduced so that the conduction intervals can be shrunk. Additionally, an edge connector is introduced instead of a screw-based load interface, consuming less time for the connection. Another detrimental effect is the stray field of the air core and therefore an alternative solution is also discussed in this section by introducing toroidal air core inductors.

Taking into consideration the aforementioned facts, 10 µH inductors are designed which can be connected in series within the load interface as shown in Figure 5.11. This flexibility enables the possibility to design dedicated inductors in the available design area. There are also card guides offering extra mechanical and electrical support between the boards for an enhanced connection.



(a) (b)

Figure 5.11: Third hardware prototype: (a) load board (40 mm × 70 mm), (b) card guides and load connection.

Toroidal Air Core Inductor

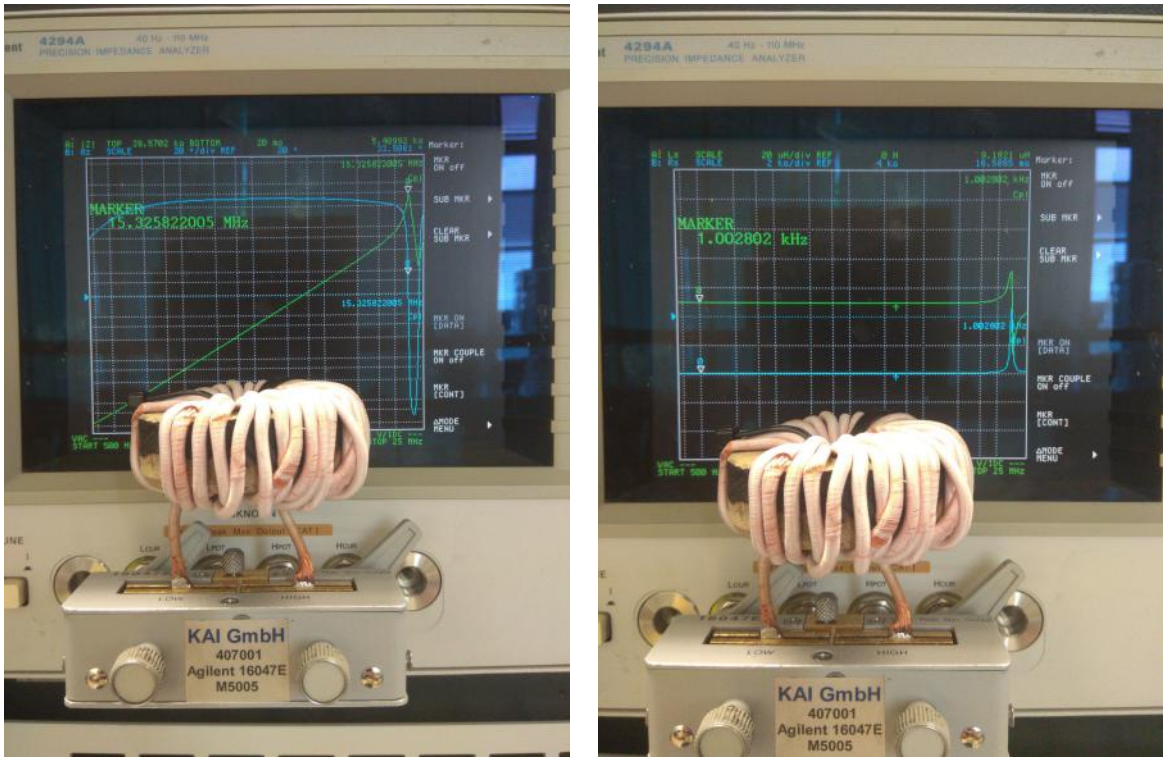
The construction of the toroidal air core inductors is realized by employing a wooden bobbin, having OD = 60 mm, ID = 25 mm and height h = 18 mm. Since the cross section is rectangular the required number of turns for a 10 µH can be found from Equation (5.8). The results gives a rounded number of 56 turns. A different type of Litz wire is used for these coils, having 990 strands of 71 µm diameter each, and thus $A_w = 3.92\,\text{mm}^2$ total cross section area. The window area of this coil is 491 mm^2, while the total cross section area of the Litz wire including the wrapping is 7.07 mm^2, which barely can fit the required number of turns.

Experimentally a 9.2 µH inductor was implemented having 41 turns. it is worth mentioning that a bank winding technique was attempted but the geometry of the bobbin and the high number of turns affected the final winding arrangement. It should be stressed that the attained flux per turn, linked with the surface per turn, and the mutual inductances are quite complicated to predict, a topic which is beyond the scope of this thesis. However, there are advanced methods in literature, for example as presented in [94] for estimating air core inductances of various geometries. The small signal frequency response and the inductor itself are depicted in Figure 5.12. The parasitic capacitance is roughly C_p = 11.7 pF.

Air Core Inductor

For the air core inductor a similar approach is followed, as previously shown. The implemented and the optimal solutions are listed in Table 5.2 for a filling factor $\gamma = 0.7$. The same bobbin has been employed again, giving a final inductance L = 9.4 µH, measured with impedance analyzer as shown in Figure 5.13. By evaluating Equation (5.1) with the dimensions of the implemented coil gives an inductance of 9.5 µH showing excellent agreement with each other. The parasitic capacitance of this coil is roughly C_p = 10.4 pF, based on its self-resonance frequency (4-layer).

The ac-resistance for each inductor is illustrated in Figure 5.14. The smaller wire cross section



(a) (b)

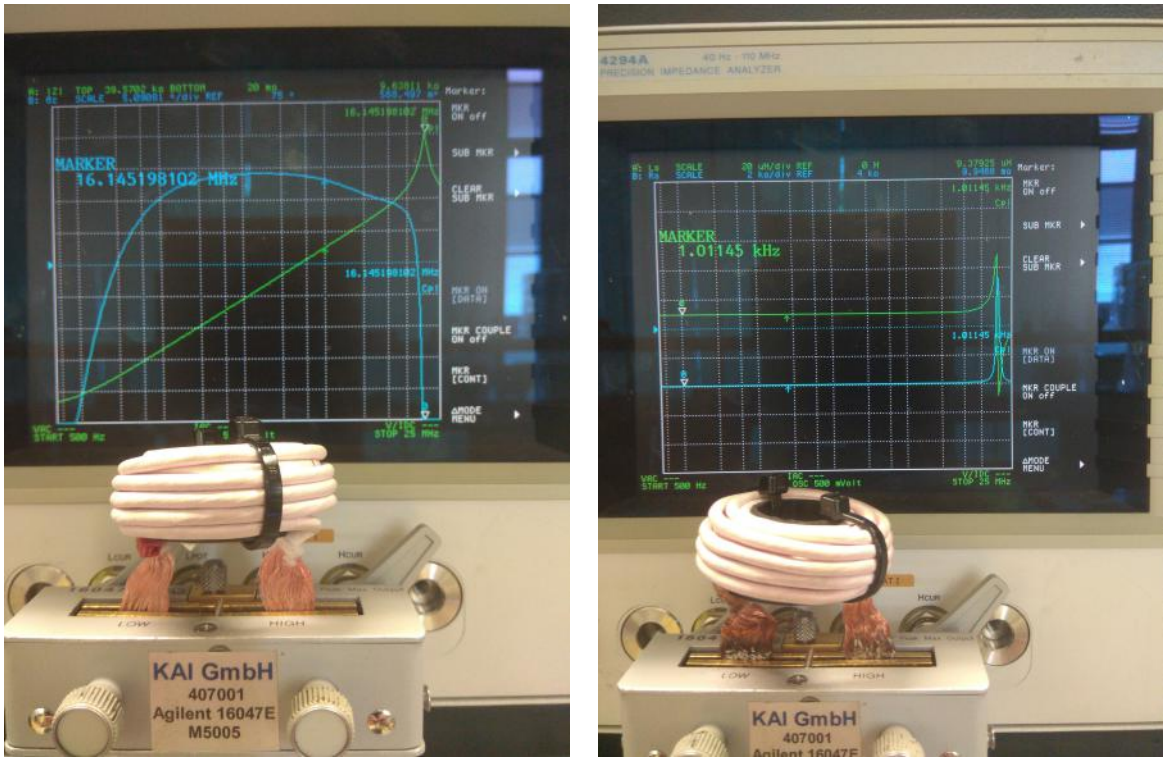
Figure 5.12: Small signal frequency response of the toroidal air core inductor: (a) self-resonant frequency - 15.3 MHz, (b) at 1 kHz, inductance of 9.2 µH and $R_{dc} \approx 16.6\,\text{m}\Omega$.

Table 5.2: Optimal and Suboptimal Solution

	Optimal	**Implemented**
N	19	19
$h(\text{mm})$	10.8	15
$r(\text{mm})$	16.2	17.75
$w(\text{mm})$	9.72	12.5
$l(\text{m})$	1.91	2.12
$R_{dc}(\text{m}\Omega)$	8.56	9.5

improves the ac-resistance in a broader range of frequencies compared with the previous air core inductor. Furthermore, the decreased number of layers probably assists in the reduction of the proximity losses. This is evident for the toroidal air core inductor, in which the field distribution results in a smaller ac-resistance. Even though the outcome is better by using thinner Litz wire, the cost of such a solution increases. Therefore, a trade-off between performance and cost arises, which is not addressed here.

Finally, two inductors are placed in a series connection of identical characteristics for each type. The total inductance of the two series air coils yields 19.6 µH, whilst for the toroidal air core inductors yields 18.4 µH. The air core presents a total parasitic capacitance C_p = 7.3 pF and the toroidal one C_p



(a) (b)

Figure 5.13: Small signal frequency response of the air core inductor: (a) self-resonant frequency - 16.1 MHz, (b) at 1 kHz, inductance of 9.4 µH and $R_{dc} \approx 9.9\,\text{m}\Omega$.

= 5.6 pF. The total mass of the toroidal inductors is around 323 g, roughly twice as that of the air core inductors 173 g. The result shows that the air core inductors are less bulky than the toroidal and have smaller dc-resistance. On the other hand, the toroidal coils exhibit better ac-resistance and potentially less stray field.

As for the stray field of each inductor, it is evaluated qualitatively by placing a passive probe in a closed loop above the inductor during a DP execution, shown in Figure 5.15a, so as to capture the induced voltage. Figure 5.15b indicates that the toroidal air core has negligible stray field at least in this direction. On the contrary, the air core inductor induces a voltage, which depends on the loop area, the magnetic density, angle and frequency. In case that the air core inductor influences the performance of adjacent circuits, it renders the toroidal air coil the sole problem solution.

5.4 Peak Current Estimation

The determination of a precise switching current is critical for this application and is influenced by several factors, such as the gate drive conditions, the load and the involved propagation delays. This section discusses the possibility of applying a pretesting routine so as to determine the peak current. However, its feasibility might limited by the microcontroller and other facts, as shortly analyzed.

The main idea of this routine is to oversample the load current, sensed by the Hall sensor, during a predefined DP or single pulse, and then numerically calculate the current derivative. By considering

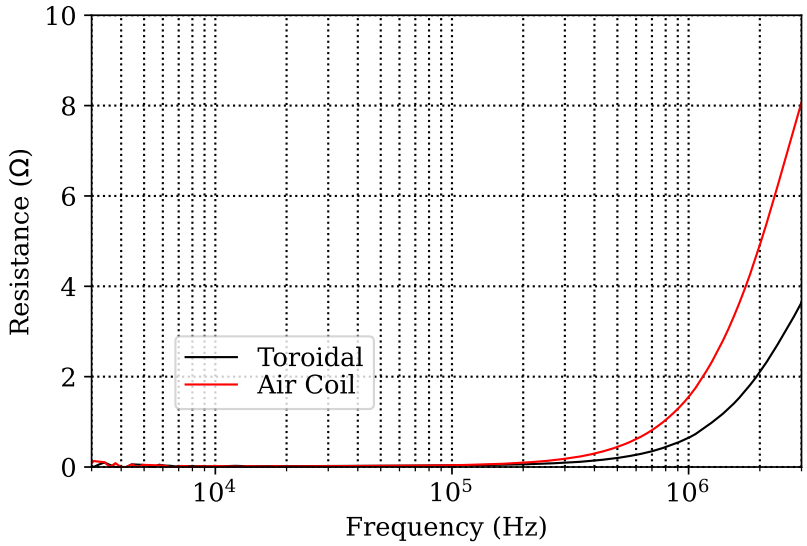


Figure 5.14: Ac-resistance of the toroidal and air core inductor.

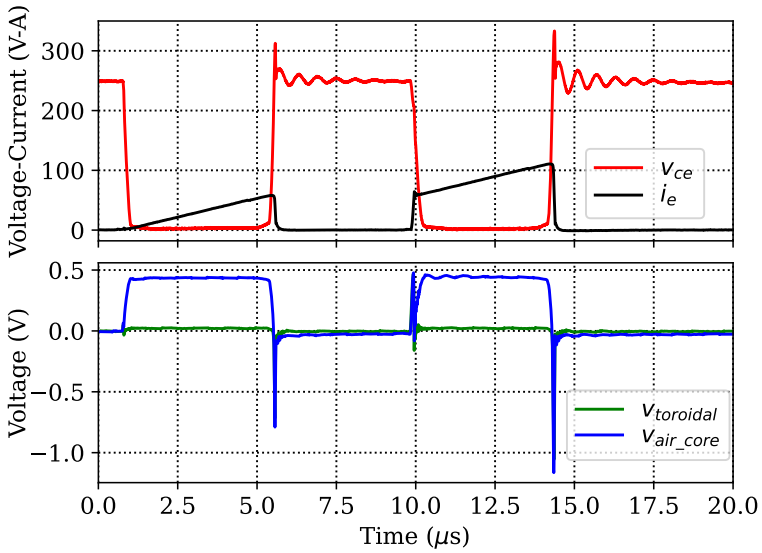
the time interval in which the derivative of current is positive and multiplying that by its mean value, the load peak current can be estimated. Two examples at 200 V are plotted in Figure 5.16, in which the microcontroller applies a 10 µs pulse. These waveforms have been captured and sampled with 100 MHz sampling frequency by an oscilloscope. As mentioned earlier, this sampling frequency is quite challenging for a microcontroller, meaning that its conversion outcome at lower sampling frequencies might be quite different than the presented one.

As for the air core measurement, the load current cannot be easily measured due to the stray field's presence and the tight load interface Figure 5.11, hence the Hall sensor's measurement accuracy is considered. In Figure 5.16a the numerically calculated emitter and Hall sensor current derivative can be seen, where the Hall signal shows a delay of around 500 ns, primarily caused by the sensor's reaction time and secondarily by the signal conditioning filter. During the switching events, there is additionally some noise in the Hall sensor's signal which might be attributed to coupled noise into the probes or can be directly coupled into the circuitry itself. Despite that fact, the time interval for the average di/dt calculation starts around 1.16 µs and ends at 10.9 µs, giving 9.73 $\mathrm{A\,\mu s^{-1}}$. Multiplying that with the time interval yields a peak current of 94.77 A, whilst the actual sensor's peak current is 94 A relatively close to the real one. By applying the same procedure for the measurement of the emitter current (Rogowski coil), the average slope is 8.98 $\mathrm{A\,\mu s^{-1}}$, giving a final peak current of 88.1 A, whilst the actual is 87.86 A. It should be noted that there is some discrepancy between the load's peak current and the actual switching current, affected by the gate drive conditions.

The second example is performed with the two series toroidal air core inductors, as shown in Figure 5.16b. In this case the load current can be measured with a Rogowski coil since the stray field is negligible. The average slope calculated with the Hall sensor is 9.71 $\mathrm{A\,\mu s^{-1}}$ (0.9 µs - 10.8 µs), giving a peak current of 96.12 A, while with the Rogowski coil the average slope is 9.6 $\mathrm{A\,\mu s^{-1}}$ (0.6 µs - 10.6 µs), giving a peak current of 96 A. The actual load peak current is 96.25 A, proving the accuracy of this method for predicting the load peak current. In this case the switching current is approximately 95.5 A.

The last example presents the same methodology, performed at 500 V with an IGBT rated at 600 V. At first glance, it can be observed that the Hall sensor's signal deviates more than the actual load

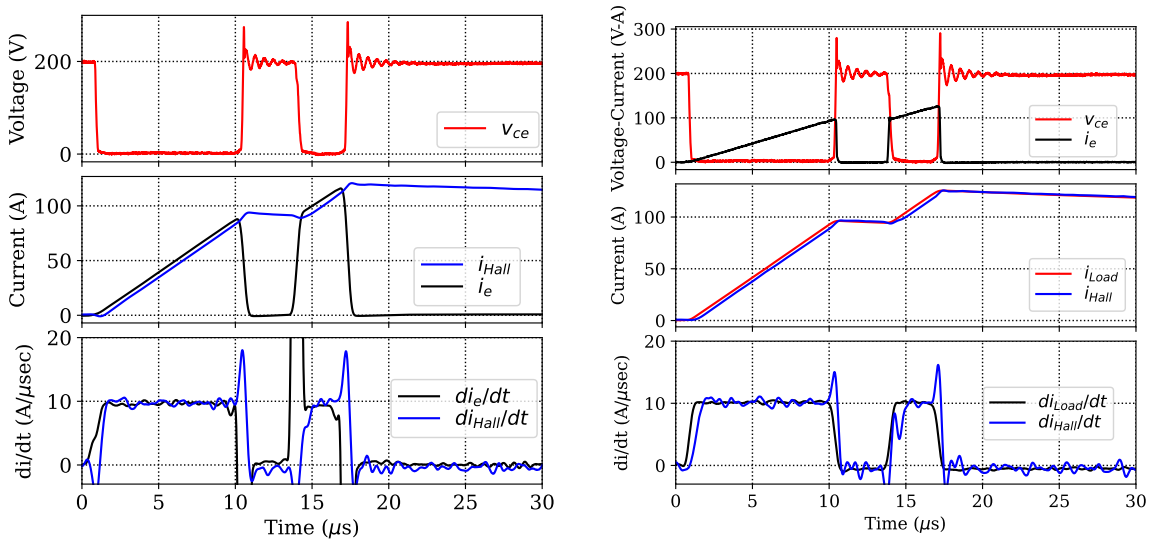
(a)



(b)

Figure 5.15: Stray field evaluation: (a) experimental setup, (b) induced voltage across the passive probe.

current. In order to estimate the switching current, it could be possible to either measure the gate-source voltage or the collector-emitter voltage. Capturing these signals with sensors has yet to be implemented and it is presented here in order to understand the challenges. This time the slope is determined by the gate-source signal, namely when it is approximately at the point of Miller plateau. The Rogowski coil measurement yields a peak current of 164.73 A. By assuming a deterministic reaction time of 500 ns as given in the data-sheet, the derivative of the sensor is shifted and the same procedure is applied, giving 159.26 A. As in the previous cases, the load peak current is estimated with the Rogowski coil to 165.7 A and with the Hall sensor to 160.35 A, while the actual is 166 A. It can be concluded that the Rogowksi coil measurement is highly accurate, while that of the Hall sensor gives a relative error of 3.4 %. All in all, this methodology has a great potential, however the limited sampling frequency, noise, high slopes may render this method unfavorable.



(a) (b)

Figure 5.16: Peak current estimation: (a) air core inductor (19.6 µH), (b) toroidal air core inductor (18.4 µH).

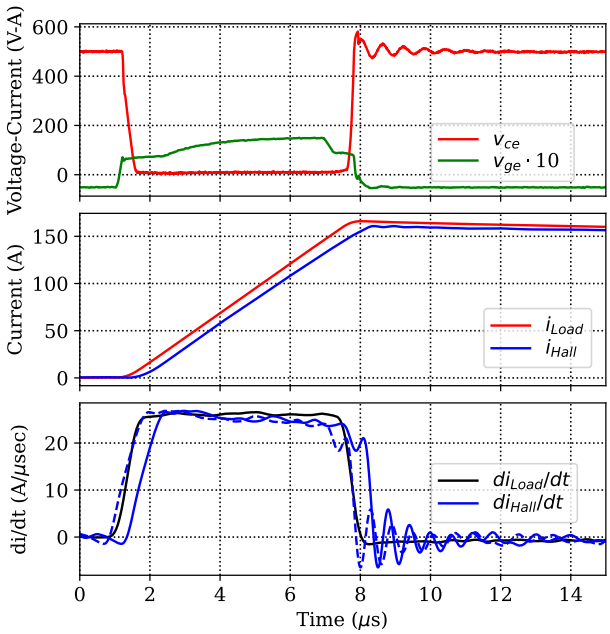


Figure 5.17: Peak current estimation (toroidal air core inductor), Halls sensor's derivative signal is shifted by 500 ns as denoted with the dashed blue line.

5.5 Conclusion

This chapter provides an introduction to the magnetics design targeting the accomplishment of dynamic pulse stress testing, and mainly intended for DP. Over the course of the hardware prototype

development, different loads and load interfaces have been adopted. Particularly, the toroidal air core inductor is the most attractive solution due to low or negligible stray fields, especially when high peak currents are necessary. The air core inductor comprises the most compact solution with the penalty of stray field, which needs further investigations in terms of near field coupling with the pending signal conditioning circuitry. As for the magnetic core inductor, it can provide low parasitic capacitance for a single layer design and ac winding losses with the drawback of lower peak currents. The preparation of such tests needs considerable effort, which can be reduced by employing a modular design, as presented in the development of the third hardware prototype by means of an edge connector. Finally, the possibility of predicting the peak current with the introduced method together with its shortcomings is also presented.

Chapter 6

Configurable Gate Driver

6.1 Introduction

This chapter is mainly related to the author's published article in [16]. As has already been highlighted in chapter 1, the intention of this multi-objective stress test system is to perform various types of tests in a multi-channel manner so as to enrich the statistical significance of the result. However, setting up such repetitive reliability tests for multiple channels requires substantial manual labour. To partially overcome this hassle, this chapter introduces a configurable gate driver based on an active gate drive (AGD) solution with adjustable gate voltage rails, which can be software programmed. This in turn enables an operator to set variable turn on/off speeds without hand-operated switching speed adjustment by gate resistors, as will be shown later. Last but not least, it should be pointed out that the CSGD development is a part of the first hardware prototype.

In general, most of the power electronic applications utilize a passive voltage source gate driver, named conventional gate drive (CGD), due to simplicity and cost reduction [95]. Such a solution is still prevalent, though, this chapter investigates alternative solutions offering less manual intervention. Therefore, the attention is turned to AGD concepts, where customized performance is provided for attaining the application's objectives. Some of the most recent studies are summarized in [95, 96, 97, 98, 99] where an in-depth overview of the different methods, such as open loop versus closed loop gate control, status feedback and protection techniques, are presented. From a stress test system point of view, the goal is to apply a dynamic repetitive stress so as to study the long-term behavior of the devices under hard switching conditions. Additionally, a simplified test pattern should be generated and executed repetitively, preferably by a not too complex local microcontroller.

By analysing the potential solutions, closed loop and feedback status solutions offer the flexibility of independent di/dt, dv/dt or even overall slope shaping control, which could be employed for sophisticated stress test scenarios. However, they tend not only to increase complexity and cost, especially the digital option, but also their required feedback circuits should be adjusted for different DUTs, introducing challenges as shown in [100]. Therefore, an open loop gate drive solution is preferred due to less cost, complexity and space requirements for a multi-channel system. In [101] an open loop CSGD for IGBTs with switching speed adjustment is proposed, however an accurately timed switching pattern for proper pulse execution is required. Another open loop approach is the employment of step-wise switched resistors but its flexibility is mainly limited by the fixed amount of parallel resistors, which is not in favour for a reliability stress test [102, 103]. Taking into account these facts, an open loop CSGD is proposed, whose gate current is adjusted via DACs in a closed loop manner.

Furthermore, low-dropout voltage regulators (LDOs) are employed for setting the desired gate voltage for the respective DUT.

This chapter covers topics, such as the circuit architecture of the CSGD, a qualitative comparison between a CGD and the CSGD during a single DP execution for various switching speeds, the derivation of the CSGD's small signal output impedance and its importance against external voltage disturbances, its small signal stability analysis extracted by a SPICE model, the comparison between the experimental and simulation results and finally potential performance improvements in the form of simulations.

6.2 CSGD Circuit Architecture

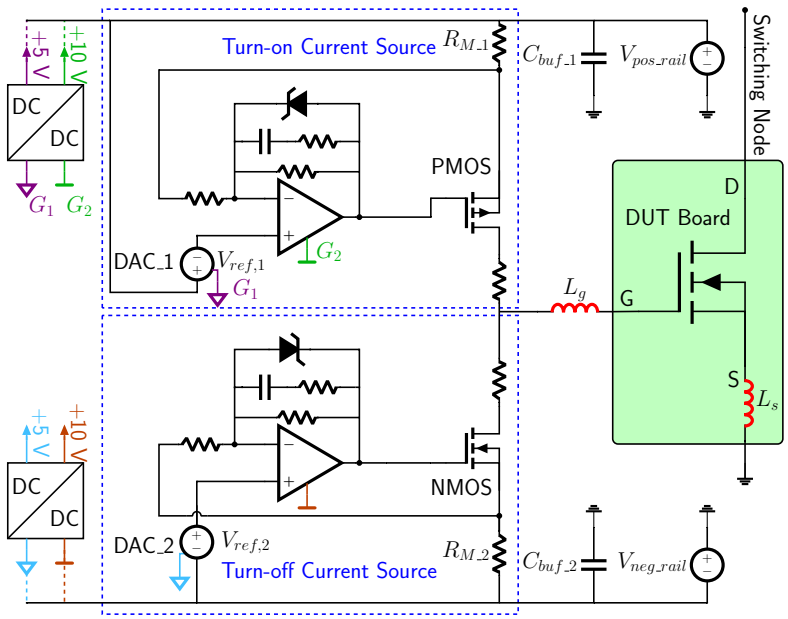


Figure 6.1: Circuit diagram of the closed loop CSGD.

The circuit diagram of the introduced CSGD is depicted in Figure 6.1. The gate driver is composed of two voltage controlled current sources, one P-type and the other one N-type (PMOS/NMOS driver) in a closed loop arrangement for a predefined charging and discharging current. Each current source employs a sufficiently fast operational amplifier to drive the PMOS/NMOS into its saturation operating area. This is accomplished by configuring the operational amplifier in a way to act as a proportional integral (PI) controller. The required signals are realized by a current sensing resistor R_{M_1}, R_{M_2}, whose voltage drop is fed back to the inverting input and a voltage reference signal connected to the non-inverting input. The voltage reference is set through a DAC over an isolated serial peripheral interface (SPI) communication. Subsequently, the operational amplifier regulates the gate voltage of the PMOS/NMOS driver in way that the sensing resistor's voltage drop is equal to the voltage reference, and therefore a gate current control. An additional high ohmic resistor is connected in the negative feedback path in combination with a zener diode for discharging the PMOS/NMOS gate voltage and clamping it to a designed zener voltage level. These operational amplifiers are supplied relative to the adjustable positive and negative rail. Just like the operational amplifier's supply, the DACs are supplied relative to the adjustable rails.

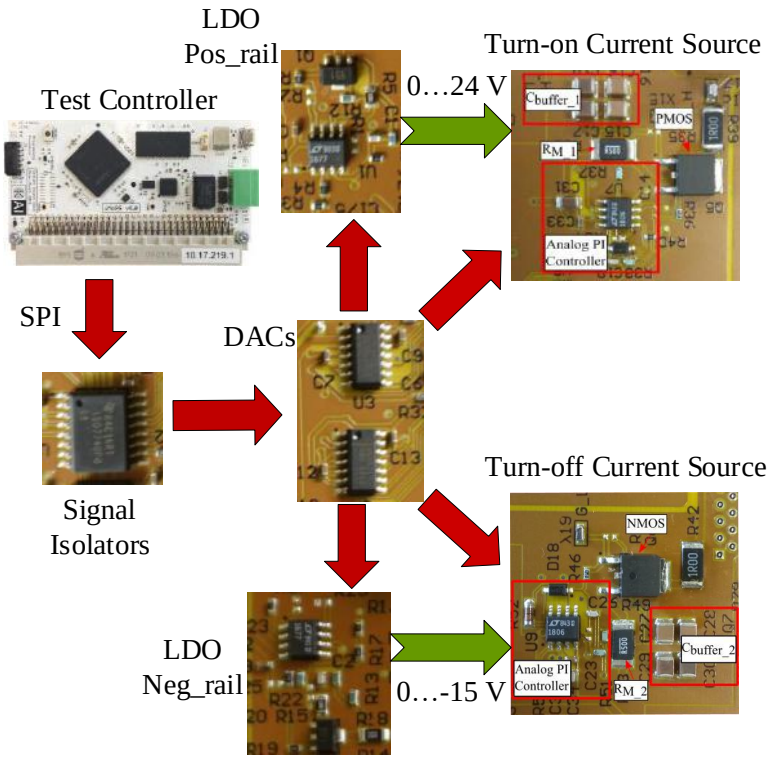


Figure 6.2: SPI and hardware interface of the CSGD. The red block arrow denotes the SPI commands, whilst the green notched arrow indicates the adjustable gate voltage rails. Turn-off current source, prototype dimensions: 27 mm x 22 mm, located on bottom side. Turn-on current source, prototype dimensions: 27 mm x 31 mm, located on top side. Signal isolators and DACs occupy a space of 29 mm x 25 mm.

The adjustable voltage rails are realized with LDOs, whose output voltage can be regulated with a reference signal provided via another DAC over the SPI interface. They support positive gate voltage up to 24 V and negative one up to -15 V. Subsequently, there are some buffer capacitors to support these supply voltages over the switching process.

The loading procedure and execution is explained with the assistance of Figure 6.2. In the beginning, an initial SPI command is sent via the μC for setting the desired gate voltage rail across the buffer capacitors C_{buffer_1} and C_{buffer_2}. Subsequently, suitable voltage references are loaded via DAC_1 and DAC_2 for attaining specific gate current. It is worth noting that the voltage reference is maintained during the total pulse duration, which is a property of the source code. For example, in case of a DP, if the first pulse is 10 µs then the voltage reference will be active during this time interval.

6.3 Preliminary CSGD Assessment

One of the major objectives of the CSGD is to drive IGBT devices sufficiently fast so that the DA phenomenon can be studied, as highlighted in chapter 2, as well as potential parameter shifts of MOSFET devices owing to repetitive hard switching events. Therefore, adequately high peak gate current should be obtained. To this end, the first hardware prototype incorporates PMOS and NMOS switches able to provide high currents (Case I), as listed in Table 6.1. Furthermore, a CGD is included

Table 6.1: CSGD Experimental Parameters

Case I †		Case II	
R_2 ‡	520 Ω	R_2 ‡	150 Ω
R_1 ‡	130 Ω	R_1 ‡	100 Ω
C ‡	100 pF	C ‡	10 pF
PMOS	DMP6180SK3	PMOS	BSS83P *
NMOS	IRLR024N	NMOS	2N7002 *

† Initial design

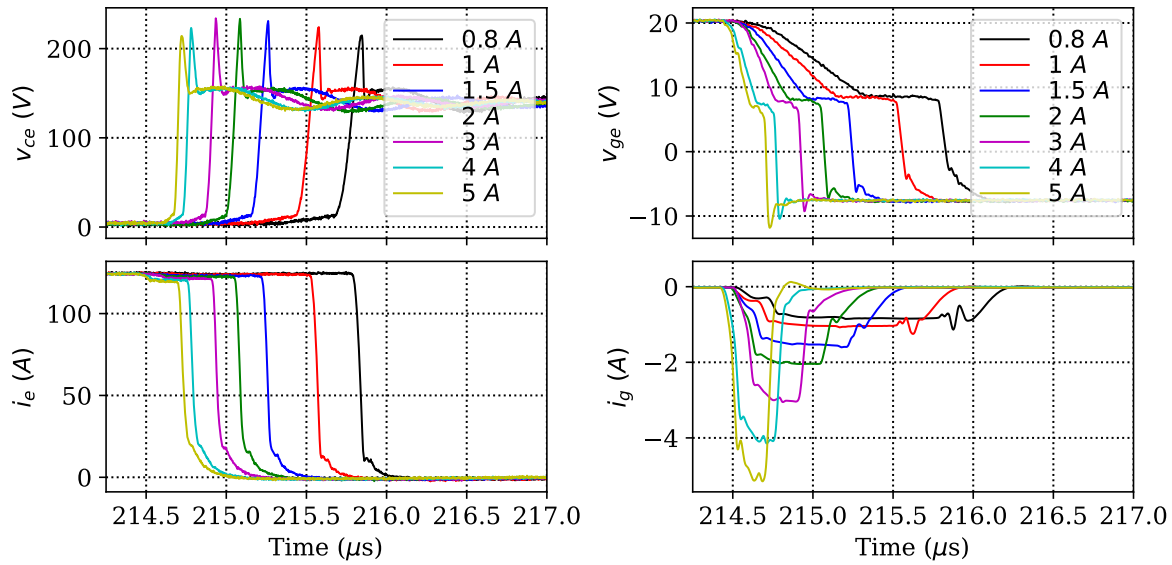
‡ Refer to Figure 6.7

* Two in parallel

for performance comparison reasons.

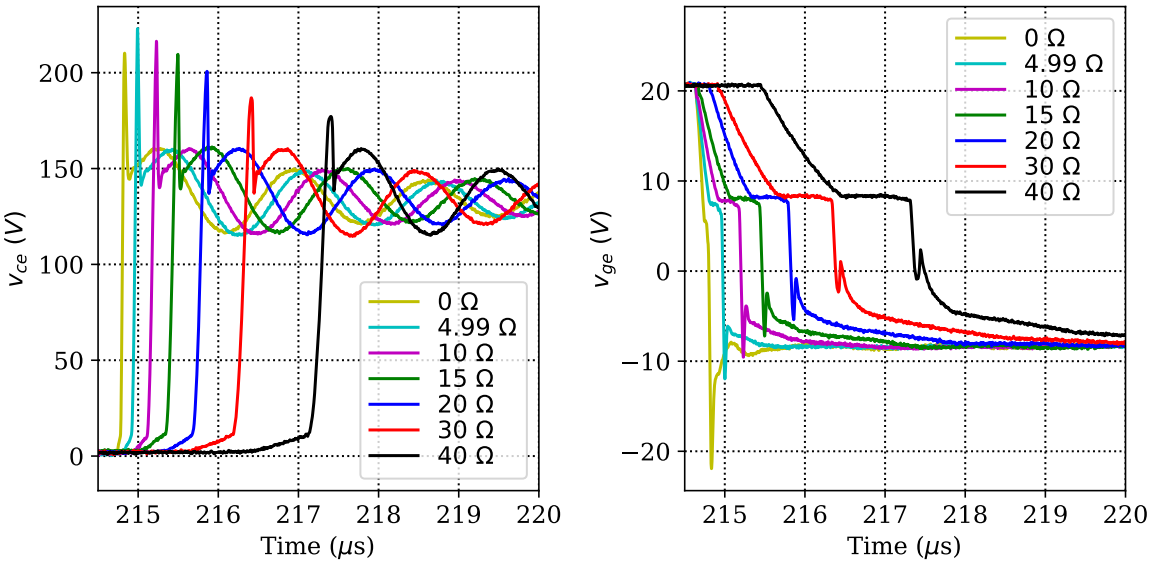
The preliminary experimental evaluation of both gate drivers is conducted by applying a single DP while using as a load the air core inductor of Figure 5.3 and dc-link voltage of 150 V. The gate voltage is preset to 20 V and −8 V. The gate current measurement is achieved by a short cable encircled around the current probe (CP030) to the gate path of the DUT. Then, the DP is executed for testing the CSGD and the CGD at various turn-off events. The current is initially ramped up to 75 A and afterwards to 120 A, for either an IGBT or a MOSFET.

The first group of waveforms refer to an IGBT in a TO-247 package, rated at 600 V and 120 A, plotted in Figure 6.3 and Figure 6.4. It should be stressed that only the turn-off transients are demonstrated, in which can be discerned that gate currents above 3 A cause the manifestation of DA, as also reported in [57]. A similar trend is seen when the CGD is used, Figure 6.4, proving the ability of the CSGD to stress this type of devices at high dv/dt and di/dt conditions.



(a) (b)

Figure 6.3: Experimental CSGD turn-off switching transients of a trenchstop IGBT: (a) collector-emitter voltage and emitter current, (b) gate-emitter voltage and gate current.



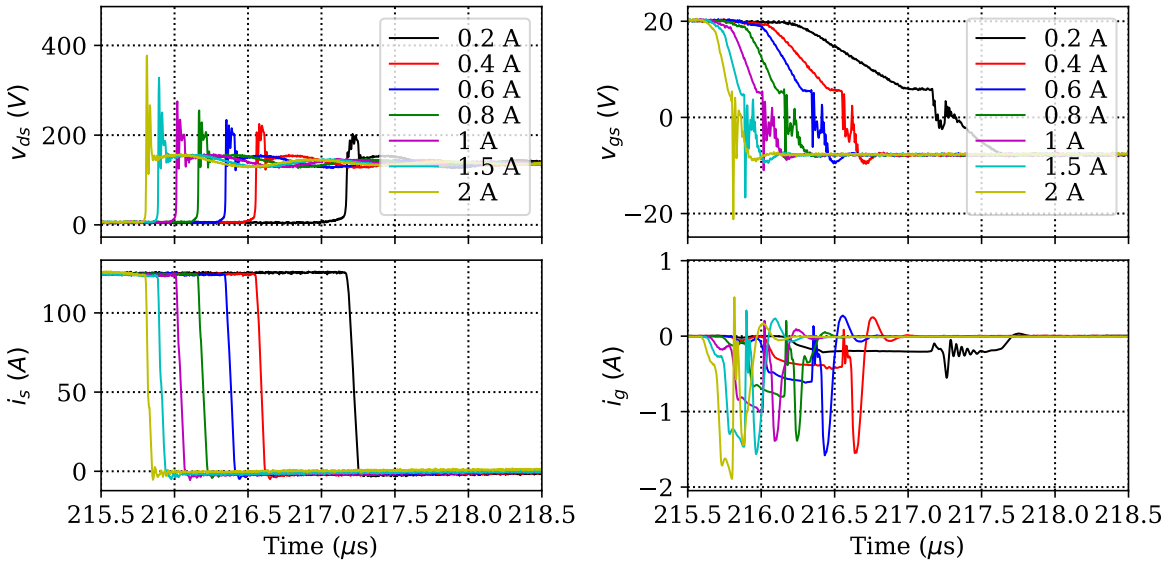
(a) (b)

Figure 6.4: Experimental CGD turn-off switching transients of a trenchstop IGBT: (a) collector-emitter voltage, (b) gate-emitter voltage.

The second group of waveforms refer to a superjunction MOSFET in a TO-247 package, rated at 600 V and 75 A, plotted in Figure 6.5 and Figure 6.6. It can be observed that the CSGD response exhibits more oscillatory behavior which is damped with the CGD, especially at slower switching speeds. This abnormal behavior occurs when the load current transitions to its off-state, appearing as an external disturbance to the CSGD due to the source inductance. Two main factors indicate the CSGD ability to overcome smoothly such events. The first one is its output impedance and the amplitude variability over the frequency, which can alter the gate current due to high external voltage spikes. The second one is the phase margin (ϕ_m), influenced by the feedback circuitry, indicating the CSGD ability to regulate the current back to its reference value. These are the linear effects, though, there is another effect which will be discussed later. To partially overcome this, it is decided to investigate the use of different PMOS and NMOS switches with less parasitic capacitances, combined with different feedback gains, with the prospect of improving the output impedance. A combination of two parallel NMOS/PMOS driver MOSFETs is chosen, for an increased gate current handling capability (Case II), as shown in Table 6.1. In both cases, the small signal output impedance and loop stability is analyzed.

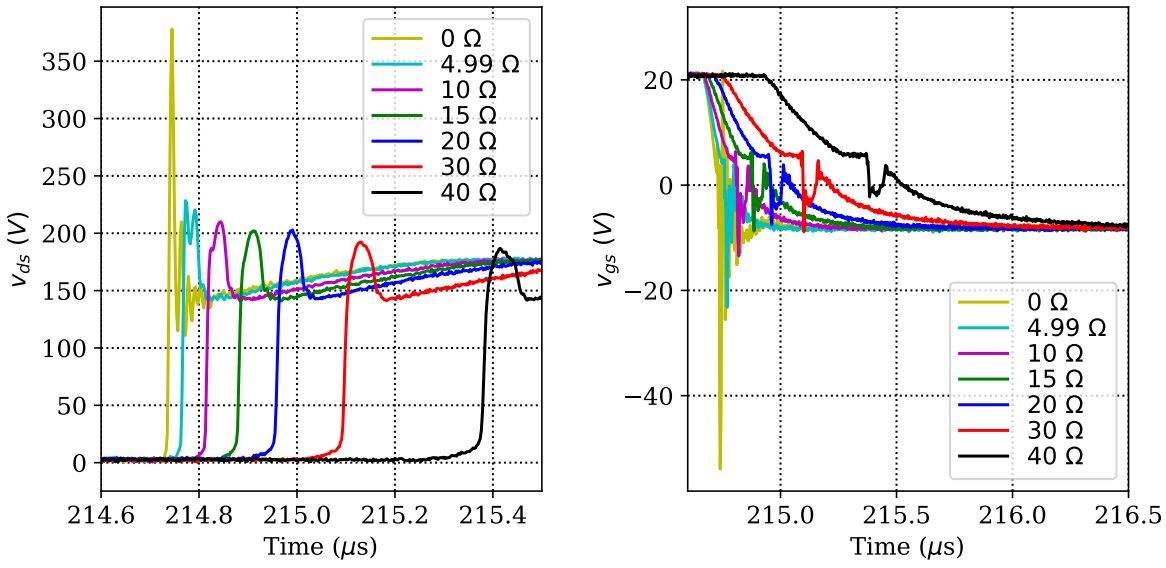
6.4 Small Signal Output Impedance

In this section, the small signal output impedance model of the currently employed gate driver is derived and its possible effects during the switching transients are indicated. As already shown, the turn-on and turn-off current source circuits are symmetrical, therefore it is adequate to independently analyse one of them. Particularly, the PMOS output driver mostly operates in the saturation area during regulation, and therefore its equivalent small signal model is substituted, as shown in Figure 6.7. Moreover, different operating points, influenced by drain-source voltage and voltage reference, affect the dynamic behavior, and consequently the frequency domain analysis. Finally yet importantly,



(a) (b)

Figure 6.5: Experimental CSGD turn-off switching transients of a superjunction MOSFET: (a) drain-source voltage and source current, (b) gate-source voltage and gate current.



(a) (b)

Figure 6.6: Experimental CGD turn-off switching transients of a superjunction MOSFET: (a) drain-source voltage, (b) gate-source voltage.

the DUT itself can cause a major impact on the dynamic response, especially during the switching transients.

Initially, all the independent voltage sources should be grounded for the ac small signal model

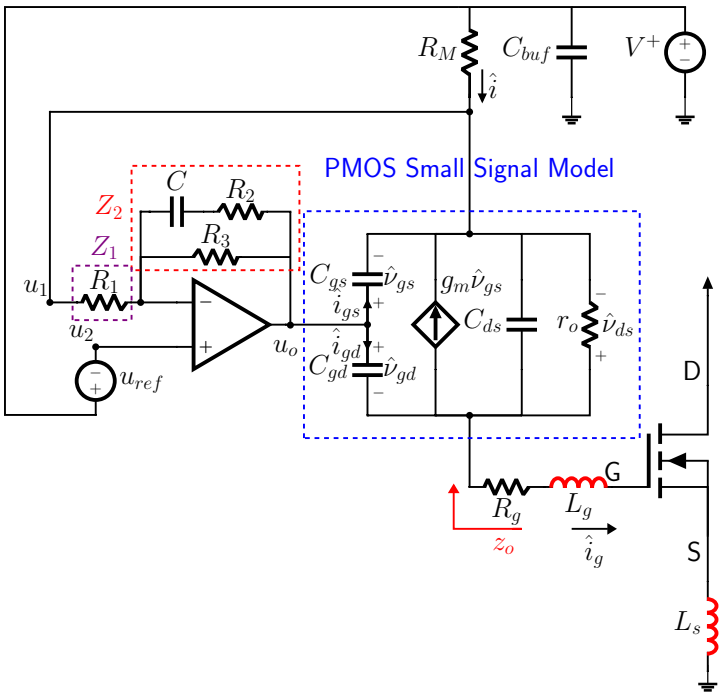


Figure 6.7: PMOS small signal circuit diagram.

derivation. Then, the output voltage of the operational amplifier is derived by applying the superposition principle for the inverting and non-inverting input, yielding Equation (6.1). Where $A(s)$ is the open loop frequency response of the operational amplifier gain, $u_o^+(s)$ is the frequency response from the non-inverting input to the output and $u_o^-(s)$ identically for the inverting input.

$$\begin{aligned} u_o(s) &= u_o^+(s) + u_o^-(s) \\ u_o^+(s) &= 0 \\ u_o^-(s) &= \frac{\frac{Z_2(s)}{Z_1(s)}}{1+\frac{1}{A(s)}(1+\frac{Z_2(s)}{Z_1(s)})} R_M i(s) \end{aligned} \tag{6.1}$$

Subsequently, the gate-source voltage is obtained in Equation (6.2) after manipulation of Equation (6.1) to find the final transfer function.

$$\begin{aligned} \hat{\mathrm{v}}_{gs}(s) &= u_o(s) - u_1(s) \\ \hat{\mathrm{v}}_{gs}(s) &= G_{op}(s) R_M \hat{i}(s) \\ G_{op}(s) &= \frac{(1+\frac{Z_2(s)}{Z_1(s)})(1+\frac{1}{A(s)})}{1+\frac{1}{A(s)}(1+\frac{Z_2(s)}{Z_1(s)})} \end{aligned} \tag{6.2}$$

Applying Kirchhoff's current law (KCL) at the source and the drain node of the PMOS results in Equation (6.3). The gate-source $\hat{i}_{gs}(s)$ and the gate-drain $\hat{i}_{gd}(s)$ current can be expressed as functions of $\hat{\mathrm{v}}_{gs}(s)$ and $\hat{\mathrm{v}}_{ds}(s)$. By substituting Equation (6.2) in Equation (6.3), the current through R_M, $\hat{i}(s)$,

can be expressed as a function of $\hat{v}_{ds}(s)$, Equation (6.4).

$$\begin{aligned} \hat{i}(s) &= -g_m \hat{v}_{gs}(s) - (\frac{1}{r_o} + C_{ds}s)\hat{v}_{ds}(s) - \hat{i}_{gs}(s) \\ \hat{i}_g(s) &= \hat{i}(s) + \hat{i}_{gd}(s) + \hat{i}_{gs}(s) \\ G_{v_{ds}}(s) &= \frac{1}{r_o} + C_{ds}s \end{aligned} \tag{6.3}$$

Equivalently, the $\hat{i}_g(s)$ can be represented as a function of $\hat{i}(s)$ and $\hat{v}_{ds}(s)$. Substitution of (6.4) into $\hat{i}_g(s)$ leads to the final small signal output impedance in Equation (6.5).

$$\begin{aligned} \hat{i}(s) &= \frac{-(\frac{1}{r_o} + C_{ds}s)}{1 + G_{v_{gs}}(s) R_M G_{op}(s)} \hat{v}_{ds}(s) \\ G_{v_{gs}}(s) &= g_m + C_{gs}s \end{aligned} \tag{6.4}$$

The output impedance serves as a performance indicator of the current source, because gradual frequency increase causes the impedance magnitude to diminish. Consequently, the driver becomes susceptible to external disturbances and oscillations. Figure 6.8 shows the small signal output impedance of both cases by using the full SPICE model, in which Case II shows higher output impedance at frequencies beyond 10 kHz.

$$\begin{aligned} z_o(s) &= -\frac{\hat{v}_{ds}(s)}{\hat{i}_g(s)} \\ z_o(s) &= \frac{1 + G_{v_{gs}} R_M G_{op}}{G_{v_{ds}}(1 + C_{iss} R_M G_{op} s) + C_{gd}(1 + G_{v_{gs}} R_M G_{op})s} \end{aligned} \tag{6.5}$$

Figure 6.9 indicates the SPICE simulation response of the NMOS current source of Case II for different biasing scenarios. As the drain-source voltage decreases during the discharging, the output impedance declines mostly due to the significant change of r_o, dependent on the parameter λ. However, as the voltage reference is increased, the output resistance (r_o) decreases, as influenced by the biased current, and the transconductance (g_m) increases, leading to smaller output impedance variations. Finally, the derived model is compared with a simplified and full SPICE model of the NMOS driver. In the mathematical model, the ideal open loop gain and gain-bandwidth product (GBP) of the operational amplifier together with the NMOS data-sheet parameters are employed. The simplified SPICE model includes an ideal operational amplifier, using again the ideal gains of the operational amplifier, as well as elimination of the majority of the NMOS internal parasitic components. The main difference between the full and the simplified model lies in the large internal gate resistance, which is 50 Ω. Last but not least, the feedback gain selection and the operational amplifier's frequency response contribute to the final output impedance magnitude as can be inferred from Equation (6.5), which is not explicitly covered.

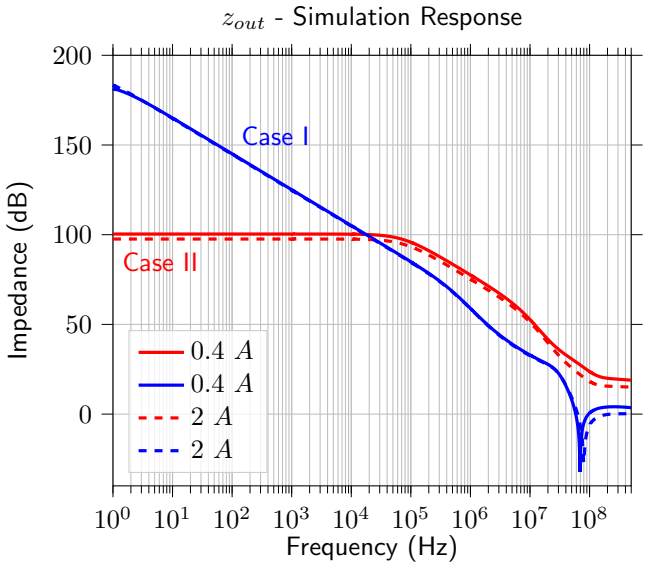


Figure 6.8: Full SPICE model - NMOS small signal output impedance biased at 15 V drain-source voltage for two different operating points. Where 0 dB refers to 1 Ω.

6.5 Stability Analysis

As has been already discerned, such a system includes many state variables and its full mathematical analysis can lead to higher order transfer functions, which are cumbersome to solve. Furthermore, a simplified model might not be sufficient enough to describe the system's stability. Therefore, the system's loop gain is estimated by simulating the full SPICE model using Tian's method [104].

Initially, the loop gain of Case I and Case II is presented in Figure 6.10. For this simulation scenario the gate inductance is assumed to be L_g = 30 nH, the R_g = 1 Ω and the R_3 = 110 kΩ. Moreover, a zener diode is included from the SPICE library. Both cases are stable since at 0 dB the phase margin is high enough, above 90 deg. However, Case I has slightly larger bandwidth and thus rendering it faster than Case II. It is also worth noting that any resonance in the loop gain might appear in the transient response, especially when its gain is high.

The next step is to point out some of the main factors that influence the system's stability by taking as a reference the Case II. Figure 6.11 shows the system's loop gain around a dc biased operating point for three different gate inductances (L_g), as well as the introduction of the zener diode, simplified by an equivalent capacitance (C_z). At low frequencies the gain is mainly limited due to the presence of R_3, affecting the integral ability of the PI controller. It can be seen that the system is only stable for $L_g = 30$ nH, having a phase margin of $\phi_m = 58.5$ deg. The introduction of the zener diode reduces the total bandwidth and stabilises the system, as it shifts the low frequency pole of the feedback network around the operational amplifier, resulting in phase margin of $\phi_m = 84$ deg at $C_z = 100$ pF.

It should be clarified that different techniques can be used, though, the introduction of the zener diode is only presented. In addition, the exact values of all the board and component parasitics can also affect the system's stability. Lastly, damping components such as ferrite beads are of particular importance, since they can improve the stability and subsequently the transient performance.

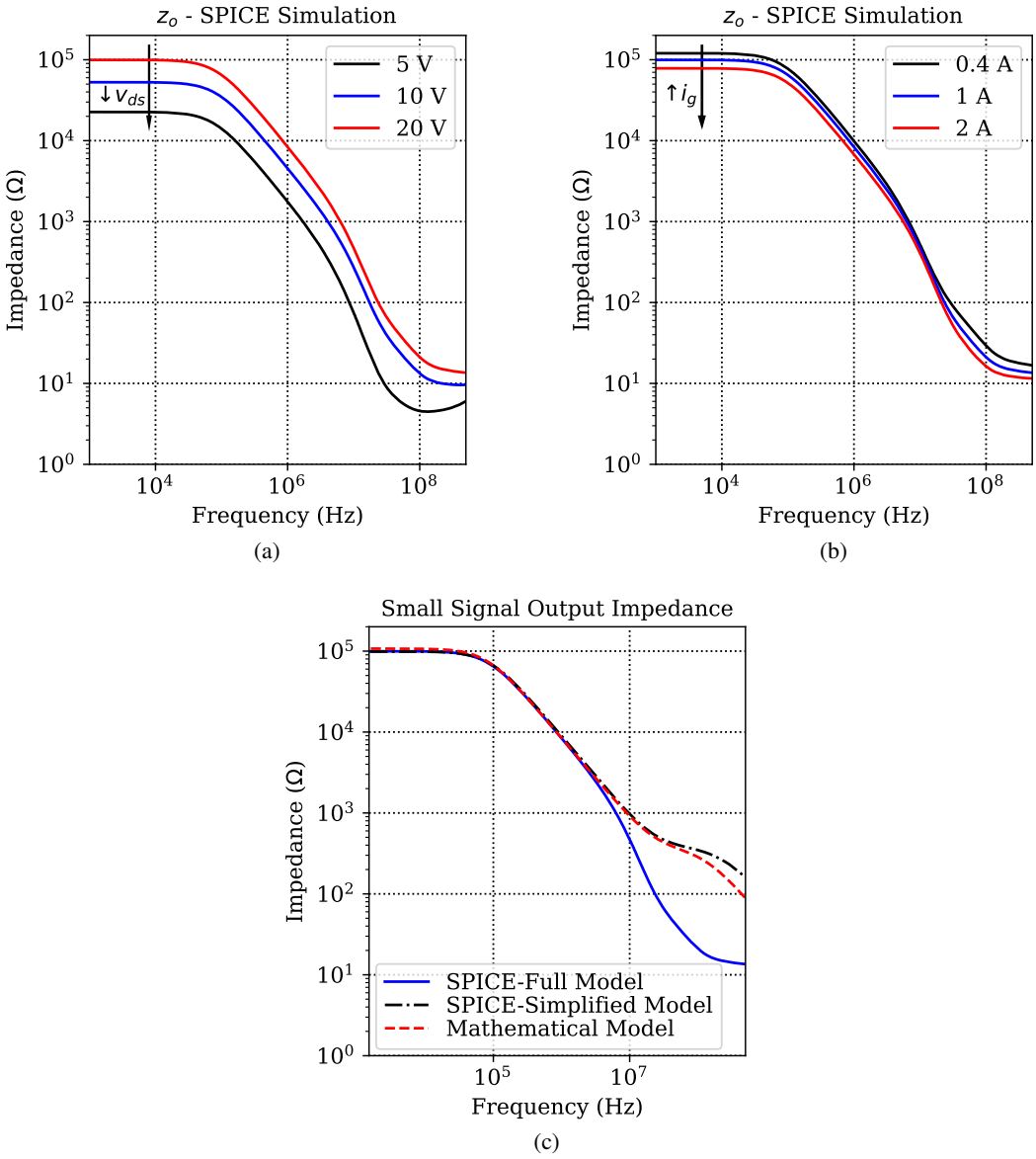


Figure 6.9: NMOS - ”2N7002” current source output impedance magnitude: (a) drain-source voltage biasing effect, where the long arrow denotes the direction of voltage decrease (b) voltage reference effect (u_{ref}) represented by its equivalent output gate current, where long arrow points the direction of voltage increase (c) comparison of derived model and SPICE models, biased at 20 V drain-source voltage and 1 A gate current, r_o derived from the SPICE model and inserted to the mathematical model.

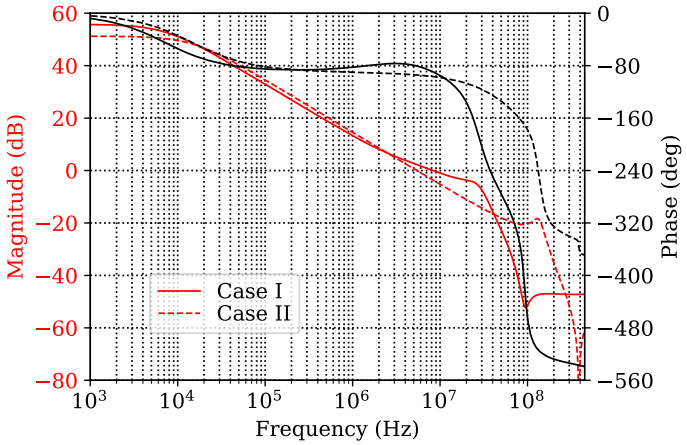
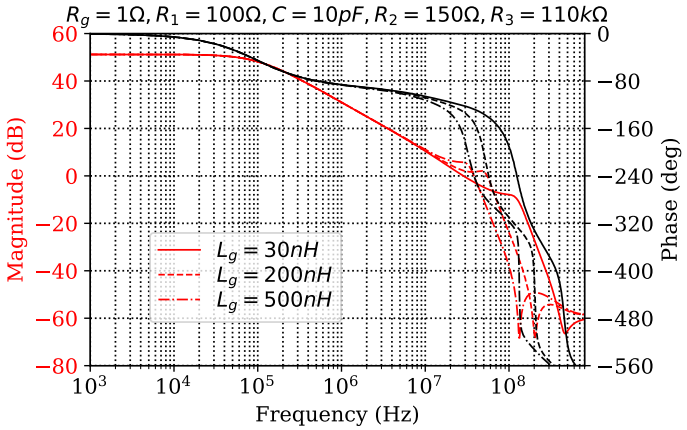
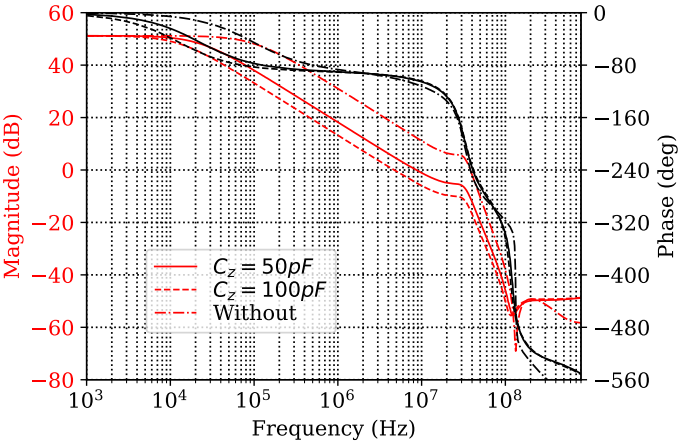


Figure 6.10: Simulation of the NMOS driver loop gain biased at 20 V drain-source voltage and 1 A gate current.

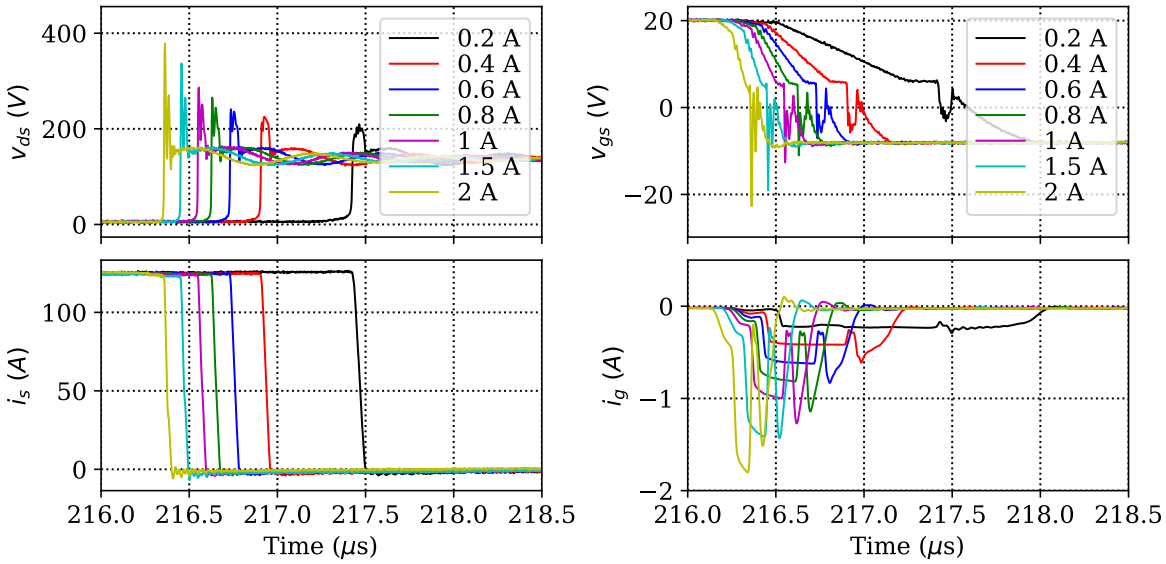


(a)



(b)

Figure 6.11: Simulation of the NMOS driver (”2N7002” - two in parallel) loop gain, biased at 20 V drain-source voltage and 1 A gate current: (a) gate inductance effect (L_g), (b) zener diode capacitance effect (C_z) at $L_g = 500\,\text{nH}$.



(a) (b)

Figure 6.12: Experimental CSGD turn-off switching transients of a superjunction MOSFET - Case II: (a) drain-source voltage and source current, (b) gate-source voltage and gate current.

6.6 Simulation - Experimental Results

This section is devoted to comparison of the experimental results of Case II and the SPICE simulation model of the CSGD. The test conditions are the same as that of the previous section. Before comparing the simulation with the experimental results, the CSGD response of Case II is plotted in Figure 6.12. It can be seen that its transient response is less oscillatory which is attributed to its higher output impedance , see Figure 6.8, as well as its slower loop gain response in which the resonance appears at higher frequencies, see Figure 6.10.

Regarding the accuracy of the simulation model, certain facts should be highlighted. A more qualitative representation of the system's behavior is presented since it relies on the component models, their availability, as well as the board and component parasitics. Additionally, the clamping diodes are simulated with an ideal diode model for complexity reduction and simulation convergence. It should be mentioned that external parasitics are added, e.g. source or emitter inductance, to improve the accuracy of the model. Last but not least, the probe location attached to the DUT has an additional effect on the comparison, due to the enclosed inductance. The following subsections discuss the simulation and experimental waveforms of the aforementioned conditions.

6.6.1 Case Study - IGBT

The turn-on transient response is illustrated in Figure 6.13. Three different switching speeds for a turn-on current of 75 A are examined, where the SPICE simulation reference current (dash-dotted line) is also added. The simulation response is slightly faster than the experimental one, probably due to higher input capacitance of the investigated device versus the SPICE model. This can also be inferred by the gate current integral, which is the total input charge. In general, as the DUT's input capacitance gets smaller, the switching speed is increased. The increased di/dt combined with the

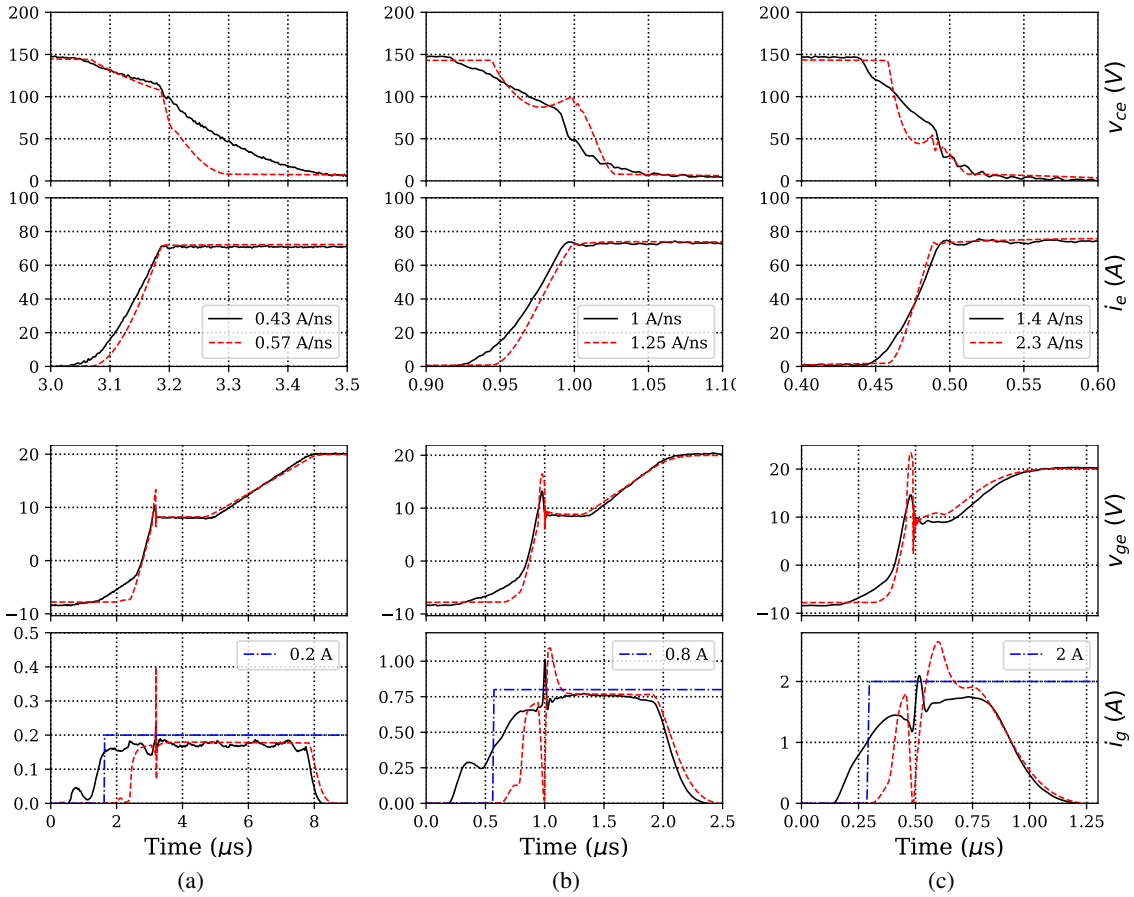


Figure 6.13: Experimental (solid line) and SPICE simulation (dashed line) turn-on switching transients of a trechstop IGBT where for each case the average di_e/dt is recorded: (a) $i_g = 0.2\,\mathrm{A}$, (b) $i_g = 0.8\,\mathrm{A}$, (c) $i_g = 2\,\mathrm{A}$.

common emitter or source inductance results in a temporary voltage dip across the PMOS/NMOS driver, as also reported for another CSGD type in [105]. This causes the current source to enter the ohmic region, a non-linear impact, and thus current destabilization.

The turn-off transient response is plotted in Figure 6.14. Likewise, three different switching speeds are indicated. It can be seen that the behavioral SPICE model does not include the tail current effect. Furthermore, it can be concluded that this IGBT has a limit for its current switching speed, as the emitter inductance is roughly (L_e) 13 nH, as stated in the data-sheet. This IGBT type also shows a different turn-off behavior than previous IGBTs in regard to a dip during the end of Miller plateau, as described in [106, 98].

6.6.2 Case Study - MOSFET

The turn-on and turn-off switching transients are presented in Figure 6.15 and Figure 6.16 respectively. In this case study, the MOSFET SPICE model shows superior accuracy over the counterpart IGBT model, so that concrete conclusions can be drawn from simulations.

As MOSFET devices intrinsically switch faster due to less input capacitance, both current sources

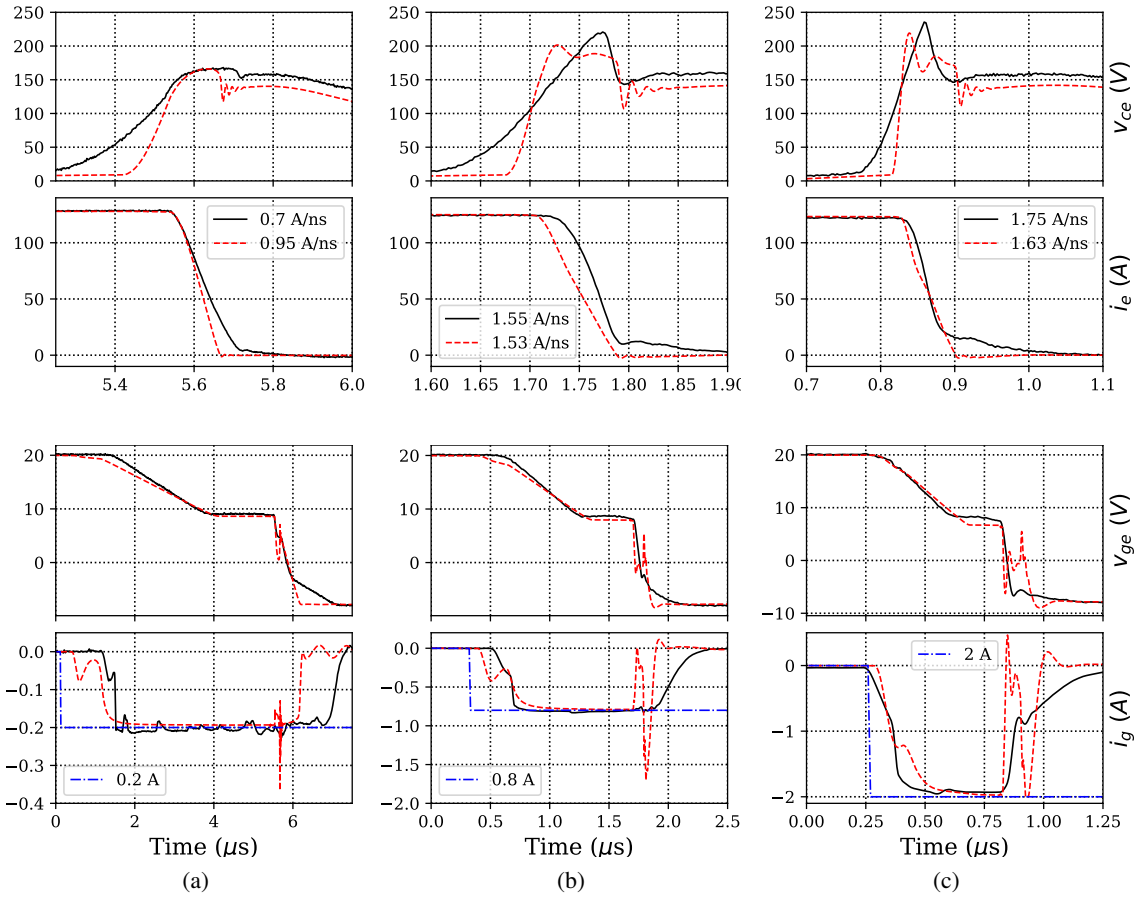


Figure 6.14: Experimental (solid line) and SPICE simulation (dashed line) turn-off switching transients of a trechstop IGBT where for each case the average di_e/dt is recorded (tail current is omitted): (a) $i_g = 0.2\,\mathrm{A}$, (b) $i_g = 0.8\,\mathrm{A}$, (c) $i_g = 2\,\mathrm{A}$.

get destabilised at turn-on and turn-off during the DUT's current decay. This happens due to the combination of output impedance effect and ohmic region regime. This transient voltage dip across the NMOS/PMOS can also go down to low voltages, causing the gate current to rapidly diminish. This non-linear effect dominates over the output impedance effect, limiting the switching speed.

All the waveforms show that the obtained gate current deviates from its reference, which is mainly attributed to the overall system's bandwidth as well as a crossing current that occurs during the transition between on and off-state. As for the latter case, for example, when the NMOS is turned off and the PMOS is turned on, this current flows from the positive to negative supply until the NMOS is fully switched off and vice versa. As for the former effect, it causes slower charging of the NMOS/PMOS gate, and thus additional time delay. In particular, the simulation models of some components are not available such as the zener diode which has an impact on the system's bandwidth, as stated previously, and may thus affect the transient response.

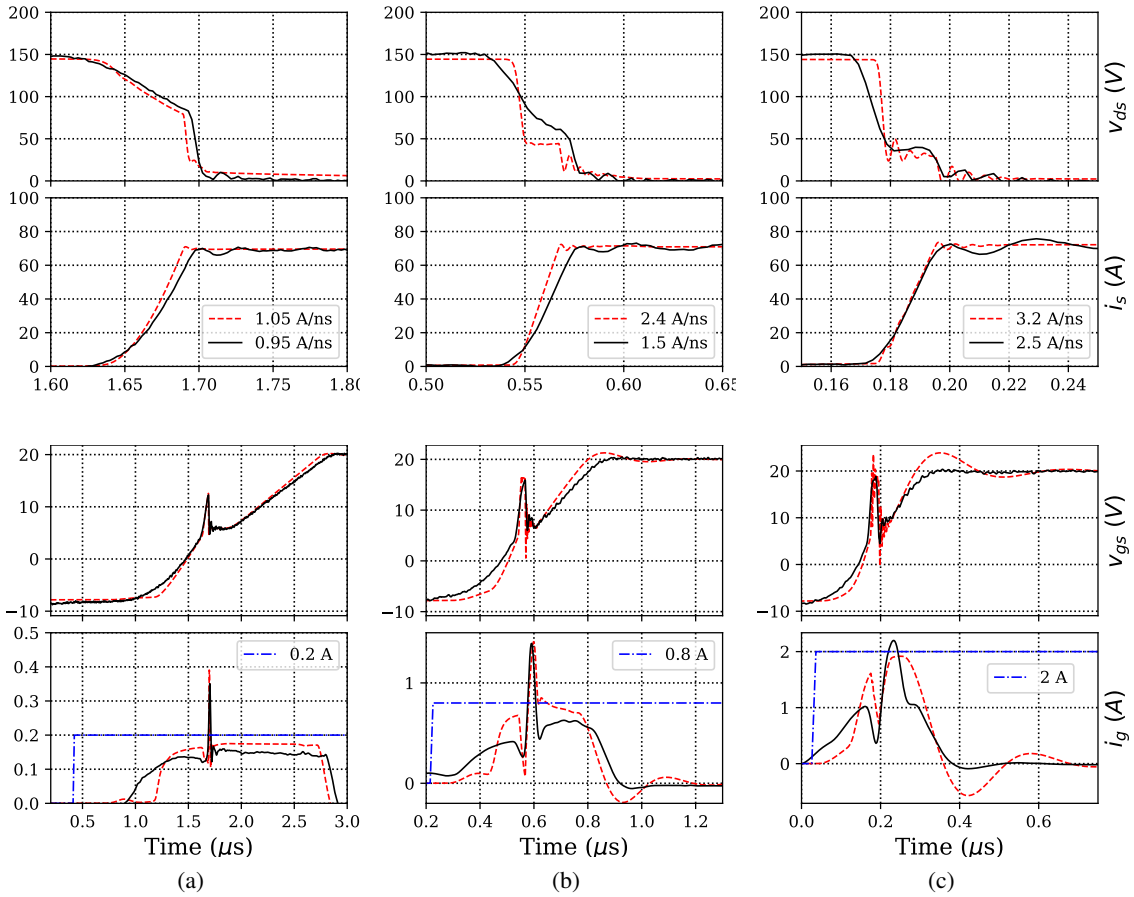


Figure 6.15: Experimental (solid line) and SPICE simulation (dashed line) turn-on switching transients of a superjunction MOSFET where for each case the average di_s/dt is recorded: (a) $i_g = 0.2\,\text{A}$, (b) $i_g = 0.8\,\text{A}$, (c) $i_g = 2\,\text{A}$.

6.7 Performance Enhancement

As already explained, the inherent limitations of the proposed current source can limit the di/dt, especially for the faster devices, namely MOSFETs. Typically, the voltage reference should be increased for faster switching capability. However, the driver's thermal peak current limit poses an upper design threshold. Alternatively, the di/dt can be increased by adding an inductor or a ferrite bead in series to the gate. This causes the output impedance to increase, and thus the voltage dip across the NMOS/PMOS driver during the current decay to be modified. Additionally, ferrite beads can also damp resonant peaks due to the formation of resonant tanks between the gate inductance and the parasitic capacitances of the NMOS/PMOS driver. A simulation has been carried out for three different gate inductors, and their effect on the switching transients is illustrated in Figure 6.17. The simulation accuracy of the superjunction MOSFET allows to conclude that faster switching is possible by carefully increasing the gate inductance on condition that gate control is retained. At higher switching speeds the transition is governed by other mechanisms for this type of MOSFET, as stated by the manufacturer's application note [107].

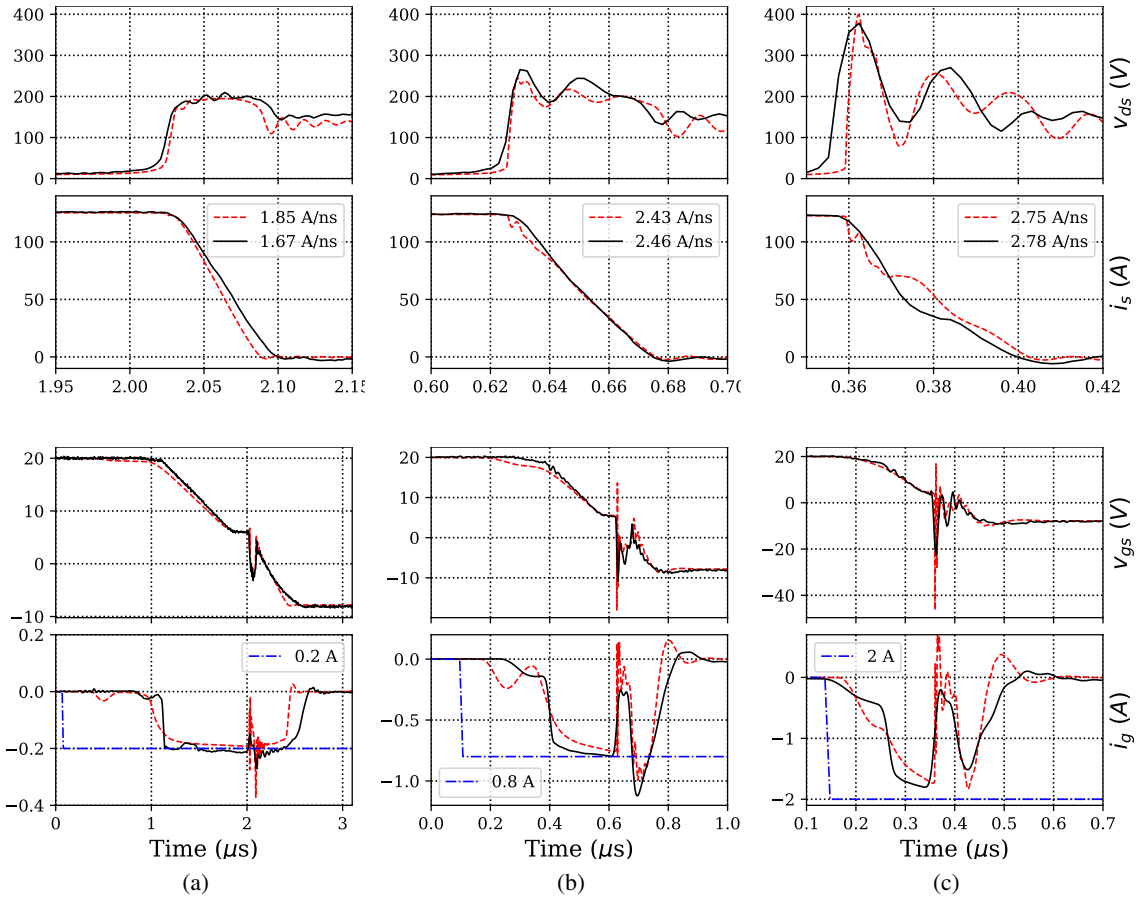


Figure 6.16: Experimental (solid line) and simulation SPICE (dashed line) turn-off switching transients of a superjunction MOSFET where for each case the average di_s/dt is recorded: (a) $i_g = 0.2\,\text{A}$, (b) $i_g = 0.8\,\text{A}$, (c) $i_g = 2\,\text{A}$.

6.8 Conclusion

From a stress test point of view, an open loop CSGD offers the flexibility to reduce the required manual effort of adjusting the gate drive conditions, less hardware complexity and cost. A software programmed interface is provided for setting the desired gate voltage and current reference. The developed prototype offers a modular way to execute different stress test conditions so that drift phenomena and potential unknown failures can be investigated.

The CSGD parasitics and non-linearities together with their repercussions on its performance have been thoroughly highlighted. A TO-247 IGBT and Si-MOSFET have been experimentally tested to evaluate the CSGD performance at different operating points. An additional comparison between the experimental and SPICE simulation switching transients indicates that there is room for additional model improvement. Particularly, the simulation model of the MOSFET presents better accuracy, and thus can be utilised as a tool for additional circuit analysis. A simulation for three different gate inductors shows the ability of the CSGD to perform even faster current switching speeds under certain conditions. Consequently, a suitable inductor or ferrite bead can be employed to cover the desired switching speed range of the case study DUT. Subsequently, this inductance can be a fixed

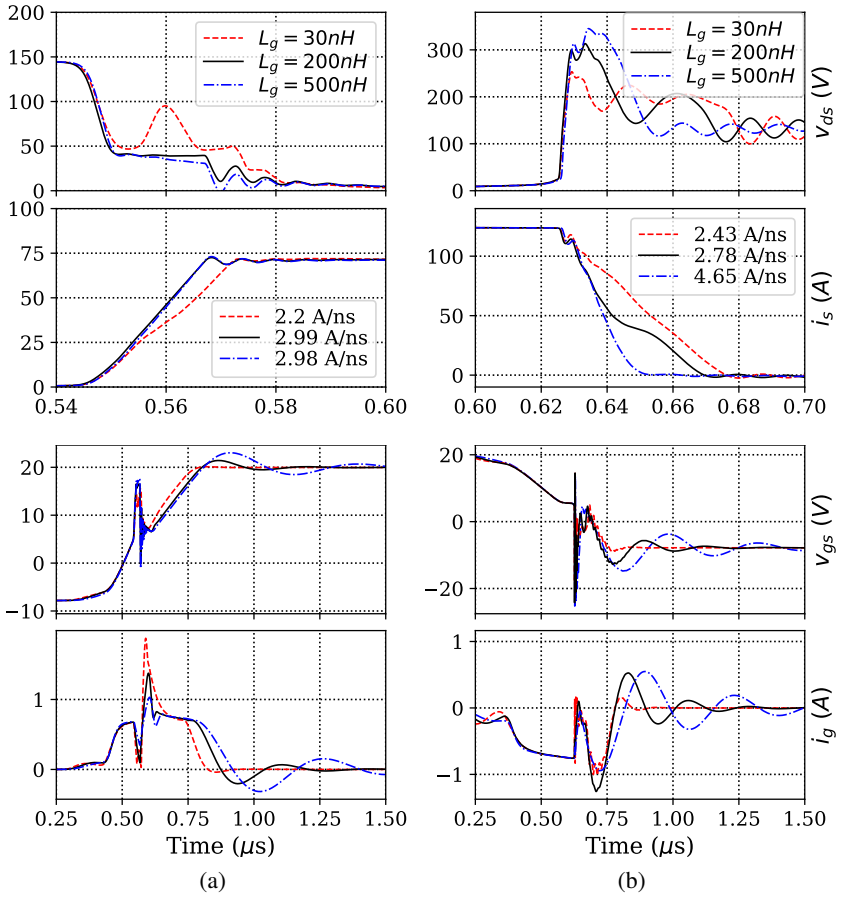


Figure 6.17: Simulation of gate inductance effect (L_g) on turn-on and turn-off of a superjunction MOSFET at $i_g = 0.8$ A: (a) turn-on, (b) turn-off.

component within the DUT interface.

As far as the overall circuit performance and analysis is concerned, there are several research topics that could be further investigated, however they are beyond the scope of this thesis. Some of them include, the CSGD ability to stress a broad range of discrete devices at several operating points, potential long-term reliability issues due to imposed oscillations in case that cannot be eliminated, the meticulous explanation of the formatting resonant tanks by incorporating PMOS/NMOS switches, component and PCB parasitic effects and lastly the validation of the output impedance model by possibly utilizing system identification techniques, as explained in [108], initially applied in the simulation domain and subsequently in the actual lab environment or directly measured by suitable instrument.

Chapter 7

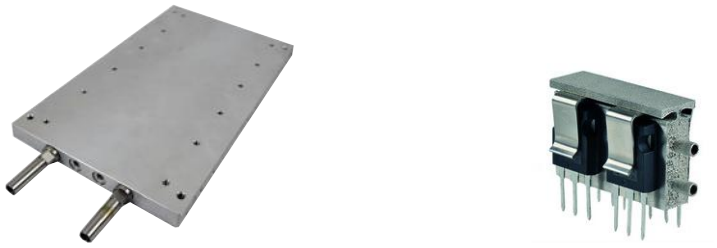
Future Work and Conclusion

7.1 Future Design Aspects

Thus far, this thesis is mainly focused on topics related to the design considerations and performance of the reliability stress test system itself, as this is its primary goal. Currently, all parameter drifts (ageing indicators) during the stress testing are periodically measured via offline read-outs. However, there is a dedicated space allocated on the DUT board as well as on the stress board where certain condition monitoring circuitry has been placed, such as the gate-voltage sensing, the front side case temperature acquired via Pt100 resistor and the collector/drain sensing voltage. Their performance has yet to be assessed. Additional circuitry details are provided in [14, 15]. Apart from that, further research is also required to develop suitable circuit arrangements in the view of measuring in-situ the representative ageing indicators for each applicable stress test, e.g. the on-state voltage drop under SC testing as highlighted in [54] or the threshold voltage drift under UIS testing as indicated in [42] provided the stressing conditions are not violated. The great benefit of the in-situ condition monitoring is the reduced time to obtain the final stress testing outcome, since the separate step of the offline read-outs is omitted.

Another topic of vital importance is the setup's ability to stress devices at elevated case temperatures which can be achieved either via a climate chamber or through a liquid cooling interface. Both cases should be evaluated in terms of their benefits and drawbacks. In particular, the great advantages of the liquid cooling interface would be that the total system is not heated up, improving its own reliability, and its cooling capability enabling the possibility to accelerate the stressing conditions. Therefore, different liquid cooling approaches can be followed either by cooling down multiple channels using one cooling plate or by individually cooling down each channel with a dedicated cooling plate, as shown for example in Figure 7.1.

Additional future protection measures can be introduced such as the adjustment of the gate-emitter voltage of the GS at the beginning of each stress test. For instance, when the stress test target is the SC test, the gate-emitter voltage can be reduced below 15 V in order to limit the SC current during the SC type II across the GS and when the target is the DP test, then the gate-emitter voltage can be increased to 15 V or even more so that the conduction and the switching losses can be reduced. Nevertheless, as the EMC analysis is also a pending topic, they have to be considered simultaneously. Furthermore, the new programmable gate driver features an analog-to-digital converter (ADC) to measure the GS external temperature by forming a resistive divider using a negatitive temperature coefficient (NTC) thermistor. This thermistor can be potentially positioned on an accessible hot spot in the vicinity of the



(a) (b)

Figure 7.1: Liquid cooling interface options: (a) cooling plate for multi-channel, (b) cooling plate for each DUT board.

GS, e.g. on the heat sink or the GS itself, which, in turn can warn the gate driver for over temperature event and subsequently to stop the test.

Another future topic is the optimization of the capacitor bank size by considering the total amount of parallel channels located on a backplane board as well as the number of backplanes boards shared by a single PSU. Moreover, the DP scheme generation is also crucial in terms of the capacitor's sizing, which can be accomplished by either sending concurrent or successive pulses among the channels. The same rationale applies to the other tests on condition that the stressing conditions are not influenced.

In order to get deeper insight into the power device characteristics, additional modelling can be employed by using both experiments and SPICE simulations for all tests. For instance, an experimental UIS pulse of a superjunction Si MOSFET with its corresponding SPICE model is compared as presented in Figure 7.2.

It can be seen that the SPICE behavioral model exhibits higher avalanche breakdown voltage and avalanche duration (t_{av}) than the actual device, indicating apparent divergence. Regarding the junction temperature estimation, both power pulses are fed to the SPICE thermal model, leading to the obtained thermal response. It should be mentioned that the experimental single avalanche pulse refers to the last measurement of Figure 4.20a. The subsequent avalanche pulse essentially causes the DUT to fail, as shown in Figure 4.20c. As analyzed in [49, 109], a curve fitting model can be applied to estimate the junction temperature based on the captured drain-source voltage, since it depends on the temperature and the drain current. This methodology could be used in-situ for the indirect junction temperature estimation. A similar approach could also be applied to the SC test.

7.2 Conclusion

The major objective of this dissertation is to develop a reliability stress test bench aiming at studying the wear-out mechanisms of discrete high voltage power semiconductors under specific dedicated stress test conditions. The complexity of the actual application setup may mask the intrinsic failure mechanisms under study, and therefore the reliability stress test bench should provide a simplified test environment. To this end, a double pulse tester is introduced as the main topology due to its simplicity. An additional half bridge is also added to protect the setup against catastrophic failures. As demonstrated later on, this half bridge is actively employed to perform the repetitive DP test, in the prospect of accelerating the stress conditions as well as minimizing the input power supplied by the PSU, and thus it enables a multi-channel functionality with less required power supply capacity.

This test bench has also to satisfy certain requirements in terms of set-up effort and multi-channel

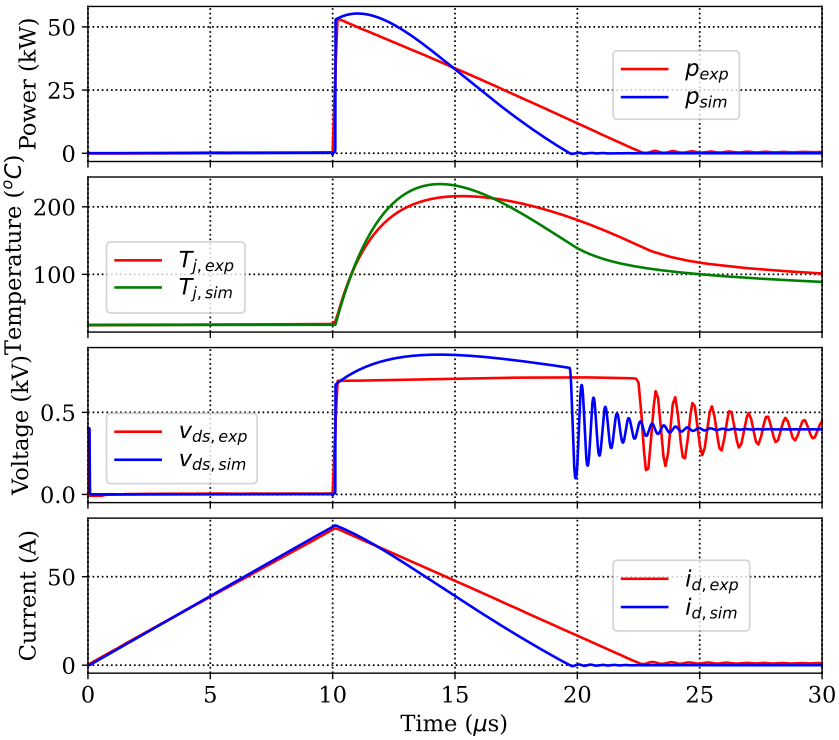


Figure 7.2: UIS comparison of a superjunction Si MOSFET with its counterpart SPICE model.

functionality. The first feature is its modularity, which is achieved by introducing the DUT board, the load interface and even the configurable gate driver. In particular, different DUT boards can be realized by mounting various types of discrete packages and technologies. Likewise, various loads can be implemented through the allocated load interface to perform the stress tests. As for the gate drive conditions, adjustable voltage rails are used to preset the gate voltages, whilst the switching speed can be either configured via the DUT board interface by mounting suitable gate resistors or by employing the developed CSGD able to set the switching speed completely via software programming without any hands-on effort. The other significant feature is its scalability, to this end a stress board has been constructed fitting into a subrack system of a 19-inch tower, which can be readily scaled to form a multi-channel test bench with the utter goal of meaningful statistical analysis over a sufficient number of DUTs. This standardised solution offers an easy to realize solution, and, as a result it enables its rapid scalability. The last characteristic is its redundancy, meaning that during a catastrophic failure of the DUT the protection scheme should be immediately activated not only to reduce the energy dissipation through the failed DUT, but also to maintain uninterrupted parallel operation of the multi-channel system.

One of the system's design challenges is to ensure its reliability and long lasting operation. Therefore, several design considerations should be followed, as already shown. More specifically, the GS has to perform multiple tasks, since beside its protective function it can be actively used in all stress tests, and therefore its final mission profile becomes quite complex. For example, its SC robustness against SC type II has been extensively investigated by adding a two level turn-off in conjugation with additional measures to reduce the stress. Moreover, its ability to turn off at high currents and voltages without being overheated is of paramount importance for the full bridge based DP test. In principle, it is of vital importance to sustain the average temperature and ΔT at relatively low levels to minimize

the accumulated damage. This measure can alleviate the thermo-mechanical stress related degradation effects. Another potential issue is the latch-up effect as stated by the manufacturer, requiring to increase the gate resistance. It is therefore apparent that the employed technology necessitates further investigations in terms of its actual capabilities, which needs to be investigated during the future practical implementation of the test system.

In conclusion, this thesis discloses the pros and cons of different stress test concepts using the introduced topology and their manufacturing feasibility. However, the primary focus is on the repetitive DP testing. A scalable single channel hardware solution is finally proposed and its performance is demonstrated via several experimental examples. The critical performance indicators together with the design trade-offs are extensively emphasized and proposal for future system improvements are given.

Bibliography

[1] K. Patmanidis, M. Glavanovics, A. Georgakas, and A. Muetze, "Modular dynamic pulse stress test system for discrete high power semiconductors," *Microelectronics Reliability*, vol. In press, 2020.

[2] K. Patmanidis, M. Glavanovics, and A. Muetze, "Scalable multitasking dynamic pulse based reliability stress test for high voltage discrete semiconductors," in *Proceedings of EPE'21*, 2021.

[3] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, *Semiconductor Power Devices: Physics, Characteristics, Reliability*. Springer Berlin Heidelberg, 2011. [Online]. Available: https://books.google.it/books?id=345uBEHneEgC

[4] H. Chung, H. Wang, F. Blaabjerg, and M. Pecht, *Reliability of Power Electronic Converter Systems*, ser. Energy Engineering. Institution of Engineering and Technology, 2015. [Online]. Available: https://books.google.at/books?id=Ix4WrgEACAAJ

[5] P. P. O'Connor and A. Kleyner, *Practical Reliability Engineering*, 5th ed. Wiley Publishing, 2012. [Online]. Available: https://books.google.at/books?id=V1Ttz5L_V50C

[6] H. Wang, M. Liserre, F. Blaabjerg, P. de Place Rimmen, J. B. Jacobsen, T. Kvisgaard, and J. Landkildehus, "Transitioning to Physics-of-Failure as a Reliability Driver in Power Electronics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 1, pp. 97–114, March 2014.

[7] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition Monitoring for Device Reliability in Power Electronic Converters: A Review," *IEEE Transactions on Power Electronics*, vol. 25, no. 11, pp. 2734–2752, Nov. 2010.

[8] R. Sleik, M. Glavanovics, Y. Nikitin, M. D. Bernardo, A. Muetze, and K. Krischan, "Performance enhancement of a modular test system for power semiconductors for HTOL testing by use of an embedded system," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, Sept 2017, pp. P.1–P.8.

[9] R. Sleik, "System Level Reliability Testing Under Application Stress Conditions," Ph.D. dissertation, Graz University of Technology, Jun. 2018.

[10] S. R. Bahl, D. Ruiz, and D. S. Lee, "Product-level reliability of GaN devices," in *2016 IEEE International Reliability Physics Symposium (IRPS)*, April 2016, pp. 4A–3–1–4A–3–6.

[11] R. Sleik, M. Glavanovics, S. Einspieler, A. Muetze, and K. Krischan, "Modular Test System Architecture for Device, Circuit and System Level Reliability Testing and Condition Monitoring," *IEEE Transactions on Industry Applications*, vol. 53, pp. 5698–5708, Nov. 2017.

[12] B. Steinwender, M. Glavanovics, and W. Elmenreich, "Executable Test Definition for a State Machine Driven Embedded Test Controller Module," in *Proceedings of the 13th IEEE International Conference on Industrial Informatics*, 2015.

[13] B. Steinwender, "A Distributed Controller Network for Modular Power Stress Tests," Ph.D. dissertation, Alpen-Adria-Universität Klagenfurt, Jun. 2016.

[14] T. H. Kist, "Design of an Intelligent Current Controlled Gate Driver for Flexible Stress Testing of Discrete High Power Semiconductors," Master's thesis, Ostbayerische Technische Hochschule Regensburg, 2019.

[15] A. Georgakas, "Development and Evaluation of a Reliability Stress Test System," Master's thesis, Aristotle University of Thessaloniki, 2020.

[16] K. Patmanidis, T. Kist, M. Glavanovics, and A. Muetze, "Configurable gate driver for a stress test bench of newly developed discrete silicon power devices," *Microelectronics Reliability*, vol. 124, p. 114283, 2021. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026271421002493

[17] C. Durand, M. Klingler, C. Daniel, and H. Naceur, "Power Cycling Reliability of Power Module: A Survey," *IEEE Transactions on Device and Materials Reliability*, vol. 16, no. 1, pp. 80–97, Jan. 2016.

[18] S. Baba, A. Gieraltowski, M. Jasinski, F. Blaabjerg, A. S. Bahman, and M. Zelechowski, "Active Power Cycling Test Bench for SiC Power MOSFETs—Principles, Design, and Implementation," *IEEE Transactions on Power Electronics*, vol. 36, no. 3, pp. 2661–2675, March 2021.

[19] F. Forest, J. . Huselstein, S. Faucher, M. Elghazouani, P. Ladoux, T. A. Meynard, F. Richardeau, and C. Turpin, "Use of opposition method in the test of high-power electronic converters," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 2, pp. 530–541, April 2006.

[20] F. Forest, A. Rashed, J.-J. Huselstein, T. Martiré, and P. Enrici, "Fast power cycling protocols implemented in an automated test bench dedicated to IGBT module ageing," *Microelectronics Reliability*, vol. 55, no. 1, pp. 81–92, Jan. 2015.

[21] U. Choi, S. Jørgensen, and F. Blaabjerg, "Advanced Accelerated Power Cycling Test for Reliability Investigation of Power Device Modules," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8371–8386, Dec 2016.

[22] U. Choi, F. Blaabjerg, and F. Iannuzzo, "Advanced power cycler with intelligent monitoring strategy of IGBT module under test," *Microelectronics Reliability*, vol. 76-77, pp. 522–526, 2017.

[23] U. Choi, F. Blaabjerg, and S. Jørgensen, "Power Cycling Test Methods for Reliability Assessment of Power Device Modules in Respect to Temperature Stress," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2531–2551, March 2018.

[24] M. Dbeiss and Y. Avenas, "Power Semiconductor Ageing Test Bench Dedicated to Photovoltaic Applications," *IEEE Transactions on Industry Applications*, vol. 55, no. 3, pp. 3003–3010, May 2019.

[25] A. Amoiridis, A. Anurag, P. Ghimire, S. Munk-Nielsen, and N. Baker, "Vce-based chip temperature estimation methods for high power IGBT modules during power cycling - A comparison," in *Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on*, Sep. 2015, pp. 1–9.

[26] U. Government, *Power MOSFET Thermal Instability Operation Characterization Support*. General Books, 2011. [Online]. Available: https://books.google.at/books?id=ktLbygAACAAJ

[27] P. Spirito, G. Breglio, V. d'Alessandro, and N. Rinaldi, "Analytical model for thermal instability of low voltage power MOS and SOA in pulse operation," in *Proceedings of the 14th International Symposium on Power Semiconductor Devices and Ics*, June 2002, pp. 269–272.

[28] Z. Zhang, B. Guo, F. F. Wang, E. A. Jones, L. M. Tolbert, and B. J. Blalock, "Methodology for Wide Band-Gap Device Dynamic Characterization," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9307–9318, Dec 2017.

[29] A. Ghosh, C. N. Man Ho, and J. Prendergast, "A Cost-effective, Compact, Automatic Testing System for Dynamic Characterization of Power Semiconductor Devices," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2019, pp. 2026–2032.

[30] Q. Ma, L. Zhang, A. Q. Huang, and M. Lee, "A GUI Based Automatic Tester with A Novel Heating Method for Power Semiconductor Device Dynamic Measurement," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 3597–3601.

[31] A. Marzoughi, R. Burgos, and D. Boroyevich, "Characterization and comparison of latest generation 900-V and 1.2-kV SiC MOSFETs," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2016, pp. 1–8.

[32] R. Li, X. Wu, S. Yang, and K. Sheng, "Dynamic on-State Resistance Test and Evaluation of GaN Power Devices Under Hard- and Soft-Switching Conditions by Double and Multiple Pulses," *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1044–1053, Feb 2019.

[33] T. Yao and R. Ayyanar, "A Multifunctional Double Pulse Tester for Cascode GaN Devices," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9023–9031, Nov 2017.

[34] S. Bahl, "Application-relevant Qualification of Emerging Semiconductor Power Devices," in *2016 Applied Power Electronics Conference (APEC), SLYY091*, March 2016. [Online]. Available: https://www.ti.com/lit/wp/slyy091/slyy091.pdf?ts=1616507303096&ref_url=https%253A%252F%252Fwww.google.com%252F

[35] O. Slobodyan, T. Smith, J. Flicker, S. Sandoval, C. Matthews, M. Van Heukelom, and S. Atcitty, "Hard-switching reliability studies of 1200 V vertical GaN PiN diodes," *MRS Communications*, vol. 8, no. 4, p. 1413–1417, 2018.

[36] *JEP180, Guideline for Switching Reliability Evaluation Procedures for Gallium Nitride Power Conversion Devices*, JEDEC Solid State Technology Association JEDEC Standard, 2020. [Online]. Available: https://www.jedec.org

[37] V. Bolloju and J. Yang, "Influence of short circuit conditions on IGBT short circuit current in motor drives," in *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2011, pp. 1675–1679.

[38] Z. Xu and F. Wang, "Experimental investigation of Si IGBT short circuit capability at 200°C," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb 2012, pp. 162–168.

[39] F. Iannuzzo, "Short-circuit robustness assessment in power electronic modules for megawatt applications," *Facta universitatis - series: Electronics and Energetics*, vol. 29, pp. 35–47, 01 2016.

[40] H. Du, P. D. Reigosa, F. Iannuzzo, and L. Ceccarelli, "Impact of the Case Temperature on the Reliability of SiC MOSFETs Under Repetitive Short Circuit Tests," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2019, pp. 332–337.

[41] D. Schleisser, D. Ahlers, M. Eicher, and M. Pürschel, "Repetitive avalanche of automotive MOSFETs," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, Sep. 2013, pp. 1–7.

[42] X. Zhou, H. Su, R. Yue, G. Dai, J. Li, Y. Wang, and Z. Yu, "A Deep Insight Into the Degradation of 1.2-kV 4H-SiC MOSFETs Under Repetitive Unclamped Inductive Switching Stresses," *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 5251–5261, June 2018.

[43] C. DiMarino and B. Hull, "Characterization and prediction of the avalanche performance of 1.2 kV SiC MOSFETs," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Nov 2015, pp. 263–267.

[44] *JESD24-5 - Single Pulse Unclamped Inductive Switching (UIS) Avalanche Test Method*, JEDEC Solid State Technology Association JEDEC Standard, Oct 2002. [Online]. Available: https://www.jedec.org

[45] L. Yang, A. Fayyaz, and A. Castellazzi, "Characterization of high-voltage SiC MOSFETs under UIS avalanche stress," in *7th IET International Conference on Power Electronics, Machines and Drives (PEMD 2014)*, April 2014, pp. 1–5.

[46] I. Dchar, M. Zolkos, C. Buttay, and H. Morel, "Robustness of SiC MOSFET under avalanche conditions," in *APEC*, Tampa, FL, United States, Mar. 2017, pp. 2263–2268. [Online]. Available: https://hal.archives-ouvertes.fr/hal-01535735

[47] S. Liu, C. Gu, J. Wei, Q. Qian, W. Sun, and A. Q. Huang, "Repetitive Unclamped-Inductive-Switching-Induced Electrical Parameters Degradations and Simulation Optimizations for 4H-SiC MOSFETs," *IEEE Transactions on Electron Devices*, vol. 63, no. 11, pp. 4331–4338, Nov 2016.

[48] "Some key facts about avalanche," Infineon Technologies AG, Jan 2017. [Online]. Available: https://www.infineon.com

[49] N. Ren, K. L. Wang, J. Wu, H. Xu, and K. Sheng, "Failure Mechanism Analysis of SiC MOSFETs in Unclamped Inductive Switching Conditions," in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 2019, pp. 183–186.

[50] N. Ren, H. Hu, K. L. Wang, Z. Zuo, R. Li, and K. Sheng, "Investigation on single pulse avalanche failure of 900V SiC MOSFETs," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 2018, pp. 431–434.

[51] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, 1st ed. Springer Publishing Company, Incorporated, 2008.

[52] A. Benmansour, S. Azzopardi, J. Martin, and E. Woirgard, "Failure mechanisms of Trench IGBT under various short-circuit conditions," in *2007 IEEE Power Electronics Specialists Conference*, June 2007, pp. 1923–1929.

[53] S. Lefebvre, Z. Khatir, and F. Saint-Eve, "Experimental behavior of single-chip IGBT and COOLMOS devices under repetitive short-circuit conditions," *IEEE Transactions on Electron Devices*, vol. 52, no. 2, pp. 276–283, Feb 2005.

[54] M. Arab, S. Lefebvre, Z. Khatir, and S. Bontemps, "Experimental investigations of trench field stop IGBT under repetitive short-circuits operations," in *2008 IEEE Power Electronics Specialists Conference*, June 2008, pp. 4355–4360.

[55] Z. Khatir, S. Lefebvre, and F. Saint-Eve, "Experimental and numerical investigations on delayed short-circuit failure mode of single chip IGBT devices," *Microelectronics Reliability*, vol. 47, no. 2, pp. 422–428, 2007. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026271406001235

[56] Y. Chen, W. Li, F. Iannuzzo, H. Luo, X. He, and F. Blaabjerg, "Investigation and Classification of Short-Circuit Failure Modes Based on Three-Dimensional Safe Operating Area for High-Power IGBT Modules," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1075–1086, Feb 2018.

[57] P. Luo, S. N. E. Madathil, S.-I. Nishizawa, and W. Saito, "Turn-OFF dV/dt Controllability in 1.2-kV MOS-Bipolar Devices," *IEEE Transactions on Power Electronics*, vol. 36, no. 3, pp. 3304–3311, March 2021.

[58] W. Saito and S.-I. Nishizawa, "Surface Buffer IGBT for High Total Performance," *IEEE Transactions on Electron Devices*, vol. 67, no. 8, pp. 3263–3269, Aug 2020.

[59] T. Laska, F. Hille, F. Pfirsch, R. Jereb, and M. Bassler, "Long Term Stability and Drift Phenomena of different Trench IGBT Structures under Repetitive Switching Tests," in *Proceedings of the 19th International Symposium on Power Semiconductor Devices and IC's*, May 2007, pp. 1–4.

[60] W. Yang, C. Wang, R. Zhang, L. Su, and Q. Zhang, "A Dynamic Self-Clamping Caused by Dynamic Avalanche During the Turn-Off of PT-IGBT," *IEEE Transactions on Electron Devices*, vol. 68, no. 1, pp. 208–215, Jan 2021.

[61] S. Geissmann, L. D. Michielis, C. Corvasce, M. Rahimo, and M. Andenna, "Extraction of dynamic avalanche during IGBT turn off," *Microelectronics Reliability*, vol. 76-77, pp. 495–499, 2017. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026271417303992

[62] G. De Falco, A. Würfel, L. Maresca, N. Kaminski, A. Irace, and D. Silber, "Effects of current filaments during dynamic avalanche on the collector-emitter-voltage of high voltage Trench-IGBTs," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Sep. 2015, pp. 1–9.

[63] C. Sandow, P. Brandt, H. . P. Felsl, F. . J. Niedernostheide, F. Pfirsch, H. . J. Schulze, A. Stegner, F. Umbach, F. Santos, and W. Wagner, "IGBT with superior long-term switching behavior by asymmetric trench oxide," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 2018, pp. 24–27.

[64] H. Luo, F. Iannuzzo, and M. Turnaturi, "Role of Threshold Voltage Shift in Highly Accelerated Power Cycling Tests for SiC MOSFET Modules," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1657–1667, June 2020.

[65] U. Hecht and U. Scheuemann, "Power cycling lifetime of advanced power modules for different temperature swings," in *PCIM Europe, 2002, International European Power Electronics Conference, 45, PCIM, International Intelligent Motion Conference, 39, European Power Quality Conference, 8*, 2002, pp. 1–6. [Online]. Available: https://www.tib.eu/de/suchen/id/tema%3ATEMA20030307178

[66] J. P. Kozak, R. Zhang, H. Yang, K. D. Ngo, and Y. Zhang, "Robustness Evaluation and Degradation Mechanisms of SiC MOSFETs Overstressed by Switched Stimuli," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2020, pp. 1135–1140.

[67] J. P. Kozak, R. Zhang, J. Liu, K. D. T. Ngo, and Y. Zhang, "Physics of Degradation in SiC MOSFETs Stressed by Overvoltage and Overcurrent Switching," in *2020 IEEE International Reliability Physics Symposium (IRPS)*, April 2020, pp. 1–6.

[68] U.-M. Choi, F. Blaabjerg, and S. Jørgensen, "Study on Effect of Junction Temperature Swing Duration on Lifetime of Transfer Molded Power IGBT Modules," *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 6434–6443, Aug 2017.

[69] U. Scheuermann and U. Hecht, "Power cycling lifetime of advanced power modules for different temperature swings," May 2002.

[70] D. Baba, "Benefits of a multiphase buck converter," Texas Instruments Incorporated, 2012. [Online]. Available: https://www.ti.com

[71] J.-P. Lee, H. Cha, D. Shin, K.-J. Lee, D.-W. Yoo, and J.-Y. Yoo, "Analysis and Design of Coupled Inductors for Two-Phase Interleaved DC-DC Converters," *Journal of Power Electronics*, vol. 13, 05 2013.

[72] R. Bidenbach, "How to Use LTspice Simulations to Account for the Effect of Voltage Dependence," Analog Devices, August 2021.

[73] M. Newville, T. Stensitzki, D. B. Allen, and A. Ingargiola, "LMFIT: Non-Linear Least-Square Minimization and Curve-Fitting for Python," Sep 2014. [Online]. Available: https://doi.org/10.5281/zenodo.11813

[74] "PLECS 4.5.7 Manual," Plexim, Jan 2021. [Online]. Available: https://www.plexim.com/download/documentation

[75] "Technical Introduction," Fischer Electronik. [Online]. Available: https://www.fischerelektronik.de/en/service-en/technical-information/thermal-resistance-of-a-heatsink

[76] Y. Gerstenmaier, W. Kiffe, and G. Wachutka, "Combination of thermal subsystems modeled by rapid circuit transformation," in *2007 13th International Workshop on Thermal Investigation of ICs and Systems (THERMINIC)*, Sep. 2007, pp. 115–120.

[77] U. Drofenik and J. Kolar, "A Thermal Model of a Forced-Cooled Heat Sink for Transient Temperature Calculations Employing a Circuit Simulator," *Ieej Transactions on Industry Applications*, vol. 126, Oct 2006.

[78] X. Tang, Y. Pan, P. Zhang, and Z. Zhao, "A new method to extract stray inductance in IGBTs' Dynamic testing platform," *IOP Conference Series: Materials Science and Engineering*, vol. 439, p. 022025, Nov 2018.

[79] LEM, "Isolated current and voltage transducers Characteristics - Applications - Calculations," LEM, techreport, 2010. [Online]. Available: https://www.lem.com/en/file/3139/download

[80] N. Mohan, T. Undeland, and W. Robbins, *Power Electronics: Converters, Applications, and Design*, ser. Power Electronics: Converters, Applications, and Design. John Wiley & Sons, 2003, no. Bd. 1. [Online]. Available: https://books.google.at/books?id=wmTTnQEACAAJ

[81] S. Mocevic, J. Wang, R. Burgos, D. Boroyevich, C. Stancu, M. Jaksic, and B. Peaslee, "Comparison between desaturation sensing and Rogowski coil current sensing for shortcircuit protection of 1.2 kV, 300 A SiC MOSFET module," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018, pp. 2666–2672.

[82] R. Locher and O. Zschieschang, "IXBH40N160 BiMOSFET Developed for High Voltage, High Frequency Applications," IXYS, application note, IXAN0016. [Online]. Available: https://www.ixyspower.com/images/technical_support

[83] L. Helong, "Parallel Connection of Silicon Carbide MOSFETs for Multichip Power Modules," Ph.D. dissertation, Aalborg University Aalborg, nov 2015.

[84] T. Basler, J. Lutz, T. Brückner, and R. Jakob, "IGBT Self-Turn-Off under Short-Circuit Condition," in *10th International Seminar on Power Semiconductors (ISPS)*, Sept 2010.

[85] V. Sung and W. G. Odendaal, "Litz Wire Pulsed Power Air Core Coupled Inductor," *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3385–3393, July 2015.

[86] K. W. Whites, "1 - Magnetostatics," in *The Electrical Engineering Handbook*, W.-K. CHEN, Ed. Burlington: Academic Press, 2005, pp. 479–497. [Online]. Available: https://www.sciencedirect.com/science/article/pii/B9780121709600500372

[87] A. Massarini and M. Kazimierczuk, "Self-capacitance of inductors," *IEEE Transactions on Power Electronics*, vol. 12, no. 4, pp. 671–676, July 1997.

[88] B. X. Foo, A. L. F. Stein, and C. R. Sullivan, "A step-by-step guide to extracting winding resistance from an impedance measurement," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 861–867.

[89] P. Thummala, H. Schneider, Z. Zhang, and M. A. E. Andersen, "Investigation of Transformer Winding Architectures for High-Voltage (2.5 kV) Capacitor Charging and Discharging Applications," *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5786–5796, Aug 2016.

[90] J. Biela and J. Kolar, "Using transformer parasitics for resonant converters - a review of the calculation of the stray capacitance of transformers," in *Fourtieth IAS Annual Meeting. Conference Record of the 2005 Industry Applications Conference, 2005.*, vol. 3, Oct 2005, pp. 1868–1875 Vol. 3.

[91] J. Smajic, M. Bucher, T. Franz, B. Cranganu-Cretu, A. Shoory, and J. Tepper, "Modeling of Frequency Dependent Parameters in Time Domain High Frequency Transformer Simulations," *Procedia Engineering*, vol. 202, pp. 251–263, 2017, special issue of the 4th International Colloquium "Transformer Research and Asset Management". [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1877705817342510

[92] "Impedance Measurement Handbook, A guide to measurement technology and techniques," Keysight Technologies, November 2016.

[93] J. Wang, H. S.-h. Chung, and R. T.-h. Li, "Characterization and Experimental Assessment of the Effects of Parasitic Elements on the MOSFET Switching Performance," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 573–590, Jan 2013.

[94] M. STOJANOVIC, F. Lafon, R. Perdriau, and M. Ramdani, "Self-Inductance Prediction for Straight and Toroidal Air Core Coils ," in *CEM 2018*, Paris, France, Jul 2018. [Online]. Available: https://hal.archives-ouvertes.fr/hal-01810360

[95] Y. Lobsiger and J. W. Kolar, "Closed-Loop di/dt and dv/dt IGBT Gate Driver," *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 3402–3417, June 2015.

[96] L. Dang, H. Kuhn, and A. Mertens, "Digital Adaptive Driving Strategies for High-Voltage IGBTs," *IEEE Transactions on Industry Applications*, vol. 49, no. 4, pp. 1628–1636, July 2013.

[97] F. Zhang, X. Yang, Y. Ren, L. Feng, W. Chen, and Y. Pei, "Advanced Active Gate Drive for Switching Performance Improvement and Overvoltage Protection of High-Power IGBTs," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 3802–3815, May 2018.

[98] Y. Ling, Z. Zhao, and Y. Zhu, "A Self-Regulating Gate Driver for High-Power IGBTs," *IEEE Transactions on Power Electronics*, vol. 36, no. 3, pp. 3450–3461, March 2021.

[99] L. Shu, J. Zhang, F. Peng, and Z. Chen, "Active Current Source IGBT Gate Drive With Closed-Loop di/dt and dv/dt Control," *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3787–3796, May 2017.

[100] J. Groeger, A. Schindler, B. Wicht, and K. Norling, "Optimized dv/dt, di/dt sensing for a digitally controlled slope shaping gate driver," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 3564–3569.

[101] F. Stamer, A. Liske, and M. Hiller, "New Gate Driver for online adjustable switching behavior of Insulated Gate Bipolar Transistors (IGBTs)," in *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, Sep. 2019, pp. P.1–P.10.

[102] C. Luedecke, G. Engelmann, and R. W. De Doncker, "Optimized IGBT Turn-On Switching Performance Using the Full Device Safe Operating Area," in *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, May 2019, pp. 1–8.

[103] J. Gottschlich and R. W. De Doncker, "A programmable gate driver for power semiconductor switching loss characterization," in *2015 IEEE 11th International Conference on Power Electronics and Drive Systems*, June 2015, pp. 456–461.

[104] M. Tian, V. Visvanathan, J. Hantgan, and K. Kundert, "Striving for small-signal stability," *IEEE Circuits and Devices Magazine*, vol. 17, no. 1, pp. 31–41, Jan 2001.

[105] J. Fu, Z. Zhang, Y.-F. Liu, P. C. Sen, and L. Ge, "A New High Efficiency Current Source Driver With Bipolar Gate Voltage," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 985–997, Feb 2012.

[106] D. Heer and R. Bayerer, "Simple turn-off description of trench-field-stop IGBT - IGBT 3/3.3kV," in *PCIM Europe, International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2012*. Berlin, Offenbach: VDE-Verlag, 2012, pp. 938–943.

[107] J. Hancock, F. Stueckler, and E. Vecino, "CoolMOS C7: Mastering the art of quickness a technology description and design guide," Infineon Technologies Austria AG, April 2013.

[108] K. Keesman, *System Identification: An Introduction*, ser. Advanced Textbooks in Control and Signal Processing. Springer London, 2011. [Online]. Available: https://books.google.at/books?id=gHssIP_dDwUC

[109] A. Agnone, F. Chimento, S. Musumeci, A. Raciti, and G. Privitera, "A New Thermal Model for Power Mosfet Devices Accounting for the Behavior in Unclamped Inductive Switching," in *2007 IEEE Power Electronics Specialists Conference*, June 2007, pp. 1006–1012.