Mehdi Gholizadeh

Advanced Techniques in Electromagnetic Compatibility: Applications in GaN-Based Power Converters and ESD-Sensitive Electronic Systems

DOCTORAL THESIS

to achieve the university degree of

Doctor of Philosophy

in

Electrical Engineering

submitted to

Graz University of Technology

Advisor

David Pommerenke
Institute of Electronics, Graz University of Technology

Reviewer

Ramiro Serra
Department of Electrical Engineering, Eindhoven University of Technology

Graz, July 2025

Affidavit

I declare that I have authored this thesis independently, that I have not used other than the declared sources/resources, and that I have explicitly indicated all material which has been quoted either literally or by content from the sources used. The text document uploaded to TUGRAZonline is identical to the present PhD thesis.

Date	Signature

Abstract

The push toward high-efficiency, high-frequency power conversion and the increasing susceptibility of electronic systems to electromagnetic disturbances has intensified the demand for precise electromagnetic compatibility (EMC) modeling and measurement techniques. This thesis addresses these challenges through several contributions that advance the prediction, probing, and analysis of electromagnetic interference (EMI) and electrostatic discharge (ESD) effects, focusing on GaN-based power converters and ESD-sensitive structures.

A central theme in this work is the accurate modeling of EMI in GaN transistors. A behavioral modeling framework is proposed that adapts a simplified power MOSFET model to GaN devices, requiring only minimal parameter extraction and demonstrating prediction accuracy up to 300 MHz. Using both circuit simulation and 3D electromagnetic modeling, the influence of layout and DC operating points on conducted emissions is evaluated, showing that a compact model based on three lumped elements and a diode can achieve strong agreement with experimental data.

To improve the predictive fidelity of this model, the resistive loss component of the transistor output capacitance—termed R_{oss}—is introduced and experimentally extracted using a novel S-parameter-based methodology. This parameter, often overlooked in standard models, has been shown to significantly impact the damping of switching oscillations and the suppression of spectral peaks in the 30–150 MHz range. When incorporated into the transistor model, R_{oss} reduces EMI prediction errors by up to 14 dB across the investigated cases, effectively bridging the gap between device-level loss modeling and system-level EMC behavior.

Complementing the modeling work, this thesis introduces a high-impedance voltage probe based on a printed circuit board (PCB) structure, optimized through capacitive symmetry to mitigate distortion and frequency-dependent loading. The probe achieves a flat frequency response with 3 GHz bandwidth and is suitable for high-voltage measurements in GaN switching environments. Building on this, an extended set of PCB-based probes is developed, adding current sensing capability through a low-resistance shunt design with minimal mutual inductance. The integrated voltage and current probes provide reliable waveform acquisition with GHz-level resolution and validate key assumptions in EMI and switching performance analysis.

Finally, the thesis expands its EMC investigation into the domain of ESD susceptibility. It quantifies the voltages induced in PCB traces and flex cables by various near-field probes during scanning procedures. By comparing probe-induced voltages to those caused by a standardized ESD gun, the work offers guidelines for selecting probe types and adjusting test parameters to avoid overstress and false-positive fault detection during compliance evaluation.

Together, these contributions deliver a comprehensive suite of EMC techniques, spanning behavioral modeling, high-speed waveform acquisition, and board-level susceptibility analysis. The outcomes support improved EMI prediction and measurement practices while enhancing the resilience and reliability of next-generation electronic systems across power and signal integrity domains.

Kurzfassung

Der Trend zu hocheffizienter, hochfrequenter Leistungsumwandlung sowie die zunehmende Störanfälligkeit elektronischer Systeme gegenüber elektromagnetischen Einflüssen erfordern präzise Methoden zur Modellierung und Messung der elektromagnetischen Verträglichkeit (EMV). Diese Dissertation greift diese Herausforderungen auf und leistet mehrere Beiträge zur Vorhersage, Messung und Analyse elektromagnetischer Störungen (EMI) und elektrostatischer Entladungen (ESD), mit einem Fokus auf GaN-basierte Leistungswandler und ESD-empfindliche Strukturen.

Ein zentrales Thema dieser Arbeit ist die genaue Modellierung der EMI in GaN-Transistoren. Es wird ein verhaltensbasiertes Modell entwickelt, das auf einem vereinfachten MOSFET-Modell basiert und auf GaN-Bauelemente übertragen wird. Dieses Modell erfordert nur wenige Parameter und ermöglicht die Vorhersage leitungsgebundener Störungen bis 300 MHz. Mit Hilfe von Schaltungssimulationen und 3D-Feldmodellierung wird der Einfluss des Layouts und der Betriebspunkte auf das Störspektrum analysiert. Ein kompakter Modellaufbau mit drei passiven Elementen und einer Diode zeigt dabei eine sehr gute Übereinstimmung mit experimentellen Messungen.

Um die Vorhersagegenauigkeit dieses Modells zu verbessern, wird die Widerstandsverlustkomponente der Ausgangskapazität des Transistors – bezeichnet als R_{OSS} – eingeführt und experimentell mithilfe einer neuartigen, auf S-Parametern basierenden Methodik extrahiert. Dieser Parameter, der in Standardmodellen oft vernachlässigt wird, hat sich als entscheidend für die Dämpfung von Schwingungen beim Schalten sowie für die Unterdrückung von Spektralpeaks im Bereich von 30–150 MHz erwiesen. Wird R_{OSS} in das Transistormodell integriert, reduziert sich der Fehler bei der EMI-Vorhersage in den untersuchten Fällen um bis zu 14 dB und überbrückt damit effektiv die Lücke zwischen verlustbezogener Modellierung auf Bauteilebene und dem EMV-Verhalten auf Systemebene.

Ergänzend zur Modellierung wird eine hochimpedante Spannungsmesssonde auf Leiterplattenbasis vorgestellt, die durch symmetrisches Layout parasitäre Kapazitäten kompensiert und einen flachen Frequenzgang bis 3 GHz erreicht. Diese Sonde eignet sich insbesondere für hochspannende, schnelle Schaltvorgänge in GaN-Systemen. Darauf aufbauend wird ein erweitertes Messsystem entwickelt, das eine Strommesssonde mit niedriger Induktivität ergänzt. Durch die Kombination beider Sonden wird eine simultane Erfassung von Spannungs- und Stromverläufen mit GHz-Bandbreite ermöglicht.

Abschließend untersucht die Arbeit die EMV-Anfälligkeit im Bereich der ESD. Es werden die

durch Nahfeldsonden induzierten Spannungen in Leiterbahnen und Flexkabeln gemessen und mit jenen eines normierten ESD-Simulators verglichen. Die Ergebnisse liefern praxisnahe Empfehlungen zur Auswahl geeigneter Sonden und zur Einstellung sicherer Prüfspannungen, um Überbelastung und Fehldiagnosen bei EMV-Prüfungen auf Board-Level zu vermeiden.

Diese Beiträge liefern ein umfassendes Methodenset zur Modellierung, Messung und Diagnose im Hochfrequenz-EMV-Bereich. Die Arbeit verbindet gerätebezogene Modellierung mit praxisnaher Messtechnik und Systemanalyse und bietet damit eine fundierte Grundlage für die Entwicklung robuster, emissionsarmer elektronischer Systeme der nächsten Generation.

Acknowledgements

The pursuit of this PhD has been a profoundly transformative chapter in my life—technically demanding, personally enriching, and emotionally humbling. I am deeply grateful to all those who supported and encouraged me throughout this journey.

Above all, I extend my heartfelt gratitude to Prof. Dr. David Pommerenke, whose mentorship has been nothing short of exceptional. His profound knowledge, patient guidance, and unwavering belief in my potential have shaped me not only as a researcher but also as a thinker. I could not have asked for a better advisor, and I will carry the lessons learned under his supervision with me throughout my professional and personal life.

I am also sincerely thankful to Dr. Jan Hansen for his generous support and insightful feedback, which proved invaluable during several critical phases of this work. My appreciation also goes to Prof. Dr. Bernd Deutschmann for fostering an open, collaborative, and intellectually stimulating research environment at TU Graz. Special thanks go to my colleagues at Silicon Austria Labs—Herbert Hackl, Ralph Prestros, and Bernhard Auinger—whose expertise, technical input, and cooperation greatly enriched this research.

To my wife, Tara Mortezaei—you have been the quiet, constant force behind everything I have accomplished. Your unwavering love, patience, and belief in me carried me through the most challenging moments. This thesis belongs as much to you as it does to me, and I am eternally grateful for your presence in my life. I am equally indebted to my parents, Fatemeh and Hooshang Gholizadeh, for their unconditional love, sacrifices, and the values they instilled in me. Their lifelong support has been the foundation upon which this achievement stands.

I would also like to thank my colleagues and friends—Sajjad Sadeghi, Seyed Mostafa Mousavi, and Amin Pak—for their insightful discussions, encouragement, and friendship throughout this journey.

To the best of my knowledge and with deep appreciation, I would like to acknowledge everyone who helped me—whether in significant ways or through small but meaningful acts—on the path to this degree: David Pommerenke, Jan Hansen, Bernd Deutschmann, Herbert Hackl, Ralph Prestros, Bernhard Auinger, Sajjad Sadeghi, Seyed Mostafa Mousavi, Amin Pak, Ko Odreitz, Christian Riener, Leonhard Petzel, Rui Mi, Daniel Eisenkölbl, and Tim Reisenhofer, Fatemeh and Hooshang Gholizadeh, Tara Mortezaei.

Contents

1 Introduction

1.1 Background and Motivation

The demand for high-frequency, high-efficiency, and high-density power electronics has led to the increasing use of gallium nitride (GaN) devices in modern converter applications. GaN high-electron-mobility transistors (HEMTs) offer advantages such as lower on-resistance, reduced parasitic capacitance, and negligible reverse recovery charge compared to their silicon (Si) counterparts, making them ideal for fast-switching, compact power systems [15]. These characteristics are particularly beneficial in applications such as electric vehicles and high-frequency soft-switching topologies, where performance and size are critical. However, the high-speed switching transitions inherent to GaN devices result in significant electromagnetic interference (EMI), posing challenges for system-level electromagnetic compatibility (EMC). A tenfold increase in switching speed typically leads to approximately 20 dB higher emissions, making EMC a key design constraint [1]. These emissions can affect adjacent circuits and compromise compliance with regulatory standards such as CISPR 25 [10].

To address these challenges, circuit simulation plays a pivotal role in predicting EMI early in the design process. Physical transistor models—based on semiconductor geometry—offer high fidelity but require extensive parameter extraction, while behavioral models treat the transistor as a black box and emphasize ease of implementation and simulation speed [2], [3]. Behavioral modeling techniques have proven useful across different technologies, including GaN, SiC, and super-junction structures, although the modeling of high-speed GaN devices still faces challenges due to the presence of nonlinear capacitances and parasitic resonances [41].

Among the dynamic characteristics of GaN transistors, losses associated with the output capacitance (C_{OSS}) have become an area of focus. These losses increase with frequency and become a dominant factor in MHz-range switching applications [18]. The loss can be separated into capacitive components—attributed to charge hysteresis effects that become significant above 20 MHz—and resistive components. The latter—commonly termed R_{OSS}—is often neglected in datasheets despite its significant contribution to damping and waveform behavior [25]. Existing models typically assume a lossless charging and discharging of C_{OSS} or simplify the behavior into a passive capacitance in the OFF-state. However, empirical studies have shown that up to 20% of the energy stored in EOSS may be lost during each switching cycle [18]-[24].

Characterizing these behaviors requires high-bandwidth voltage and current measurements. However, commercial high-voltage probes often struggle to achieve bandwidths beyond 100 MHz—particularly at high voltages—due to frequency-dependent loading and parasitic effects [62]–[65]. These limitations are especially critical in applications such as double pulse testing of GaN switches in electric vehicle modules, where accurate waveform reconstruction is essential [47]–[50]. Additionally, since these probes are not integrated into the circuit layout, they increase the complexity of the test setup.

Resistive voltage dividers (RVDs) are frequently used in high-speed environments. However, as frequencies exceed a few MHz, parasitic capacitances across and to ground dominate behavior, reducing measurement fidelity. Design trade-offs between resistance, capacitance, and bandwidth become critical in this regime [59]. In general, increasing input impedance reduces probe bandwidth, and vice versa, making symmetrical PCB layout and parasitic balancing key to achieving reliable GHz-bandwidth measurement performance [62]-[65].

While voltage sensing can typically be performed with minimal disturbance to the circuit, current measurement remains more challenging due to its inherently intrusive nature. Resistive shunts and Rogowski coils offer alternative approaches, each with trade-offs in bandwidth, linearity, and spatial constraints [66]-[84].

Beyond GaN-based power systems, the susceptibility of electronic systems to electrostatic discharge (ESD) remains a critical EMC concern. ESD scanning is widely employed to investigate soft-failure mechanisms, particularly in systems that fail to pass standards such as IEC 61000-4-2 [99]-[100]. Field probes excited by pulsed voltage sources are moved across traces, interconnects, or PCBs to localize sensitivity. However, the exact voltage induced by these probes is often not quantified, and over-injection risks overstressing the system under test [101]-[104].

In summary, the interaction of fast-switching GaN devices, measurement system bandwidth, and system-level ESD susceptibility forms a complex landscape in EMC engineering. The challenges in modeling losses like R_{OSS}, measuring high-speed transients, and characterizing probe-induced disturbances all point to the need for more refined approaches in both simulation and experimentation.

1.2 Objectives of the Dissertation

This dissertation aims to improve electromagnetic compatibility (EMC) engineering across high-speed power and signal systems by addressing predictive modeling, high-bandwidth measurement, and ESD susceptibility characterization. The focus lies in GaN-based power converters and PCB-level electronic interfaces. The core research questions include:

- How can compact transistor models predict conducted EMI in GaN-based converters with minimal input requirements?

- What previously unaccounted loss mechanisms critically affect waveform damping and EMI peaks in GaN switching?
- How can voltage and current waveforms be measured with GHz-level fidelity using compact, manufacturable PCB probes?
- How do voltages induced by ESD field probes compare to those from standardized ESD guns, and what are the implications for test safety and accuracy?

To address these, the dissertation makes the following novel contributions:

- Compact Behavioral Modeling of GaN Transistors for EMI Prediction:

A simplified GaN transistor model is adapted from silicon MOSFET architectures using three lumped elements and a diode. It is designed for rapid, practical prediction of conducted EMI up to 300 MHz using only datasheet data and a single reference waveform. The model includes DC operating point sensitivity and 3D layout parasitic effects, supporting system-level EMI simulation for early-stage design decisions.

- Incorporation of R_{OSS} into EMI-oriented GaN Modeling:

A compact measurement and modeling method is proposed to extract the resistive component of the output capacitance (R_{OSS}) using S-parameter measurements. This parameter is integrated into an LTspice-compatible model and shown to significantly impact oscillation damping and EMI prediction accuracy, particularly in the 30–150 MHz range. Experimental validation across three GaN devices reveals that including ROSS improves prediction error by up to 14 dB.

- Development of a PCB-Based GHz Bandwidth Resistive Voltage Probe:

A compact, high-resistance voltage probe is designed using a symmetrical PCB structure to suppress parasitic capacitance and balance electric fields. The probe achieves 3 GHz bandwidth with a 5 kΩ input resistance, verified through full-wave electromagnetic simulation and experimental testing. Its design offers a scalable, low-distortion voltage sensing solution tailored for fast-switching GaN environments, including high-voltage applications.

- Design of a PCB-Integrated GHz Bandwidth Resistive Current Probe:

A planar, resistive PCB current sensor is introduced with a bandwidth exceeding 1 GHz. The probe is compact and highly integrable, offering minimal parasitic interaction and a wide linear range. Key design trade-offs are explored to support both symmetric and asymmetric test setups. The resulting probe allows simultaneous, non-invasive current waveform capture during rapid switching transitions in GaN-based circuits.

- Evaluation of Probe-Induced Voltages in ESD Susceptibility Testing:

A systematic comparison is conducted between voltages induced by local field probes and those from standard IEC 61000-4-2 ESD gun discharges. Using controlled TLP excitation, this work establishes thresholds for safe probe operation, identifies geometrical effects on coupling behavior, and outlines guidelines for selecting appropriate probes and tuning voltage levels during ESD susceptibility scans.

Together, these contributions form an integrated approach to modern EMC challenges—linking predictive device modeling, GHz-class instrumentation, and practical susceptibility diagnostics. The work supports more reliable, simulation-informed design and testing for fast-switching power systems and sensitive electronic platforms.

2 Cumulative Part of the Dissertation

2.1 List of Accepted/Under Review Publications

2.1.1 1st Author

- ESD Susceptibility Analysis: Coupling to Traces and Interconnect
  2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium
- A PCB Based High Resistance GHz Bandwidth Voltage Pick Up for Detecting Switching Voltage
  2023 International Symposium on Electromagnetic Compatibility – EMC Europe
- Modeling a GaN Transistor and its Impact on Conducted Emission up to 300 MHz
  2023 International Symposium on Electromagnetic Compatibility – EMC Europe
- PCB Integrated GHz Bandwidth Resistive Voltage and Current Probes for Characterization of Wide Bandgap Semiconductor Devices
  IEEE Transactions on Instrumentation and Measurement (accepted on July 13, 2025)
- Modeling and Experimental Characterization of R_{OSS} for EMI Prediction in GaN-based Power Converters
  IEEE Transactions on Power Electronics (under review)

2.1.2 Co-Author

- Mode Stirred Chamber Measurement of GHz Emissions of Wireless Power Transfer Systems
  2022 International Symposium on Electromagnetic Compatibility–EMC Europe
- Modular Measurement System for System-Efficient ESD Design on System and Component Level
  IEEE Transactions on Electromagnetic Compatibility
- Configurable resonant and broadband magnetic near-field probe
  2023 International Symposium on Electromagnetic Compatibility – EMC Europe

- On the Simulation of Conducted Emission of a Flyback Converter using LTSpice
  2024 International Symposium on Electromagnetic Compatibility – EMC Europe

- An Insight into the Practical Problems of Near-field to Far-field Transformation in the Time Domain for EMI Test
  2024 International Symposium on Electromagnetic Compatibility – EMC Europe

- Mechanisms for Unwanted Magnetic Field Coupling to a Shielded Magnetic Near-Field Probe
  IEEE Transactions on Electromagnetic Compatibility

- A Simple Method to Build a Linear Circuit Model for a Multi-Winding Transformer Used in EMI/EMC Analysis
  IEEE Letters on Electromagnetic Compatibility Practice and Applications

- Investigating the Challenges of Near-Field to Far-Field Transformation at Low Frequencies in Electromagnetic Compatibility Testing
  2025 International Symposium on Electromagnetic Compatibility – EMC Europe

- Localizing Harmonics Source on Large Conductor Based on Near-field Scanning
  2025 International Symposium on Electromagnetic Compatibility – EMC Europe

2.2 Dissertation Reuse Permission Grant by IEEE

Requirements to be followed when using any portion (e.g., figure, graph, table, or textual material) of an IEEE copyrighted paper in a thesis:

1. In the case of textual material (e.g., using short quotes or referring to the work within these papers) users must give full credit to the original source (author, paper, publication) followed by the IEEE copyright line © 2011 IEEE.
2. In the case of illustrations or tabular material, we require that the copyright line © [Year of original publication] IEEE appear prominently with each reprinted figure and/or table.
3. If a substantial portion of the original paper is to be used, and if you are not the senior author, also obtain the senior author's approval.

Requirements to be followed when using an entire IEEE copyrighted paper in a thesis:

1. The following IEEE copyright/ credit notice should be placed prominently in the references: © [year of original publication] IEEE. Reprinted, with permission, from [author names, paper title, IEEE publication title, and month/year of publication]
2. Only the accepted version of an IEEE copyrighted paper can be used when posting the paper or your thesis on-line.
3. In placing the thesis on the author's university website, please display the following message in a prominent place on the website: In reference to IEEE copyrighted material which is used with permission in this thesis, the IEEE does not endorse any of [university/educational entity's name goes here]'s products or services. Internal or personal use of this material is permitted. If interested in

reprinting/republishing IEEE copyrighted material for advertising or promotional purposes or for creating new collective works for resale or redistribution, please go to http://www.ieee.org/publications_standards/publications/rights/rights_link.html to learn how to obtain a License from RightsLink.

If applicable, University Microfilms and/or ProQuest Library, or the Archives of Canada may supply single copies of the dissertation.

2.3 Modeling a GaN Transistor and its Impact on Conducted Emission up to 300 MHz

M. Gholizadeh, K. Odreitz, C. Riener, A. Pak, D. Pommerenke, and J. Hansen, "Modeling a GaN transistor and its impact on conducted emission up to 300 MHz," in *Proc. 2023 Int. Symp. Electromagn. Compat. (EMC Europe)*, Sep. 4, 2023, pp. 1–6.

2.3.1 Abstract

Accurate transistor models in the wide frequency range are essential for the prediction of electromagnetic interference. This paper investigates the applicability of a silicon power MOSFET behavioral model to GaN transistors and shows which parameters are important for modeling high-frequency emissions. In the tested case we show that GaN modeling is feasible up to 300MHz using datasheet information and a single measurement. In addition, a simplified power MOSFET model is proposed that requires only three lumped element values and an ideal diode. We also investigate the impact of the layout by 3D simulations, the impact of two DC voltage levels, and we compare the simulated results to measurements.

2.3.2 Introduction

The development of gallium nitride (GaN) devices has been driven by the increasing demand for power electronic devices with new specifications such as high frequencies, voltages, temperatures, and high current densities. GaN is the technology of choice for fast switching frequencies, offering the highest efficiency and power density at an optimized total cost for power applications. However, fast switching comes at the price of higher electromagnetic emissions: a factor of 10 faster rise time results in about 20 dB higher emissions at high frequencies [1]. The number of redesigns should be kept to a minimum as they are time-consuming and costly. Therefore, circuit simulations are used, supplemented by parasitic elements to account for the electromagnetic properties of the electromechanical setup of the test system.

Transistor modeling usually follows one of two approaches: physical or behavioral. Physical models are created with numerous parameters because they are based on the semiconductor structure. Therefore, knowledge of the internal geometry and material is required in order to extract these parameters [2]. Behavioral models, on the other hand, treat the chip as a black box where only the pins are accessible. A behavioral metal–oxide–semiconductor field-effect transistor (MOSFET) model, including a comparison with physical models, is presented by Turzynski and Kulesza [3].

Ideally, a universal behavioral model must satisfy several requirements. First, it must provide high accuracy in fast simulation times. Second, the lumped-element model must not suffer from convergence problems in a SPICE simulation. Third, it is advantageous if it is independent of semiconductor technology such as GaN, silicon carbide (SiC) [4], [5], or super-junction (SJ) structure [6]. This requirement is usually not met because

the channel of a silicon transistor is formed by an inversion layer, whereas a GaN device forms a two-dimensional electron gas (2DEG) through a heterojunction. A good approach to meet these requirements is presented by Endruschat et al [7].

This paper investigates the applicability of a silicon power MOSFET behavioral model for GaN transistors. The Infineon CoolGaN™ IGOT60R070D1 [8] is modeled using the procedure proposed in [9], which was originally developed for super-junction FETs. The model is then analyzed in a half-bridge topology by both simulation and measurement according to the CISPR 25 standard [10]. A 3D simulation is performed in CST Studio Suite [11], which includes the MOSFET model. Thus, the effects of the given PCB layout and two different DC voltages are also investigated.

The aim is to analyze which parameters of the model become critical at higher frequencies. We only use datasheet information and a single measurement. In this paper, we use a conducted emission measurement, alternatively, a double-pulse measurement does also work. We show that with the developed model, measured conducted emission data is well reproduced up to 300 MHz. In addition, a simplified universal power MOSFET model is proposed, including its limitations. In summary, this paper has the following novelties:

- A quick and easy way to create a universal power MOSFET model that is also valid for GaN transistors,
- Which (few) parameters are, in the given case, critical for accurate emission modeling up to 300 MHz.

We note that we refer to conducted emission modeling, even though this procedure is usually only performed up to 108 MHz. In our paper, we extend the frequency range of investigation up to 400 MHz for comparison with measurement.

2.3.3 Transistor Modeling

The power MOSFET model and the proposed simplified version are shown in Figure 3.1 and Figure 3.2, respectively. The complex version separates static and dynamic behavior. Especially the latter is of interest for high-frequency analysis.

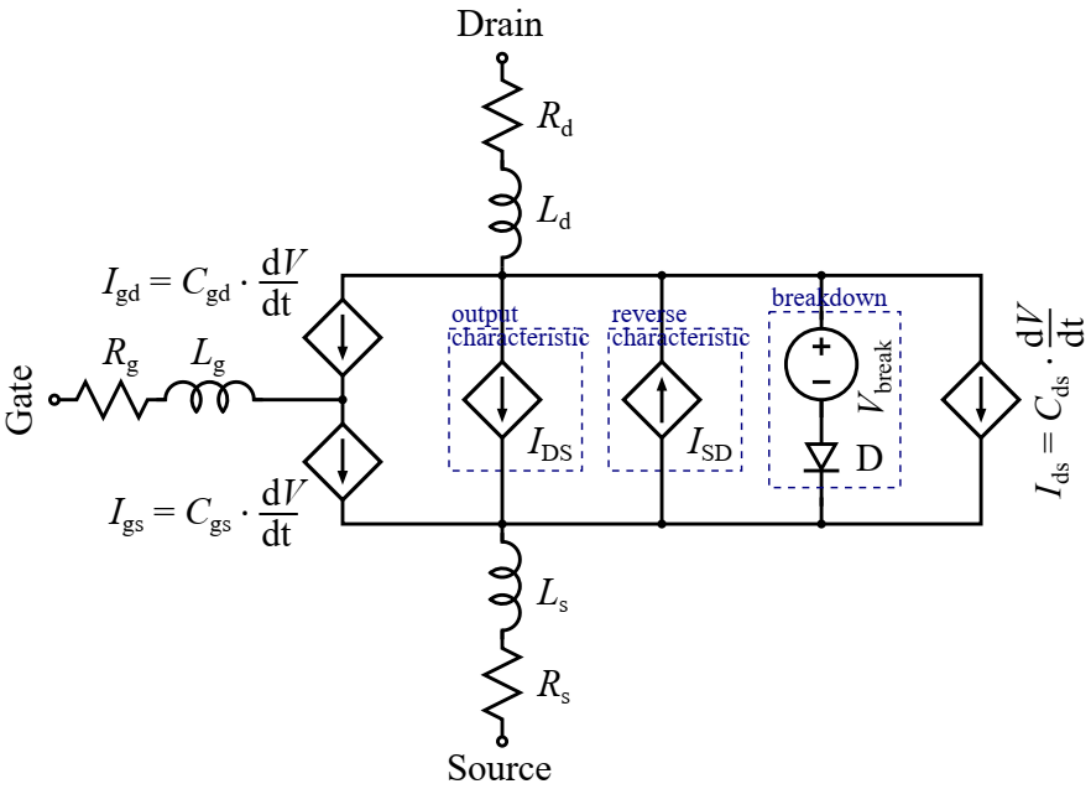


Fig. 3.1: Detailed equivalent circuit model of the power MOSFET used in this work, incorporating voltage-dependent capacitances (Cgs, Cgd, Cds), parasitic resistances (Rg, Rd, Rs), and inductances (Lg, Ld, Ls) to capture high-frequency switching behavior and conducted EMI up to 300 MHz.

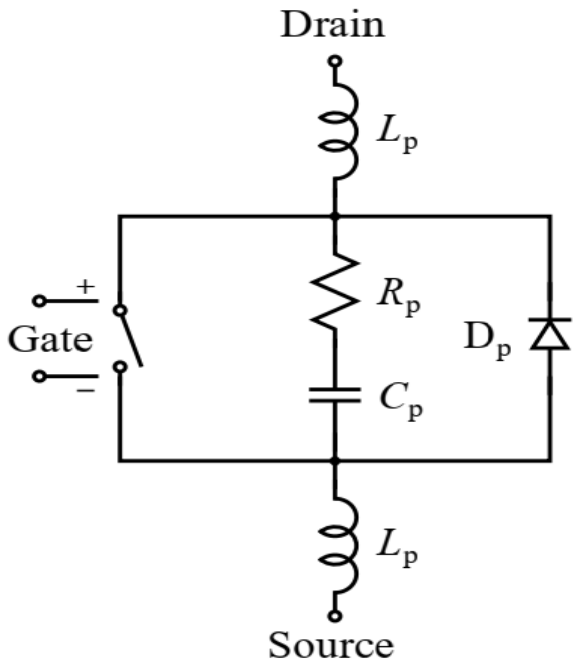


Fig. 3.2: Simplified behavioral MOSFET model derived from Fig. 3.1, retaining dominant parasitic elements (Rp, Lp, Cp) to reduce simulation complexity while preserving key resonance and damping effects relevant to EMI analysis.

2.3.3.1 DC Characteristics

The output characteristic of the MOSFET is modeled with a voltage-controlled current source (I_{DS}). Depending on whether the MOSFET is biased in the linear region or in the saturation region, the current can be calculated by Eq. 3.1 and Eq. 3.2 of Shichman and Hodges [12]:

$$I_{DS,lin} = \frac{\beta}{2}(2(V_{gs} - V_{to})V_{ds} - {V_{ds}}^2)(1 + \lambda V_{ds}) \quad (3.1)$$

$$I_{DS,sat} = \frac{\beta}{2}((V_{gs} - V_{to})^2(1 + \lambda V_{ds})) \quad (3.2)$$

The three unknown parameters are the threshold voltage V_{to}, a factor β which is a function of the internal semiconductor geometry and material, and the channel length modulation factor λ. For the investigated GaN transistor, λ has a small value. For simplicity, it is set to 0. The other two parameters can be extracted from the datasheet by taking the two points I_{ds1} and I_{ds2} at V_{gs1} and V_{gs2} from the transfer characteristic. The rearrangement of Eq. 2 gives β and V_{to} with Eq. 3.3 and Eq. 3.4, respectively:

$$\beta = 2I_{ds1}/(V_{gs1} - V_{to})^2 \quad (3.3)$$

$$V_{to} = V_{gs2} - V_{gs1}(\sqrt{I_{ds2}/I_{ds1}})/(1 - \sqrt{I_{ds2}/I_{ds1}}) \quad (3.4)$$

The reverse characteristic of the GaN transistor is modeled in a very similar way by taking two points from the datasheet again. The breakdown is modeled by an ideal diode which becomes conductive when the applied voltage exceeds V_{break}.

2.3.3.2 AC characteristics

The voltage-dependent capacitances between the drain, gate, and source are modeled as voltage-controlled current sources whose output currents follow the current–voltage relation $I = C \cdot dV/dt$. The capacitance values are stored in tables as voltage sources. Since datasheets give the values as input capacitance C_{iss}, output capacitance C_{oss}, and feedback capacitance C_{rss}, these must be converted according to Eq. 3.5–3.7:

$$C_{gd} = C_{rss} \quad (3.5)$$

$$C_{gs} = C_{iss} - C_{rss} \quad (3.6)$$

$$C_{ds} = C_{oss} - C_{rss} \quad (3.7)$$

A first-order estimate of the parasitic self-inductance of the bond wires is made using the formula for the inductance of a straight piece of round wire [13] as most datasheets do not provide this information. The same applies to R_d and R_s. These values can be initially estimated to be $R_{DS(on)}/2$, each.

2.3.3.3 Simplified model

The complex model depicted in Figure 3.1 is simplified in Figure 3.2 to investigate the impact of the gate terminal at high frequencies. R_p, L_p, and C_p in the simplified model correspond to R_d and R_s, L_d and L_s, and C_{ds}

in the complex model, respectively.

2.3.4 Device-under-Test

We investigate two 600+V CoolGaN™ IGOT60R070D1 from Infineon [8] mounted in a half-bridge topology on a printed circuit board as shown in Figure 3.3. The gate signal is generated by an external waveform generator and processed on the board by an auxiliary gate driver circuit (1EDF5673K). Two DC link capacitors of nominal 1.0 µF are connected between the DC+ and DC- nodes. The load is an RL series circuit connected between the switching node and DC+. It is composed of a power resistor with aluminum housing and a high-current power inductor with nominal values of 10 Ω and 10 µH and about 15 cm of wire at both ends. The fundamental switching frequency is 200 kHz, and the rise and fall times of the drain-source voltage are about 10 ns. Further hardware details are described in [1].

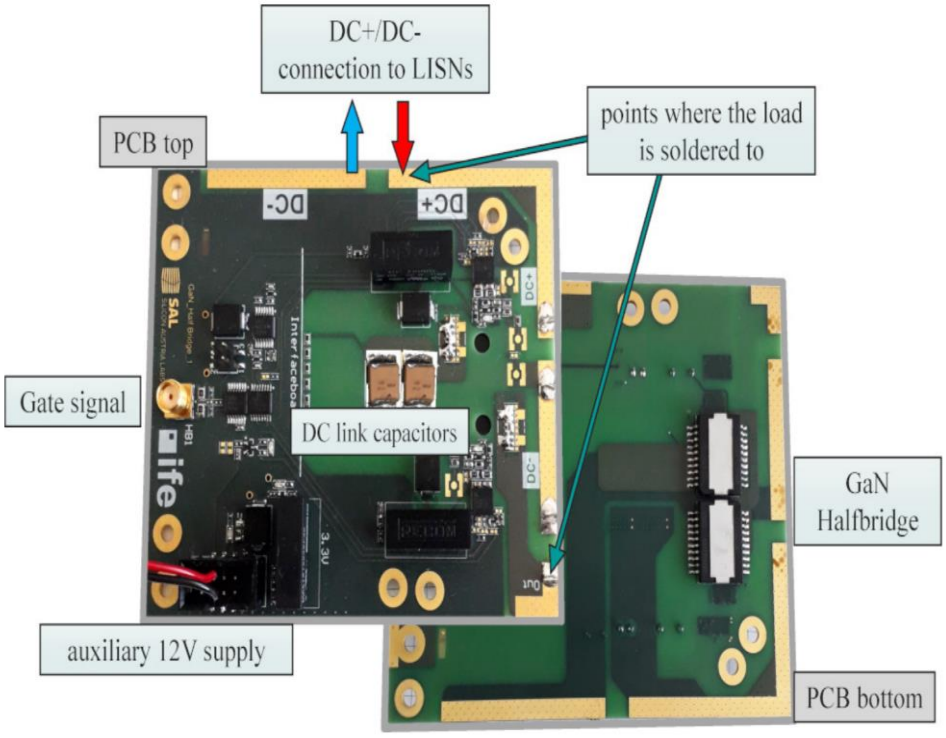


Fig. 3.3: The GaN half bridge board top and bottom side.

2.3.4.1 Conducted Emission Measurements

Conducted emission measurements according to the voltage method described in the CISPR 25 standard [10] were carried out. As can be seen in Figure 3.4, the board and the load are placed 50 mm above a full metal table, and two Line Impedance Stabilization Networks (LISNs) [14] are connected between the power supply and the DUT. At the positive LISN, an EMI receiver measures the EMI spectrum in the frequency range from 150 kHz to 400 MHz. It should be noted that there is an additional effect of LISNs above 150 MHz, which we have not investigated. Two operating points were measured, one with a DC supply voltage of V_{DC} = 10 V and one with V_{DC} = 60 V. Further details of the measurements are described in [1].

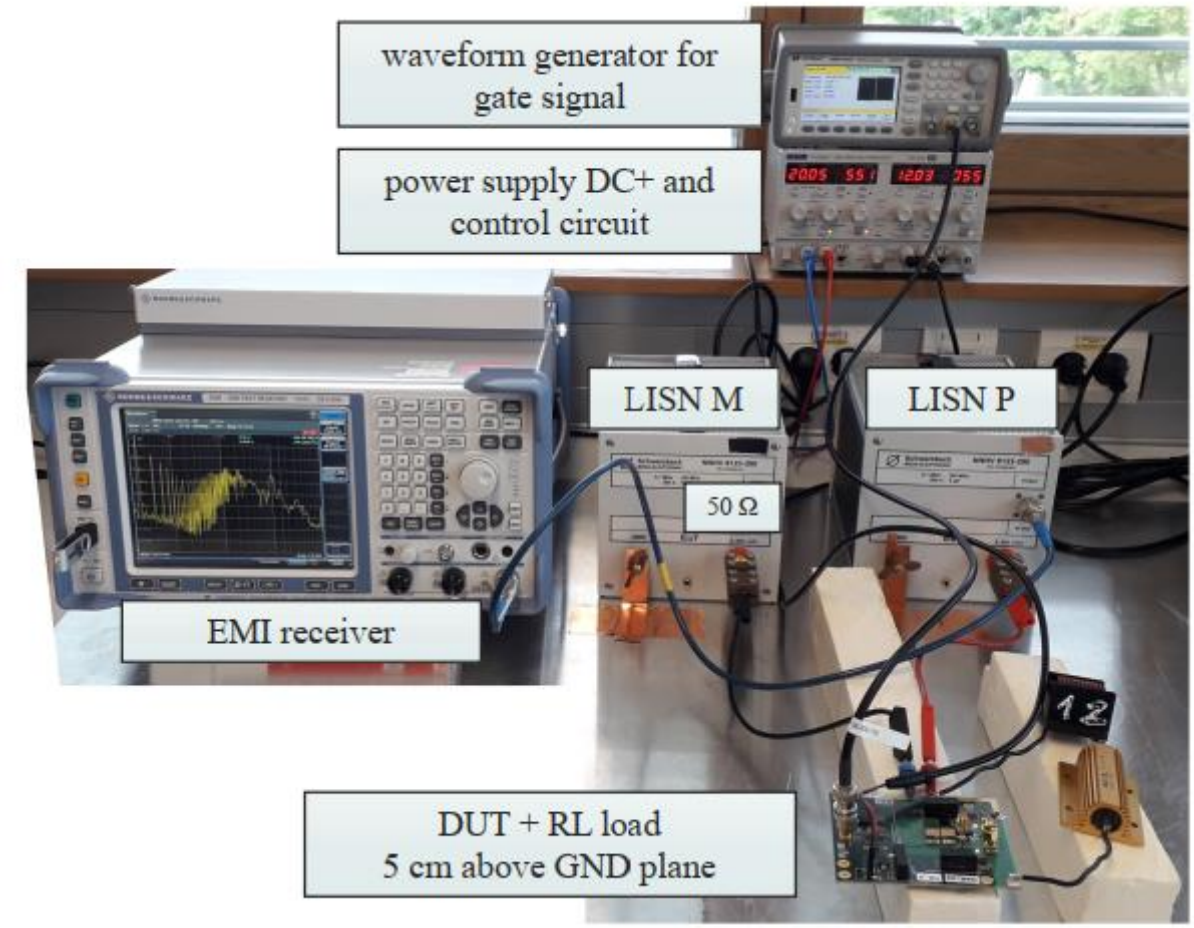


Fig. 3.4: Setup of the conducted emission measurement. Two LISNs are used, and the emission measurement used in this paper is recorded at LISN P at the positive supply terminal.

2.3.4.2 Simulation Model

Figure 3.5 shows the numerical 3D model of the DUT. It was developed in [1] and reused to test the accuracy of the novel GaN MOSFET model compared to the previously reported one. The 3D model considers a distance of 50 mm between the DUT and the ground reference table. Furthermore, the supply cables connecting the LISN networks and the load are also included in the model. The electromagnetic behavior of the PCB is numerically estimated using full-wave finite element method (FEM) simulations in CST Studio Suite [11] and a multi-port S-Parameter model is generated from the 3D simulation results [1]. Finally, this S-Parameter model is then deployed in a SPICE framework to connect equivalent circuit (EC) models of the GaN MOSFETs, capacitors (equivalent circuits with parasitic inductance taken from data sheet), load (network analyzer measurement for differential mode plus additional common mode capacitance obtained using an impedance analyzer), and LISN networks (circuit schematic). Figure 3.6 shows the top-level circuit schematic of the com- plete system. It comprises the novel EC model of the GaN MOSFETs detailed above (see Figs. 3.1 and 3.2) as well as the previously reported EC models of the load, LISNs, and DC link capacitors [1].

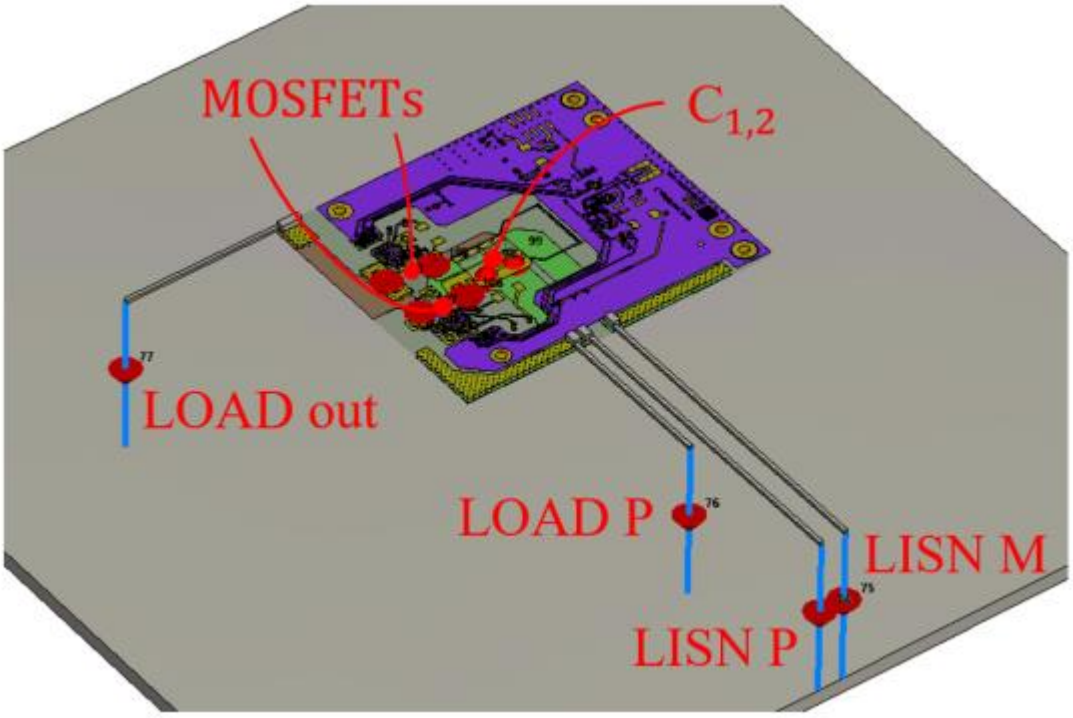


Fig. 3.5: Full-wave 3D electromagnetic model of the GaN half-bridge test setup used for conducted EMI simulation. The model includes the PCB layout, LISN connections, supply and load wiring, and a 50 mm spacing to the ground reference plane, enabling accurate extraction of the multi-port S-Parameter model of PCB shown in the center of Fig. 3.6.

.

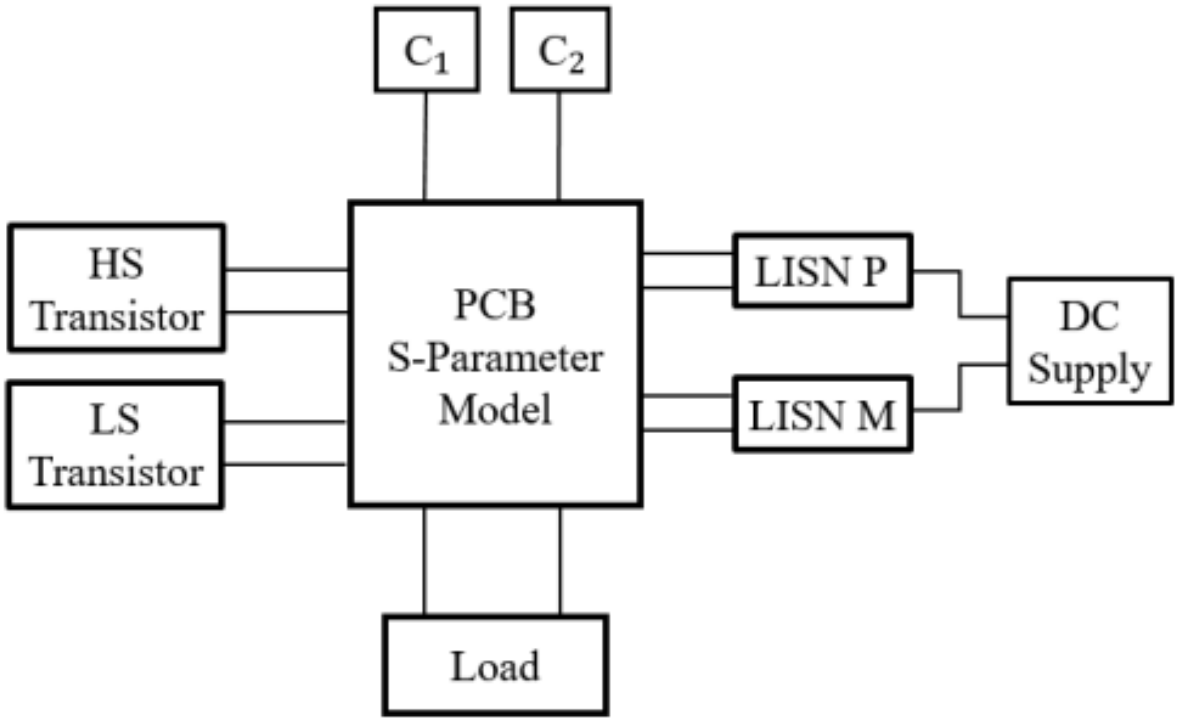


Fig. 3.6: Top-level circuit schematic for system simulations of the conducted emissions.

2.3.5 Model Analysis

In this section, firstly, the comparison between the simulation using a complex transistor model and the measurement using DC power supplies of 10 V and 60 V up to 400 MHz is shown. Then, the impact of individual parameters of the model used on the simulation result is studied to gain insight into its sensitivity. Both the parameters of the GaN model and the impact of the 3D geometry are investigated.

2.3.5.1 Comparison to Measurements

Fig. 3.7 and Fig. 3.8 show the comparison between measure- ment and simulation results using the complex model shown in Fig. 1 at VDC = 10 V and VDC = 60 V , respectively. To investigate the impact of the transistor model parameters, we use a manual fitting procedure. We start using the datasheet values and subsequently investigate the sensitivity of all parameters. It turns out that the following parameters are of relevance: λ, R_g, R_d, R_s, L_d, L_s, C_{gd} and C_{ds}. In the end, a very good match between simulation and measurement is obtained with the values found in Tab. I, which results in the frequency responses of Fig. 3.7 and Fig. 3.8.

The parasitic capacitance values are close to the datasheet values (±10% deviation). In the complex model, to obtain the desired overshoot attenuation between 70 MHz and 90 MHz, there is a trade-off between Rd and Rs, and λ. In this case, when λ=0, Rd and Rs tend to be larger than estimated from the datasheet (about 20 times larger). However, Rd and Rs can have values close to the datasheet if λ can have a larger value such as 0.5.

Note that alternatively, these parameters could be obtained by comparing measured and simulated waveforms of a double pulse setup. The parameters of the simple model are chosen according to [1].

From 70 to 90 MHz, the maximum difference between simulation and measurement is about 6 dB at V_{DC} = 10 V . In both figures, the difference between simulation and measure- ment, from 3 to 40 MHz, can be proven to be due to the load, as shown in [1]. In conclusion, the chosen model topology, originally devised for power MOSFETs characterizes the GaN very well for emission simulation up to 300 MHz. Above 300 MHz, the measurement appears to show a resonance, which is not predicted by the model.

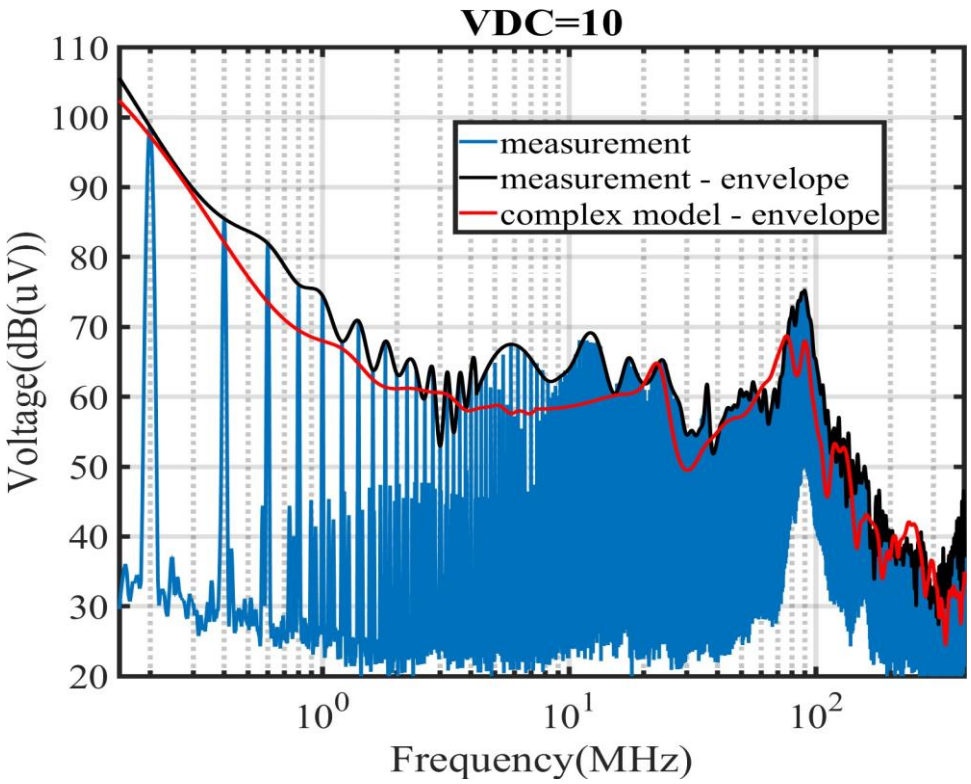


Fig. 3.7: Comparison between measured and simulated conducted emissions using complex model (VDC = 10 V).

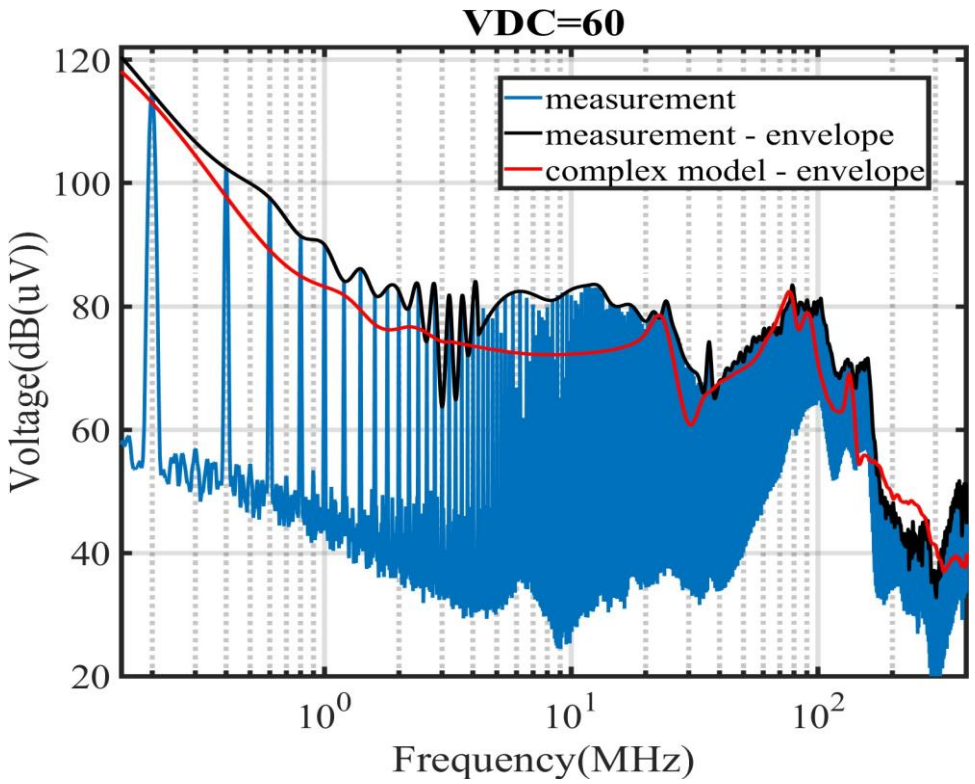


Fig. 3.8: Comparison between measured and simulated conducted emissions using complex model (VDC = 60 V).

2.3.5.2 Sensitivity Analysis of System Parameters

The simulation results of the complex and simple models are compared with and without the effect of PCB layout at VDC = 10 V (Fig. 3.9). It is clear that ignoring the effect of the PCB layout results in the disappearance of the overshoot between 70 MHz and 90 MHz, which is demonstrated by both models. Using the simple model without layout, the overshoot frequency is visible at a much higher frequency, because the parasitic inductance of the layout is missing. The simple and the complex transistor models differ in the peak amplitude at the resonance. Compared to the measurement, the amplitude of the complex model is about 5 dB too low (cf. Fig. 3.9), and that of the simple model is 5 dB too high.

Fig. 3.10 compares the simulation results with the complex and simple models for V_{DC} = 10 V and V_{DC} = 60 V. Below 80 MHz, the frequency response at 10 V is shifted up by about 15 dB at 60 V as shown by both models which equals 20 $\log_{10}(6)$, i.e. it is proportional to the increase in DC voltage. Above 80 MHz the simple model shows almost the same overshoot between 70 MHz and 90 MHz at both voltages, which is wrong for the frequency response at 10 V. At 60 V, above 150 MHz, the frequency response should drop sharply, but, this is not possible with the simple model. The parameters R_g and C_{gd} of the complex model produce this behavior very well. At 60 V, the first resonance (region A) is well described by both the simple and the complex transistor models, but the second (region B) is only correctly described by the complex model.

The impact of individual parameters of the complex model on the simulation result has been investigated in further simulations and is as follows:

- C_{gd} and C_{ds} define the frequency of the overshoot between 70 MHz and 100 MHz.
- C_{gs} has in our experimental setup (the load is attached to the drain-side) minor impact on the frequency response.
- Damping can be tuned to a high extent by R_g, R_d and R_s.
- The falling slope at higher frequencies could be tuned to a higher extent by R_g and C_{gd} and to a lower extent by L_d and L_s
- The effect of L_g is negligible.

The high-frequency performance of the complex model can be divided into regions A, B, and C as it is shown in Fig. 3.10. The third column of Table 3.1 shows which region is dominated by which parameter. The dots ... indicate that the parameter has no effect.

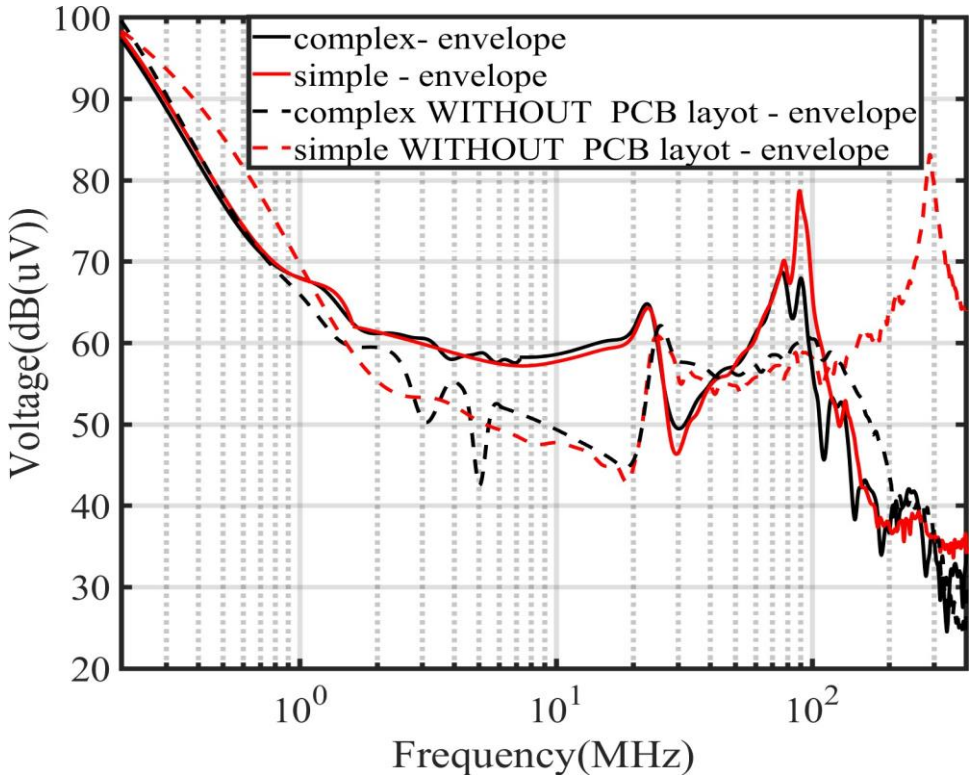


Fig. 3.9: Simulated conducted emissions: comparison between complex and simple (Rcs=0) models with and without the effect of PCB layout (VDC = 10 V).

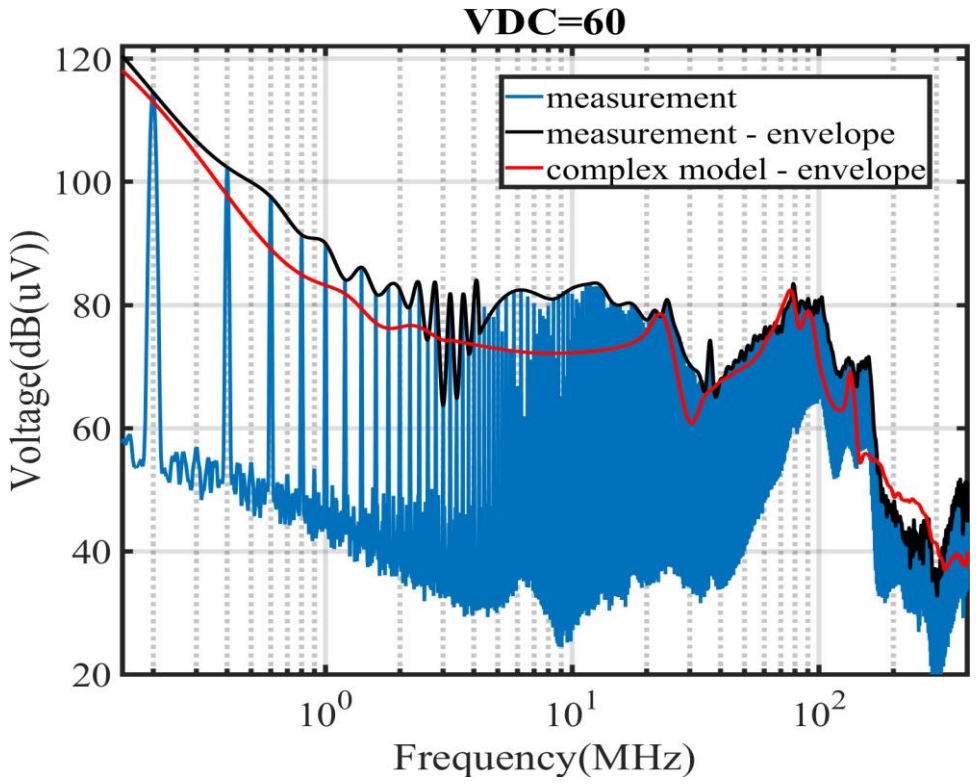


Fig. 3.10: Simulated conducted emissions: comparison between complex and simple models at $V_{DC} = 10\ V$ and $V_{DC} = 60\ V$.

Table 3.1: Chosen values of the parameters of the complex model for the simulation.

Parameter	value	Region of impact
λ	0	…
R_d	0.7 Ohm	A
R_S	0.7 Ohm	A
Rg	1 Ohm	A, B and C
L_d	3.3 nH	C
Ls	1.2 nH	C
Lg	5 nH	…
C_{ds}(10 V)	120 pF	A
C_{ds}(60 V)	148 pF	A
Cgs(10 V)	363 pF	…
Cgs(60 V)	400 pF	…
C_{gd}(10 V)	60 pF	A, B
C_{gd}(60 V)	6 pF	A, B

2.3.6 Conclusion

In this paper, a silicon power MOSFET behavioral model is adapted to GaN transistors to characterize conducted emission. The model is analyzed in a half-bridge topology using both 3D simulations of the test setup and measurements. Using datasheet information and a single measurement, our approach indicates that GaN modeling up to 300 MHz is possible by considering only a few parameters of a very general transistor model. We also present a simple model which shows good results at a low supply voltage of 10 V and up to the resonance frequency generated by the layout inductance and the transistor capacitances.

2.3.7 My Scientific Contribution

This paper evaluates the applicability of a behavioral model—originally developed for silicon power MOSFETs—to GaN transistors, with a focus on identifying key parameters influencing high-frequency emission modeling. It further investigates the impact of PCB layout through 3D electromagnetic simulations, examines the effect of different DC voltage levels, and compares simulation results with experimental measurements.

My specific contributions to this work include:

- Developing of a GaN transistor model for transient co-simulation in CST Studio Suite
- Performing 3D full-wave electromagnetic simulations
- Conducting high-frequency emission measurements
- Designing and executing a sensitivity analysis to assess the influence of model parameters and PCB layout effects
- Analyzing and interpreting the resulting data

2.4 Modeling and Experimental Characterization of R_{OSS} for EMI Prediction in GaN-based Power Converters

M. Gholizadeh and D. Pommerenke, "Modeling and experimental characterization of R_{OSS} for EMI prediction in GaN-based power converters," *submitted to IEEE Trans. Power Electron.*, Apr. 30, 2025; reviews received Jul. 21, 2025; revision currently in preparation.

2.4.1 Abstract

This paper presents a detailed investigation into the impact of the resistive component of the output capacitance—denoted as ROSS—on the electromagnetic compatibility (EMC) performance of GaN-based power converters. It shows that this loss can dominate the resonance often seen in the electromagnetic interference (EMI) measurements. A behavioral compact model of a GaN high-electron-mobility transistor (HEMT) is developed and implemented in LTspice, incorporating nonlinear capacitances, dynamic on-state resistance, and a voltage-dependent ROSS. The ROSS parameter, which is not provided in standard datasheets, is experimentally extracted through S-parameter measurements up to several hundred megahertz using a calibrated transmission line setup. The model is validated across three different GaN devices through both time-domain and frequency-domain measurements using a half-bridge test platform. Results confirm that ROSS significantly affects switching waveform damping and EMI emissions, particularly in the 30–150 MHz range. Devices with higher ROSS show reduced overshoot and improved damping, translating to up to 15 dB lower conducted EMI. Simulation results that incorporate ROSS show excellent agreement with measurements, highlighting the importance of including this loss mechanism for accurate modeling and EMI prediction. These findings offer new insight into GaN device selection and circuit design for EMC-critical applications.

2.4.2 Introduction

Gallium Nitride (GaN) high-electron-mobility transistors (HEMTs) are emerging as a superior alternative to traditional silicon (Si) power devices due to their lower on-resistance, reduced parasitic capacitance, and negligible reverse recovery charge. These characteristics enable faster switching speeds and higher power densities, making GaN an ideal candidate for compact and efficient power conversion in modern applications such as electric vehicles [15]. However, fully realizing the benefits of GaN devices requires a deeper understanding of their dynamic behavior, especially under high-frequency switching conditions. In addition to known challenges such as dynamic on-resistance degradation and breakdown limitations [16], [17], a key concern in MHz-range soft-switching applications is the energy loss associated with the output capacitance, COSS, of the device [18]. This loss becomes particularly significant at high switching frequencies, where it can dominate total switching losses and drastically reduce system efficiency.

Output capacitance loss can be divided into two components: capacitive loss, attributed to charge

hysteresis effects that grow prominent above 20 MHz, and resistive loss, commonly referred to as ROSS. Ideally, charging and discharging COSS would be lossless; however, empirical studies have shown that GaN HEMTs may lose up to 20% of their stored energy (EOSS) during each switching event [18]–[24]. This loss mechanism is not reflected in device datasheets but has a measurable impact on converter performance, particularly at high frequencies [24].

Prior work typically evaluates COSS losses in terms of energy dissipation per cycle (EDISS), often treating the device as a passive capacitor in the OFF-state [18]–[27]. These studies, however, either overlook the contribution of ON-state behavior or focus only on single-pulse characterization, failing to capture steady-state operating conditions. Recent methods, such as those proposed in [25], begin to address this gap by incorporating resonance-based testing under controlled conditions, yet the specific role and modeling of ROSS remains underdeveloped.

From an electromagnetic compatibility (EMC) perspective, the resistive component of COSS. or ROSS, plays a critical role in shaping the switching waveform, particularly the damping of oscillations caused by parasitic inductance and capacitance in the power loop. Recent work by Kam et al. [28] presented a practical method for quantifying Ross in low-voltage power MOSFETs (below 100 V), highlighting its significant influence on high-frequency ringing in synchronous buck converters. Their results demonstrated that variations in Ross among low-side FETs can markedly affect the waveform characteristics and, by extension, the overall radiated electromagnetic interference (EMI) performance.

In half-bridge topologies—commonly used in DC-DC converters and battery chargers—the ringing observed during switching transitions can introduce substantial conducted and radiated EMI [29], [30]. Fig. 3.11 shows a simplified schematic of the half-bridge test circuit used in this study. The corresponding switching waveform, captured in Fig. 3.12, highlights the high-frequency ringing observed during the falling-edge transition. This waveform clearly exhibits a transient overshoot followed by exponentially decaying oscillations. These oscillations are typically characterized by several parameters [28],[31]:

- Rise time: Governed by transistor switching speed and gate driver capability.
- Overshoot: Affected by the resonant interaction between parasitic inductance and COSS, and influenced by reverse conduction in the high-side switch (FET1).
- Oscillation frequency: Determined by the LC resonance of the switching loop, particularly the high-side device's output capacitance and the loop inductance.
- Decay rate: Defined by total losses in the loop, including contributions from ROSS, R_(ds,on) , and equivalent series resistance (ESR) of decoupling capacitors. (e.g., 12 mΩ).

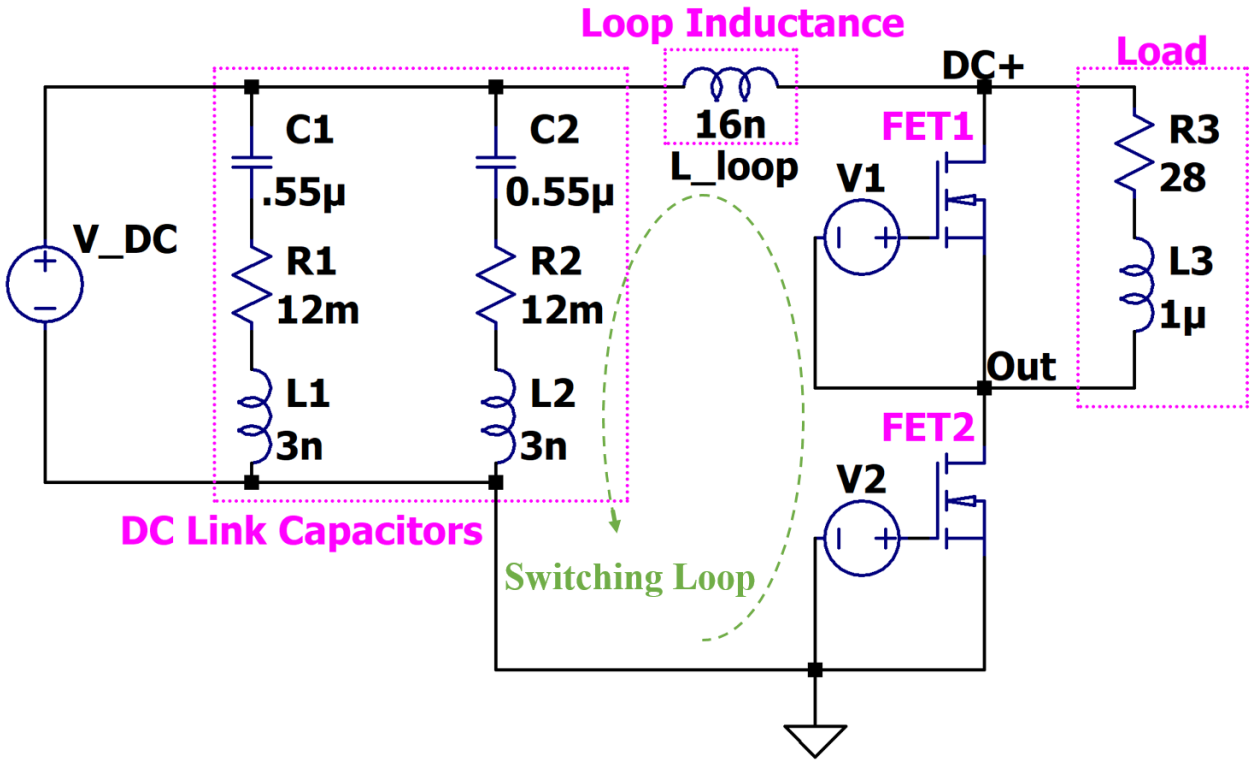


Fig. 3.11. Simplified half-bridge test circuit used for switching and EMI measurements.

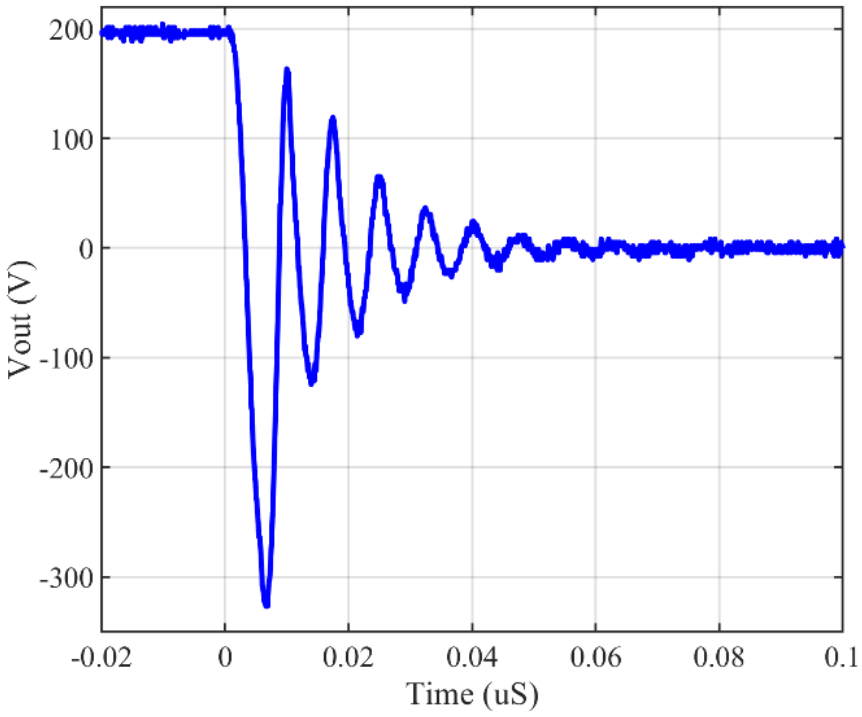


Fig. 3.12: Measured phase-node waveform at $V_{dc} = 200\,V$ using an IGOT60R070D GaN device showing high-frequency ringing.

Switching losses in these converters can be broadly categorized into conduction and switching losses (Fig. 3.13). While previous work has extensively examined dynamic R_(ds,on) [32]-[39], its effect on conduction losses, and the behavior of COSS, there is currently no established model or measurement technique to accurately quantify ROSS or integrate it into simulation frameworks [7], [39]–[41]. This omission leads to a disconnect between theoretical loss modeling and actual circuit behavior—especially in EMI prediction and time-domain waveform analysis.

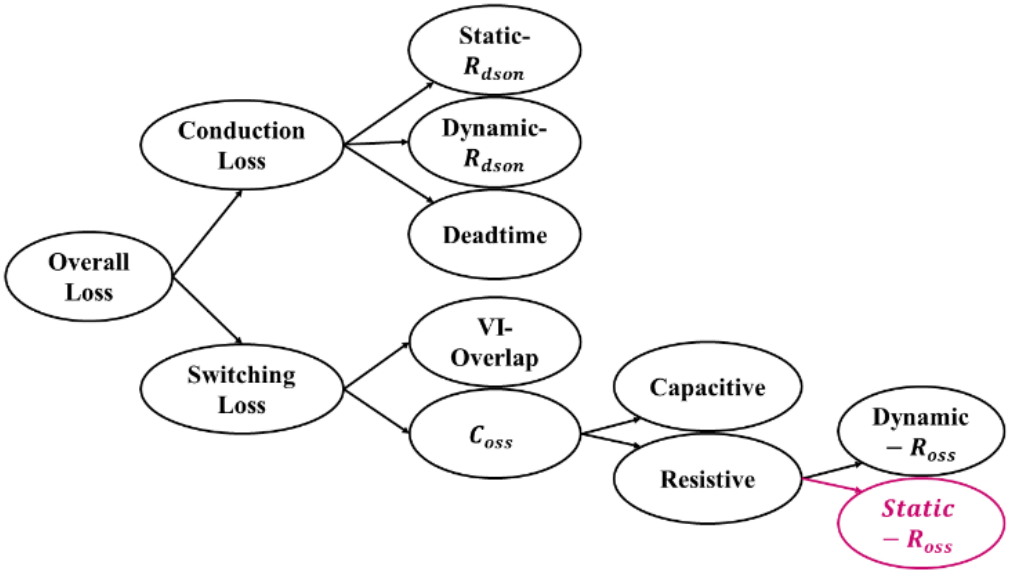


Fig. 3.13: Classification of switching and conduction losses in GaN-based half-bridge converters.

This paper addresses this critical gap by focusing on the measurement, modeling, and impact of static ROSS in GaN HEMTs. The main contributions of this work are as follows:

- A practical, high-precision measurement technique is proposed to extract R_{OSS} using S-parameter analysis up to several hundred megahertz.
- A compact GaN model is developed in LTspice, incorporating a voltage-dependent R_{OSS} extracted from experimental data.
- The influence of R_{OSS} on switching waveform damping and conducted EMI is analyzed across different GaN devices and operating voltages.
- Time-domain and frequency-domain simulations are validated against measurements, showing that including R_{OSS} leads to significantly improved correlation with experimental results—up to 14 dB difference in EMI prediction when ignored.

These findings underscore the need to consider R_{OSS} as a key parameter in both modeling and device selection for high-frequency GaN power converter applications, especially where EMC compliance is a concern.

2.4.3 GaN Device Modeling and Loss Mechanism Analysis

2.4.3.1 Compact Model of GaN Transistor in LTspice

To accurately represent power losses in GaN HEMTs, the model illustrated in Fig. 3.14 is proposed. The forward conduction behavior is captured using a voltage-controlled current source (IDS), whose value is determined based on the device's operation in either the linear or saturation region. The Shichman-Hodges model, with channel length modulation (λ) set to zero, is used to calculate IDS as follows:

$$I_{DS,lin} = \frac{\beta}{2}(2(V_{gs} - V_{to})V_{ds} - {V_{ds}}^2) \qquad (3.8)$$

$$I_{DS,sat} = \frac{\beta}{2}(V_{gs} - V_{to})^2 \qquad (3.9)$$

The parameters β and V_to are extracted from the device datasheet using two points on the transfer characteristic curve [28], according to the following equations:

$$\beta = 2I_{ds1}/(V_{gs1} - V_{to})^2 \qquad (3.10)$$

$$V_{to} = (V_{gs2} - V_{gs1}\sqrt{I_{ds2}/I_{ds1}})/(1 - \sqrt{I_{ds2}/I_{ds1}}) \qquad (3.11)$$

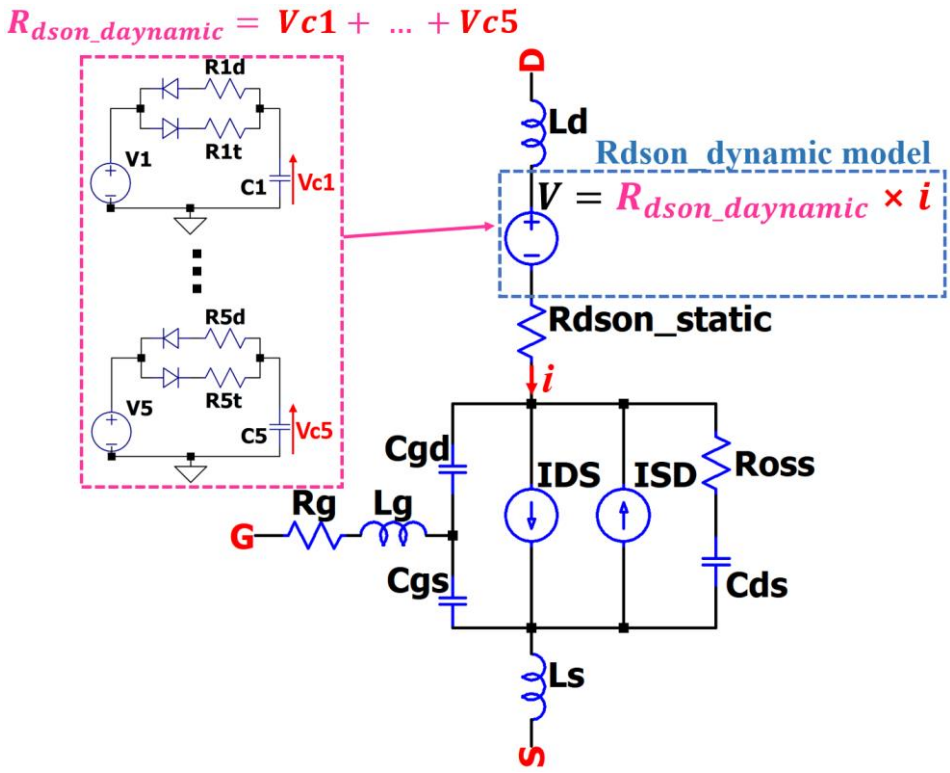


Fig. 3.14: LTspice implementation of the proposed compact GaN HEMT model.

Since GaN HEMTs are lateral devices and lack a body diode, reverse conduction occurs through the channel and is controlled by V_gd instead of V_gs [42]. The reverse conduction behavior, similar to forward conduction, is modeled using a voltage-controlled current source (ISD), with Eqs. (3.8) and (3.9) applied as functions of V_gd [7].

To model voltage-dependent parasitic capacitances in LTspice, the charge-based method is used, as illustrated in Fig. 3.15:

$$Q = f(x) = \int C(x)dx \qquad (3.12)$$

Here, x represents the voltage across the capacitor, and $C(x)$ is the voltage-dependent capacitance. Hence, $C_{ds}(V_{ds})$ and $C_{gd}(V_{gd})$ are derived through curve fitting based on datasheet values. Since datasheets typically provide input capacitance $C_{iss}(V_{ds})$, output capacitance $C_{oss}(V_{ds})$, and reverse transfer capacitance $C_{rss}(V_{ds})$, the relationships are defined as:

$$C_{gd}(V_{gd}) \approx C_{gd}(V_{ds}) = C_{rss}(V_{ds}) \qquad (3.13)$$

$$C_{ds}(V_{ds}) = C_{oss}(V_{ds}) - C_{rss}(V_{ds}) \qquad (3.14)$$

The gate-to-source capacitance, $C_{gs}(V_{gs})$, is extracted from the gate charge (Q_g) curve in the datasheet[7]. Parasitic inductances, which are typically not included in datasheets, are estimated using the formula for a straight wire [43]. Other static parameters, such as $R_{ds,on}$ and gate resistance R_g, are directly obtained from datasheet specifications [40].

Dynamic $R_{ds,on}$ effects, which result from charge trapping in the buffer layer during OFF-state stress, are also incorporated. This phenomenon leads to a temporary increase in resistance that recovers when the device returns to the ON-state. The behavior, influenced by both OFF- and ON-state durations, is modeled using RC networks, as described in [39]:

$$R_{dson}(t) = \sum_{i=1}^{n}(R_i - R_0)(1 - e^{-\frac{t_{off}}{\tau_{off_i}}})e^{-\frac{t_{on}}{\tau_{on_i}}} \qquad (3.15)$$

This time-dependent resistance is implemented in LTspice using a voltage-controlled behavioral source, as shown in Fig. 3.14. Additionally, the resistive loss associated with output capacitance, denoted R_{OSS}, is modeled as a series resistor with C_{ds}. Since R_{OSS} is not specified in datasheets and varies with V_{ds}, it is experimentally measured and modeled using a voltage-dependent resistor. A lookup table based on the measured data is implemented in LTspice, as demonstrated in Fig. 3.15.

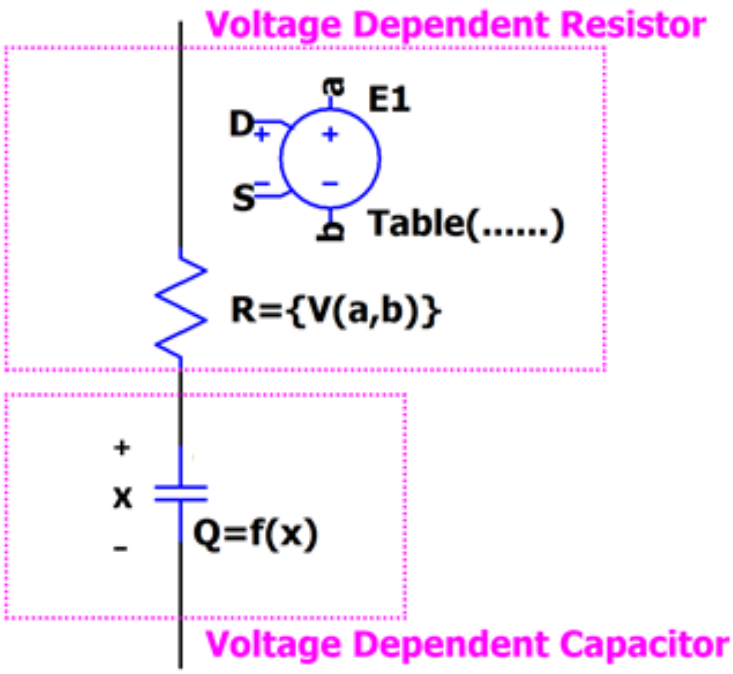


Fig. 3.15: Modeling of voltage-dependent parasitic capacitance and ROSS in LTspice.

2.4.3.2 Assessment of Individual Loss Components

Power losses in the transistors of a half-bridge circuit (Fig. 3.11) are critical in determining the overall performance and efficiency of power converters. This section evaluates the individual contributions of key loss components within such circuits using LTspice simulation. When the switching loop is modeled as a simplified series RLC network, the equivalent series resistance—denoted as R_loss, —governs the damping behavior of the waveform and is mathematically related to the exponential decay rate α by:

$$\alpha = R_{loss}/2L_{loop} \qquad (3.16)$$

LTspice simulations were performed for the circuit shown in Fig. 3.11 using the Infineon CoolGaN™ IGOT60R070D1 [44]. The transistor was modeled according to the representations in Fig. 3.14 and Fig. 3.15. All model parameters, except for ROSS and the dynamic R_(ds,on) , were extracted from the device datasheet. For the dynamic R_(ds,on), the measured parameters reported in [39] were adopted, while a constant ROSS=0.95 Ω at 60 V—measured and discussed in the following section—was assumed. Simulations were carried out with a DC bus voltage of V_dc= 60 V and a switching frequency of 200 kHz. The resulting switching waveform for the falling-edge transition is shown in Fig. 3.16. In the baseline scenario (blue curve), only the equivalent series resistance (ESR) of the input decoupling capacitors (2 × 12 mΩ) is included. Loss components are then introduced sequentially: first, the static R_(ds,on) (70 mΩ) in red, followed by the dynamic R_(ds,on) in green, and finally ROSS in purple. In each step, the total effective series resistance, denoted as R_loss, is computed based on the values summarized in Table 3.2. The results clearly demonstrate that ROSS is the dominant contributor to switching loss. Its inclusion increases R_loss significantly—from

270 mΩ to 1047 mΩ—and substantially damps the oscillations, as shown by the purple curve in Fig. 3.16. In comparison, the static R_(ds,on) is the second most impactful component, though its effect is considerably smaller than that of ROSS. Notably, the dynamic R_(ds,on) , despite being frequently emphasized in the literature, has a negligible effect on damping—adding only 27 mΩ to R_loss, as illustrated by the green curve. These findings highlight that, in GaN-based switching devices, accurate modeling and characterization of ROSS is far more critical than that of the dynamic R_(ds,on), especially in applications where ROSS significantly exceeds the static channel resistance. This insight is particularly relevant for EMC modeling and loss prediction in high-speed GaN power converter designs.

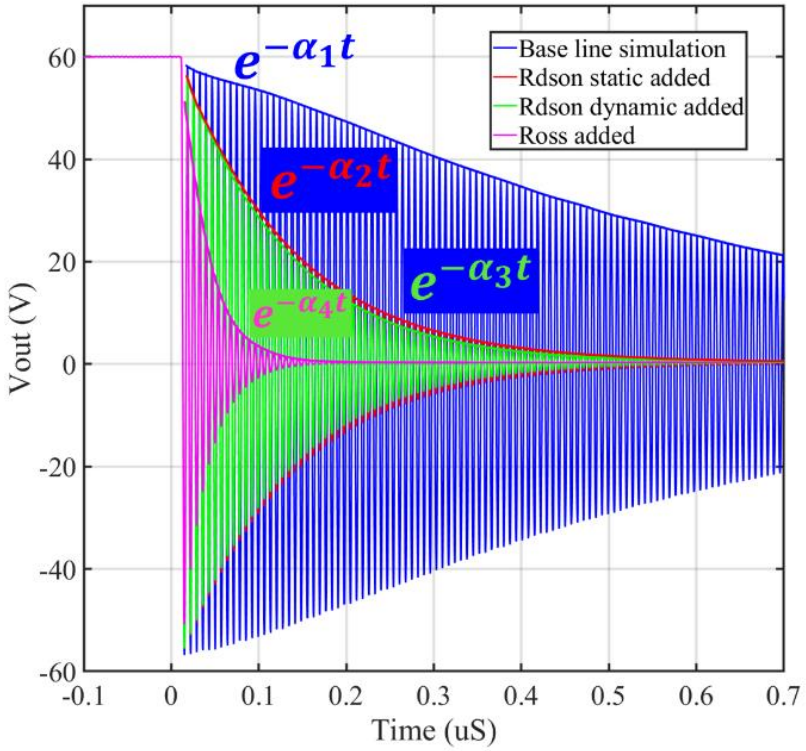


Fig. 3.16: Simulated switching waveforms showing the impact of individual loss components on damping.

Table 3.2: Contribution of Individual Loss Components to Effective Series Resistance.

Loss component added	α (1/uS)	R_{loss} (mΩ)
ESR of DC-link capacitors (Baseline simulation)	1.4	45
R_{dson_static}	7.6	243
$R_{dson\_daynamic}$	8.5	270
R_{oss}	32.7	1047

2.4.4 Experimental Characterization of *R*oss

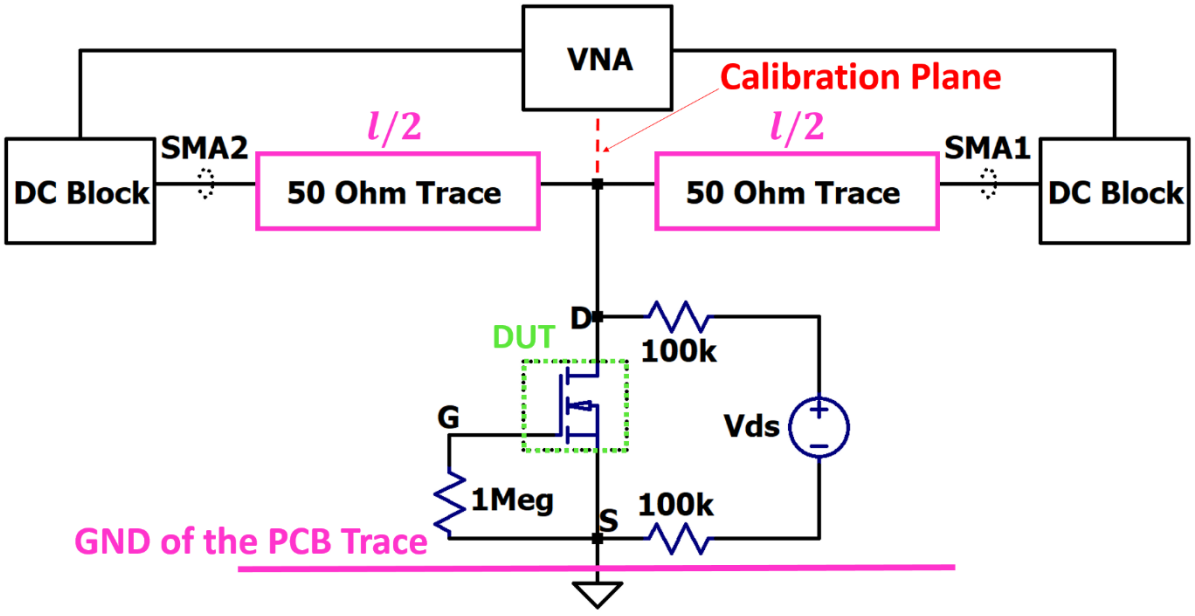
2.4.4.1 Measurement Setup and Methodology

To accurately assess the contribution of R_{OSS} to total system losses, high-frequency characterization—extending into the hundreds of megahertz—is required. This is achieved using a simple transmission line setup [28], where the GaN device's drain and source terminals are connected to the center of a microstrip trace and ground, respectively. To ensure minimal signal loss and high measurement accuracy, a low-loss PTFE substrate ($tan\,\delta = 0.0002$) is employed. The gate is biased to ground through a 100 kΩ resistor to keep the device in the OFF state during measurement. S-parameters are measured using a vector network analyzer (VNA), with port extensions applied to align the calibration plane precisely at the device location (Fig. 3.17(a)). In this OFF-state configuration, the measured S-parameters reflect the impedance of the output capacitance C_{OSS}, series resistance R_{OSS}, and equivalent series inductance (ESL), as illustrated in Fig. 3.17(b). The impedance Z can be calculated using the following expressions:

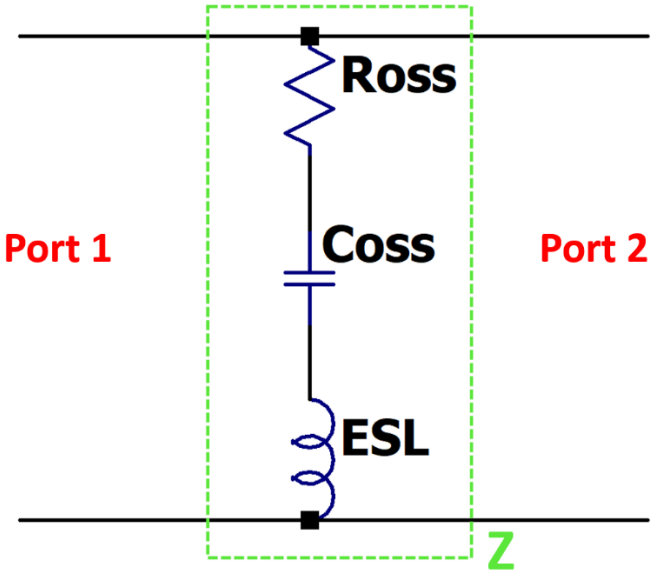
$$Z = \frac{Z_0 \times S_{21}}{2(1-S_{21})} = \frac{Z_0 \times (1+S_{11})}{-2S_{11}} \qquad (3.17)$$

Where $Z_0 = 50\ \Omega$ is the characteristic impedance of the trace. Once Z is determined, the resistive component representing R_{OSS} is extracted as:

$$R_{oss} = Real\{Z\} \qquad (3.18)$$



(a)



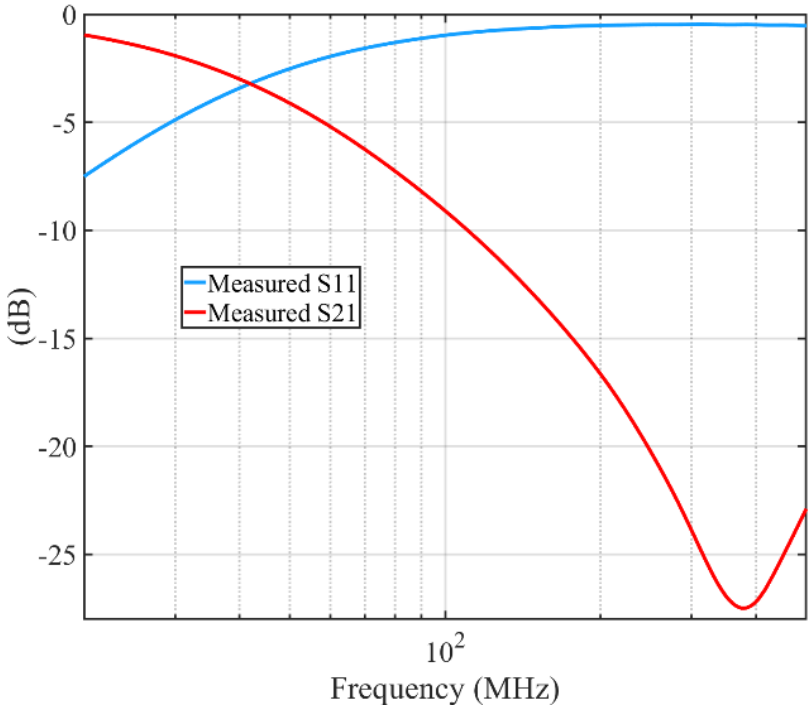
(b)

Fig. 3.17: (a) Transmission line measurement setup. (b) Equivalent circuit used for R_{OSS} extraction.

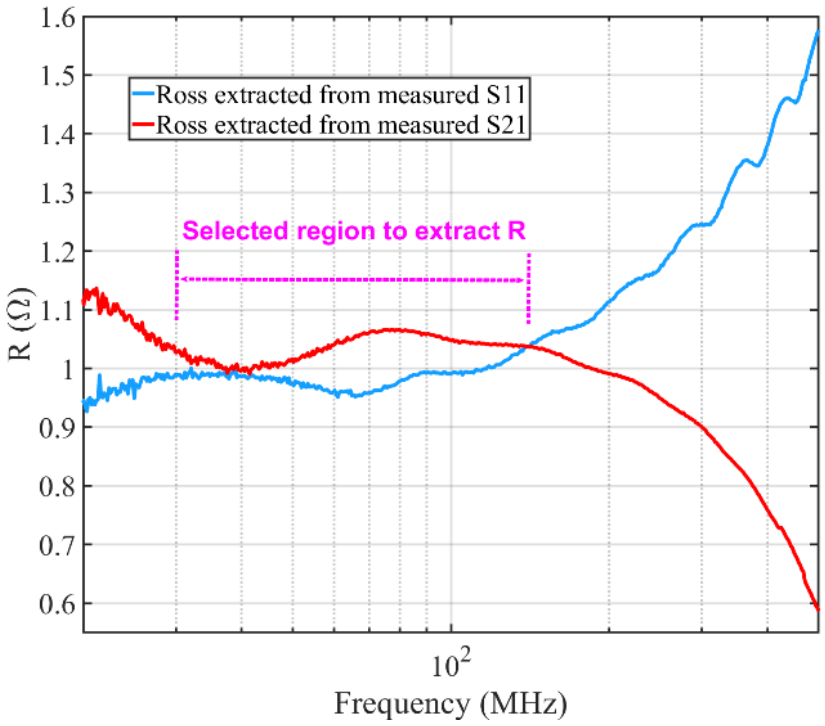
2.4.4.2 Validation Using Known Passive Components

To validate this measurement procedure, a 150 pF high- quality (Q) SMD capacitor in series with a 1 Ω SMD resistor was measured. The results, presented in Fig. 3.18, show that the extracted resistance in the frequency range of 30–150 MHz closely matches the nominal value, yielding 1 Ω with an accuracy of ±5%. This confirms the reliability of the measurement setup and methodology. Above 200 MHz, the extracted resistance shows noticeable deviation from the nominal value. This behavior can be attributed to the increasing influence of parasitic inductances associated with the surface-mount

components, minor de-embedding inaccuracies, dielectric losses of the capacitor at high frequencies, and the inherent dynamic range limitations of the VNA.



(a)



(b)

Fig. 3.18: Validation of the R_{OSS} extraction method. (a) Measured S-parameters. (b) Extracted resistance vs. frequency.

2.4.4.3 Measured Ross Across GaN Devicess

Another Table 3.3 summarizes the three types of devices under test (DUTs) used in this study, all of which are commercially available GaN HEMTs featuring different underlying technologies. R_{OSS} for each device was measured across a range of V_{dc} values. For instance, Fig. 3.19 presents the measured R_{OSS} of the IGOT60R070D device at $V_{dc} = 100\,V$, revealing a resistance value of approximately 1.2 Ω. Fig. 3.20(a) compares the R_{OSS} values of the three devices across different V_{dc} levels. As shown, R_{OSS} increases considerably with voltage for all three devices. The IGOT60R070D consistently exhibits a significantly higher R_{OSS} than the other two devices. This clearly demonstrates that R_{OSS} varies notably between manufacturers and device types, even when C_{OSS} and $R_{ds,on}$ are comparable. Finally, Fig. 3.20(b) shows the calculated Q-factors for the three devices, derived from the measured R_{OSS} values and the corresponding C_{OSS} values provided in their datasheets. As expected, the IGOT60R070D exhibits the lowest Q factor, while the TP65H150G4LSG has the highest. This indicates that the IGOT60R070D, when used as the high-side FET in the test configuration shown in Fig. 3.11, enables substantially greater damping compared to the other two devices.

Table 3.3: Key Parameters of Tested GaN Devices.

Technology	Part Number	V_{ds} (V)	I_{ds}(A)	$R_{ds,on}$ (mΩ)	C_{oss} at 400 V (pF)
P-GATE	GS66508T	650	30	50	65
HD-GIT	IGOT60R070D	600	31	70	72
GEN IV	TP65H150G4LSG	650	16	150	30

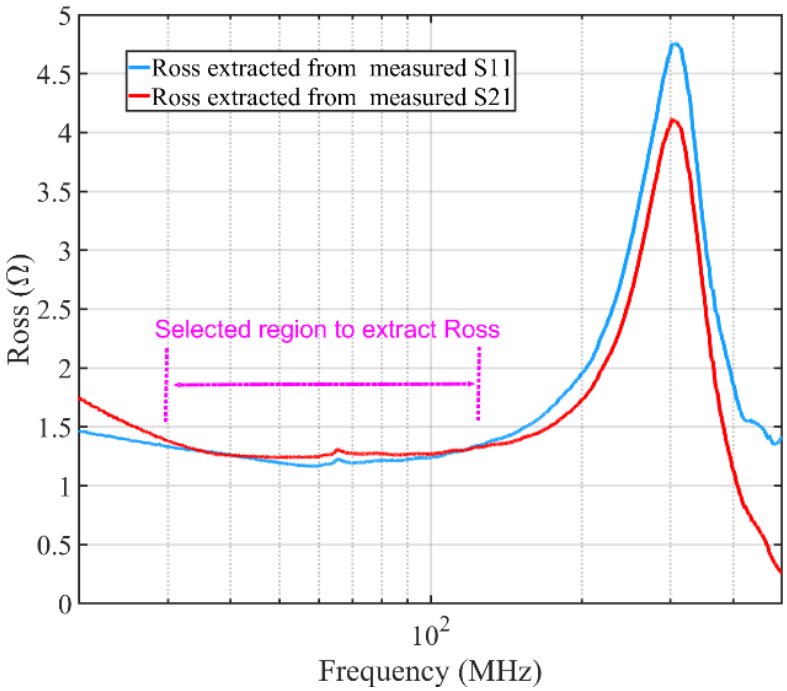
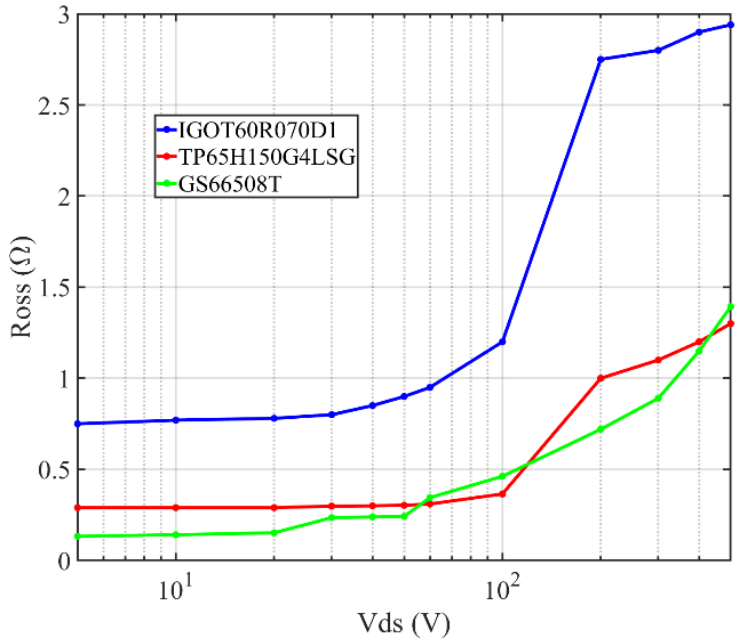
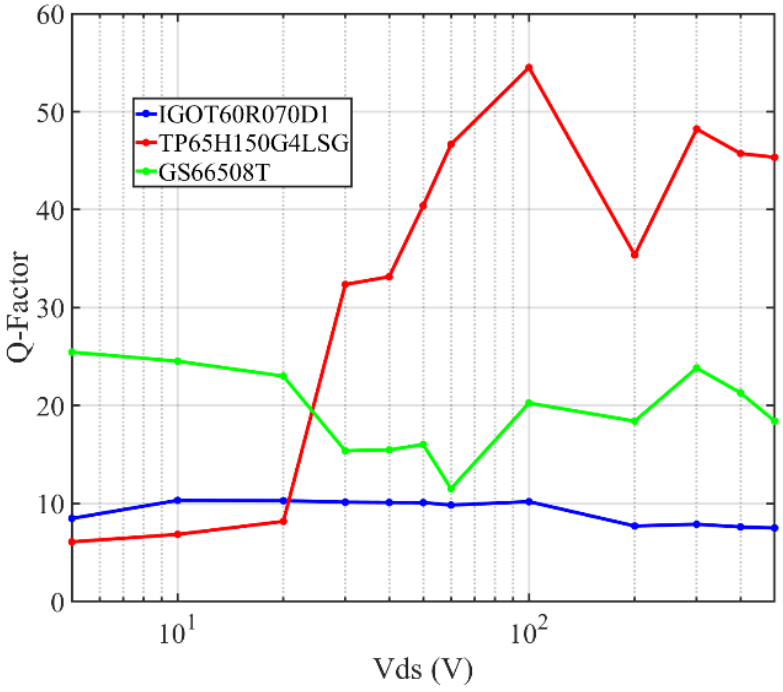


Fig. 3.19: Extracted R_{OSS} vs. frequency for IGOT60R070D at 100 V.



(a)



(b)

Fig. 3.20: (a) Measured R_{OSS} across three GaN devices. (b) Corresponding calculated Q-factors.

2.4.5 Impact of R_{OSS} on Switching Behavior

2.4.5.1 Switching Ringing Across Devices and Voltages

To illustrate the impact of high-side FET selection on switching behavior in the half-bridge circuit, measurements were taken using the test setup and board shown in Fig. 3.11 and Fig. 3.21. The low-side FET (IGOT60R070D) was fixed, while the high-side FET was varied among the GaN devices in Table 3.3. All tests were conducted at 200 kHz. Resulting waveforms are shown in Fig. 3.22(a) and 22(b) for $V_{dc} = 100\,V$ and $200\,V$, respectively. As expected, IGOT60R070D—having the highest R_{OSS} and lowest Q-factor (Fig. 3.20)—shows the most damping (blue curve), consistent across both voltages. Damping increases for all devices with V_{dc}, aligning with Fig. 3.20(a), where R_{OSS} rises with voltage, enhancing energy dissipation and ringing suppression. Notably, a crossover occurs between GS66508T and TP65H150G4LSG: at 100 V, GS66508T has higher R_{OSS} and more damping (Fig. 3.22(a)), but at 200 V, TP65H150G4LSG surpasses it, showing greater damping (Fig. 3.22(b)). These results confirm that high-side FET choice significantly affects switching waveform damping.

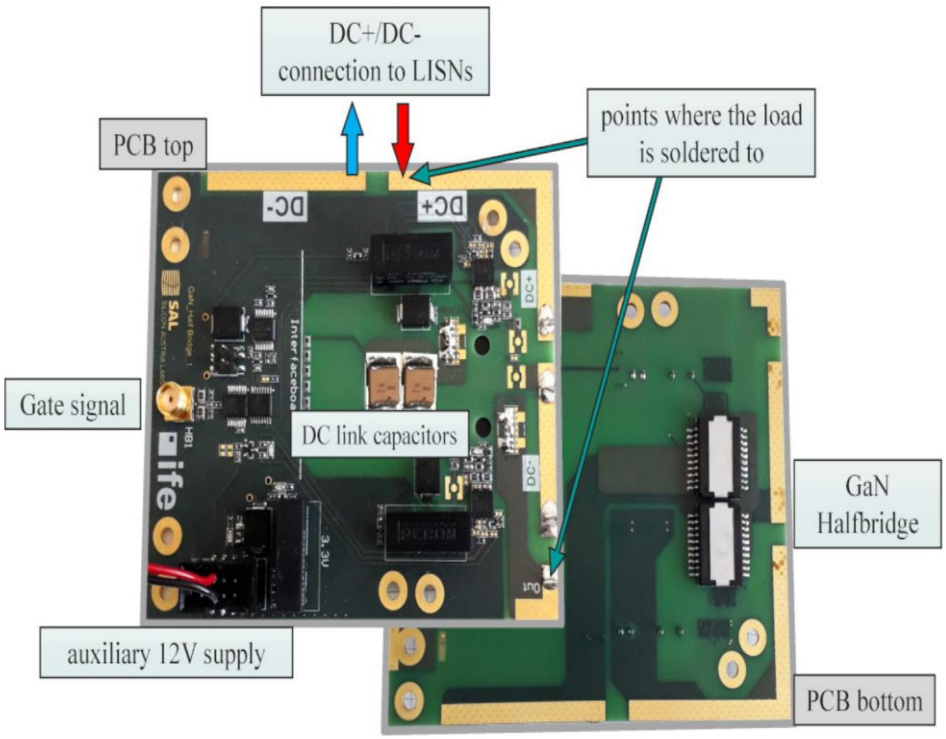
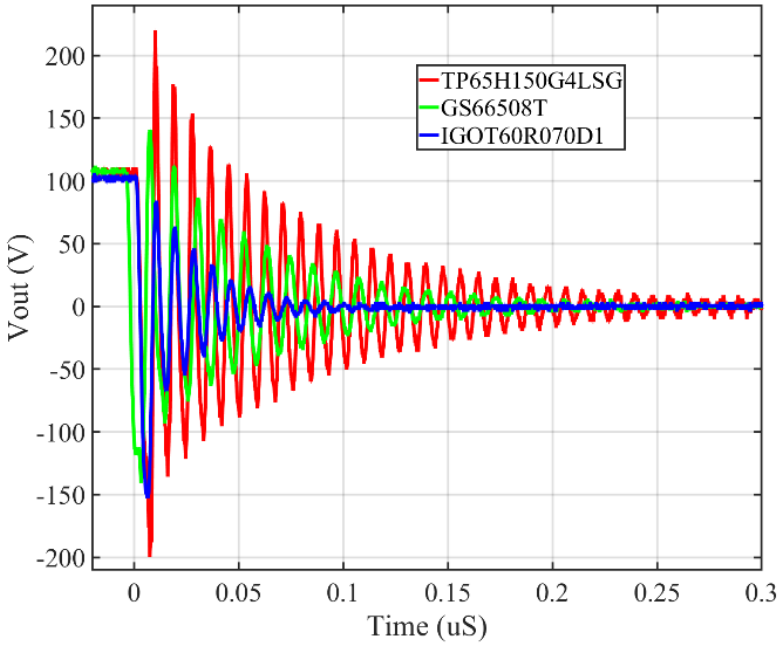
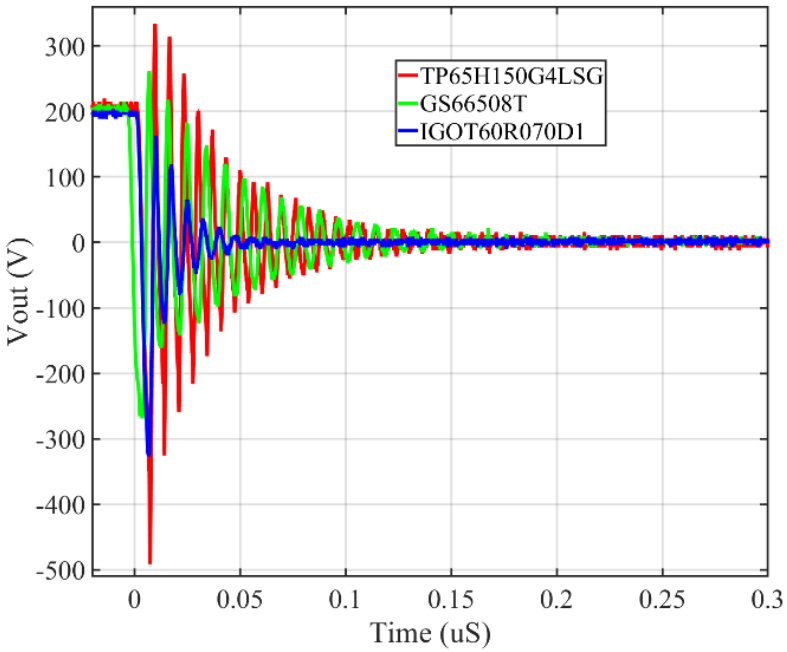


Fig. 3.21: Top and bottom views of the GaN half-bridge test PCB.



(a)

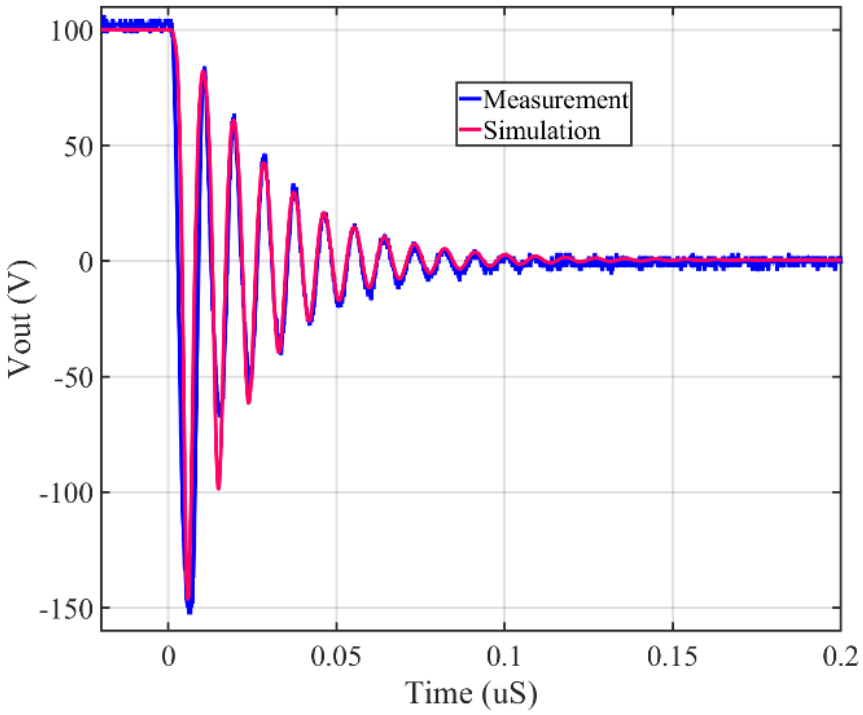


(b)

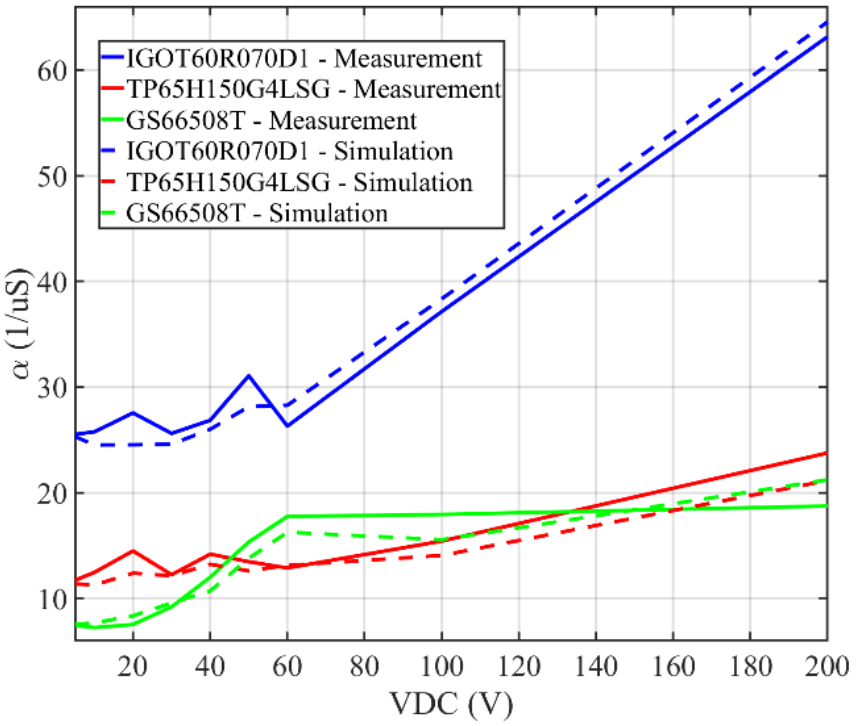
Fig. 3.22: Switching node waveforms with different high-side GaN devices at: (a) 100 V. (b) 200 V.

2.4.5.2 Time-Domain Validation of the Proposed Model

To validate the proposed compact GaN device model shown in Fig. 3.14, time-domain LTspice simulations were performed replicating the previous measurements. These simulations employed the device model described in Fig. 3.14 for each of the three GaN devices. As an example, Fig. 3.23(a) compares simulated and measured switching node waveforms for the IGOT60R070D at $V_{dc} = 100\,V$, showing excellent agreement. Fig. 3.23(b) presents the simulated exponential decay rate α across various voltages, also aligning well with measurements. Furthermore, the close correlation between the simulated α values and the measured R_{OSS} values from Fig. 3.20(a) supports the model's accuracy in capturing the damping behavior of different GaN devices.



(a)



(b)

Fig. 3.23: (a) Simulated vs. measured switching waveform for IGOT60R070D. (b) Decay rate α across voltages.

2.4.6 EMI Prediction Based on R_{OSS} Inclusion

2.4.6.1 Conducted Emission Measurements and Setup

To further assess the impact of high-side FET selection on conducted emissions, measurements were performed using the setup in Fig. 3.24 and the half-bridge board from Fig. 3.21. The tests followed the CISPR 25 voltage method [45], with the board and load positioned 50 mm above a metal table. Two LISNs [46] were connected between the power supply and the board, and an EMI receiver at the positive LISN captured the EMI spectrum. A 10 Ω resistor in series with a 10 µH inductor was used. As before, the low-side FET (IGOT60R070D) remained fixed, while the high-side FET was varied among the three GaN devices.

Fig. 3.25 shows the measured conducted emission spectra for the three devices operating at a switching frequency of 200 kHz across three different bus voltages: 30 V, 60 V, and 100 V, up to 150 MHz—the upper limit of the LISN characterization range. Across all voltage levels, the results consistently demonstrate that the choice of high-side FET significantly influences the damping of the spectral content near the resonance (ringing) frequency.

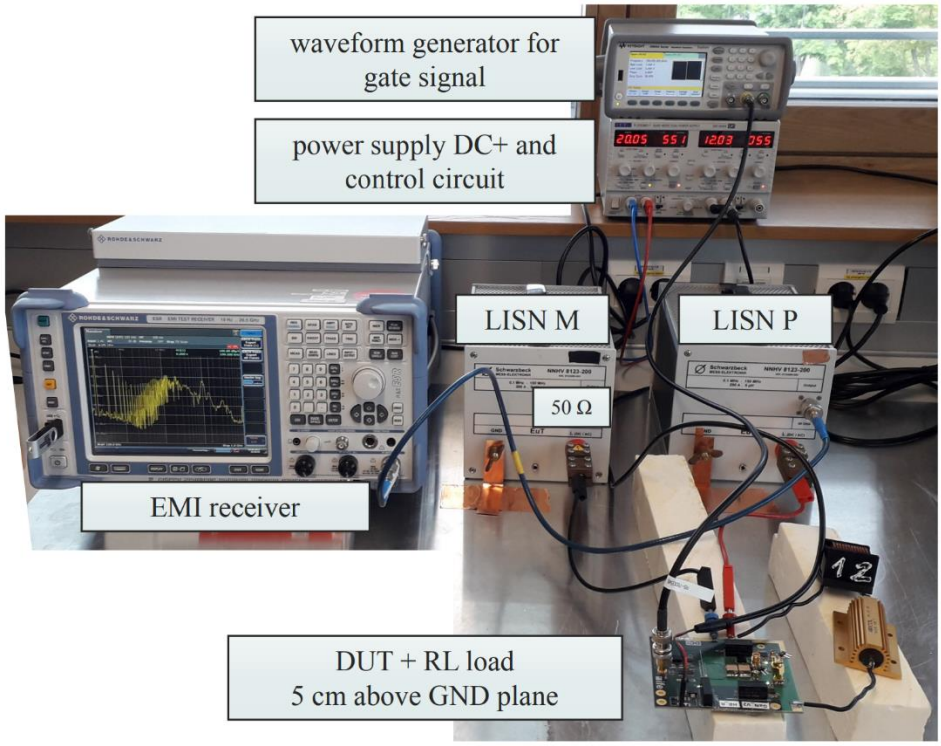
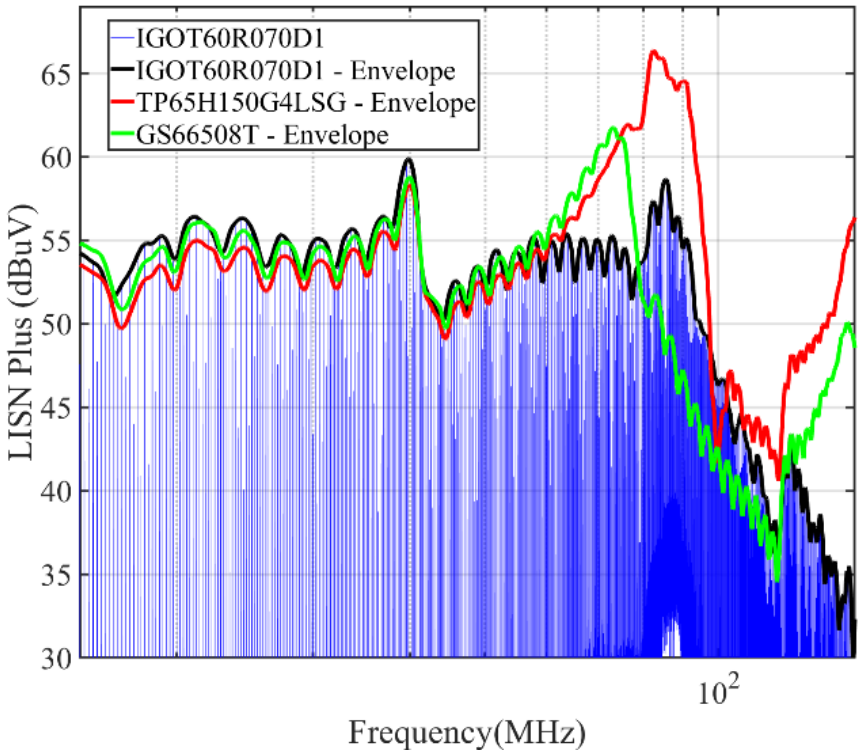
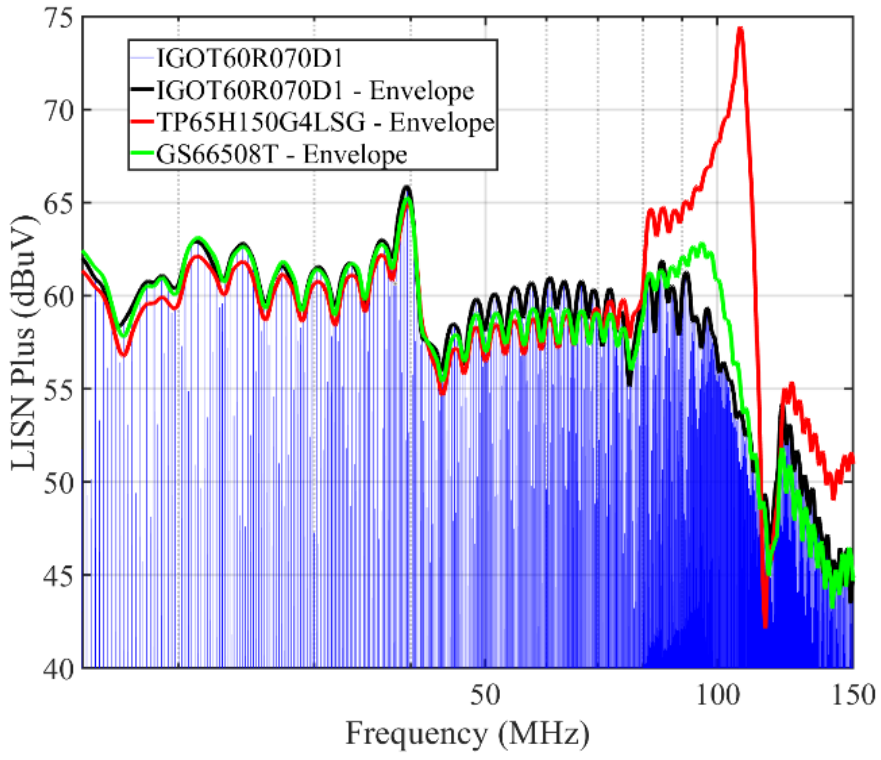


Fig. 3.24: Conducted EMI test setup with LISNs and load positioned above a ground plane.

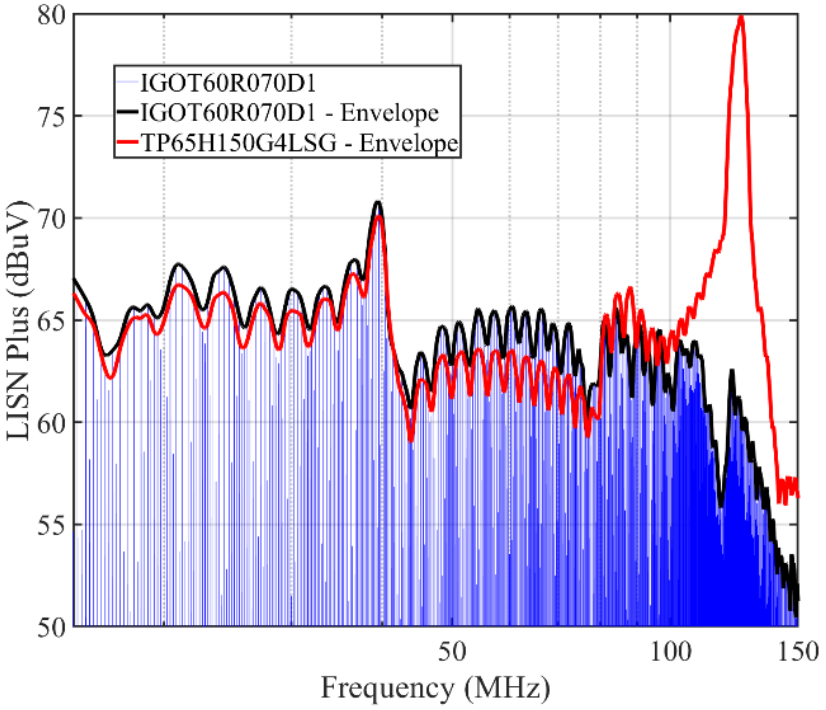
Below approximately 40 MHz, all three devices exhibit similar emission behavior. In this region, conducted EMI is dominated by common-mode noise coupling through the load impedance and parasitic elements, which is relatively independent of the switching device characteristics. However, above 40 MHz, the resonance between the output capacitance (C_{OSS}) and switching loop inductance becomes the primary factor shaping the EMI spectrum. As the bus voltage increases, the resonance peak shifts to higher frequencies, moving from approximately 60–100 MHz at 30 V, to 80–120 MHz at 60 V, and to 100–140 MHz at 100 V. This upward frequency shift is attributed to the voltage-dependent reduction in C_{OSS}. In Fig. 3.25(a) at 30 V, differences among devices are moderate, with IGOT60R070D exhibiting slightly greater damping compared to TP65H150G4LSG and GS66508T. At this lower voltage, R_{OSS} values are smaller across all devices, reducing their impact on spectral damping. In Fig. 3.25(b) at 60 V, differences become more pronounced. IGOT60R070D, which has a higher R_{OSS}, demonstrates substantially improved damping, resulting in lower spectral peaks near resonance. Meanwhile, TP65H150G4LSG and GS66508T show higher peaks, consistent with their lower measured R_{OSS} values at this voltage. In Fig. 3.25(c) at 100 V, the disparities reach their maximum. The IGOT60R070D device shows the highest damping effect, while TP65H150G4LSG exhibits up to 15 dB higher peak emissions near the resonance frequency. This clear separation underscores the dominant role of R_{OSS} in controlling the amplitude of resonance-driven EMI peaks at high bus voltages.


IGOT60R070D1
IGOT60R070D1 - Envelope
TP65H150G4LSG - Envelope
GS66508T - Envelope
LISN Plus (dBuV)
65
60
55
50
45
40
35
30
10^2
Frequency(MHz)

(a)


IGOT60R070D1
IGOT60R070D1 - Envelope
TP65H150G4LSG - Envelope
GS66508T - Envelope
LISN Plus (dBuV)
75
70
65
60
55
50
45
40
50
100
150
Frequency (MHz)

(b)



(c)

Fig. 3.25: Measured conducted emissions with different high-side devices at: (a) 30 V. (b) 60 V. (c) 100 V.

2.4.6.2 Simulated vs. Measured EMI Performance

To evaluate the predictive capability of the proposed compact GaN device model, LTspice simulations replicating the conducted emission tests were performed. The complete simulation setup is shown in Fig. 3.26 and incorporates models of the LISNs, DC-link capacitors, and, crucially, the measured load impedance [28]. The load impedance was characterized through a combination of differential-mode S-parameter measurements using a network analyzer and common-mode capacitance extraction via impedance analyzer, as described in [1]. The impedance data were processed and converted into a SPICE-compatible model using the IdEM tool in CST Studio Suite [11].

Fig. 3.27(a) compares measured and simulated conducted emissions across the entire frequency range up to 150 MHz (V_{dc}= 100 V). Up to around 40 MHz, the accuracy of the simulation mainly depends on how well the load model matches the real system. In this range, the common-mode capacitor in the load plays a major role in creating the spectral peak near 40 MHz. Above this frequency, the behavior is mainly influenced by the switching device's built-in characteristics, especially R_{OSS}.

Figures 3.27(b), 27(c), and 18 provide detailed views around the resonance regions, where differences in device behavior become critical. When R_{OSS} is included in the GaN transistor model (green curves), the simulation results align closely with measurements, accurately reproducing both the resonance

frequency and the damping behavior. In contrast, neglecting R_{OSS} (red curves, setting R_{OSS}=0) results in significant underestimation of damping, leading to an over prediction of EMI peaks by up to 14 dB for the IGOT60R070D device at 60 V. Devices with lower measured R_{OSS} show smaller, though still noticeable, discrepancies (between 3 and 6 dB).

Across all devices and voltages, the simulation results confirm that R_{OSS} is a critical loss mechanism governing the damping of parasitic resonances and, consequently, the spectral amplitude near those resonances. The close match between simulated and measured EMI spectra validates the accuracy of the proposed compact model and underscores the necessity of including R_{OSS} when aiming for realistic EMI predictions.

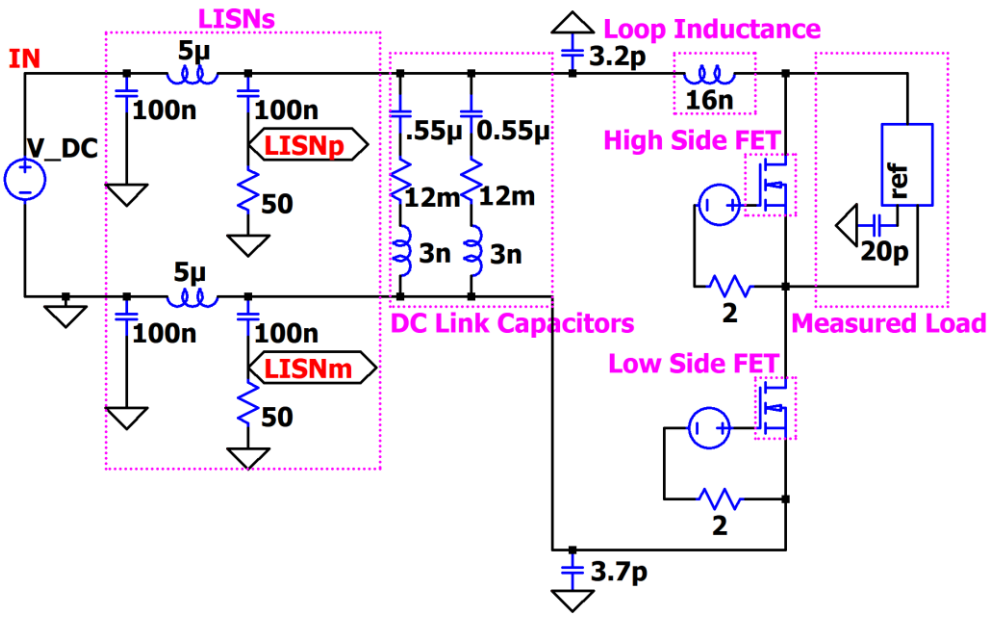
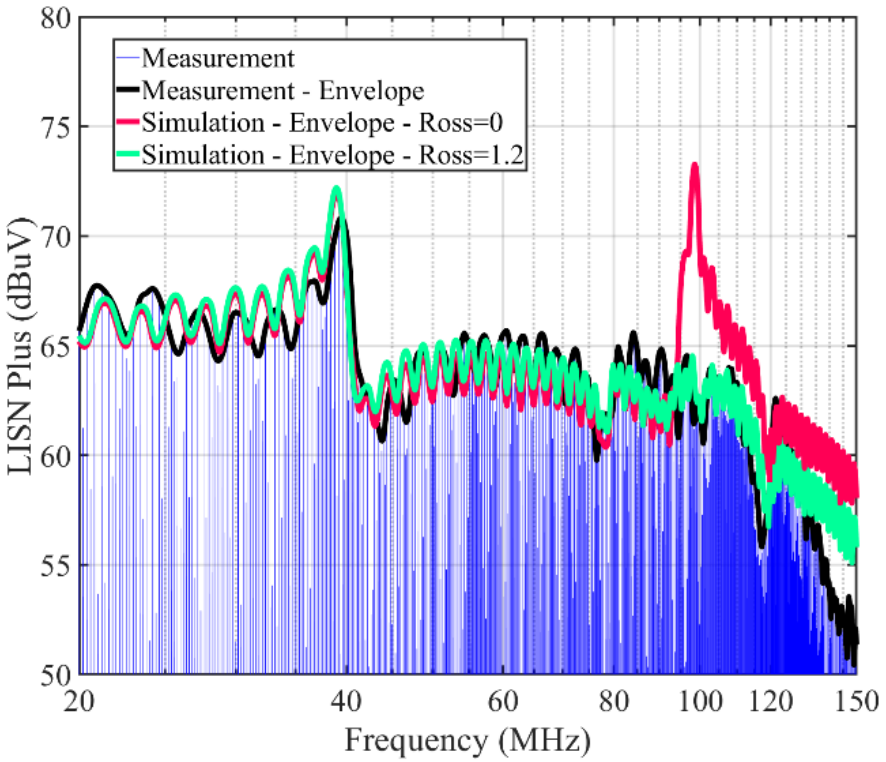
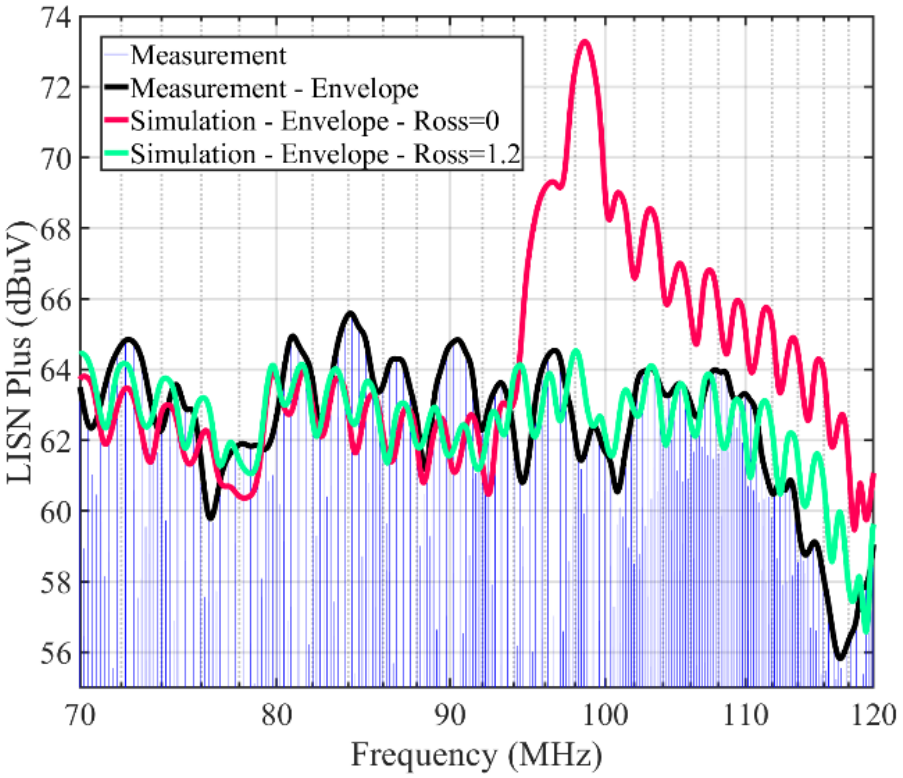


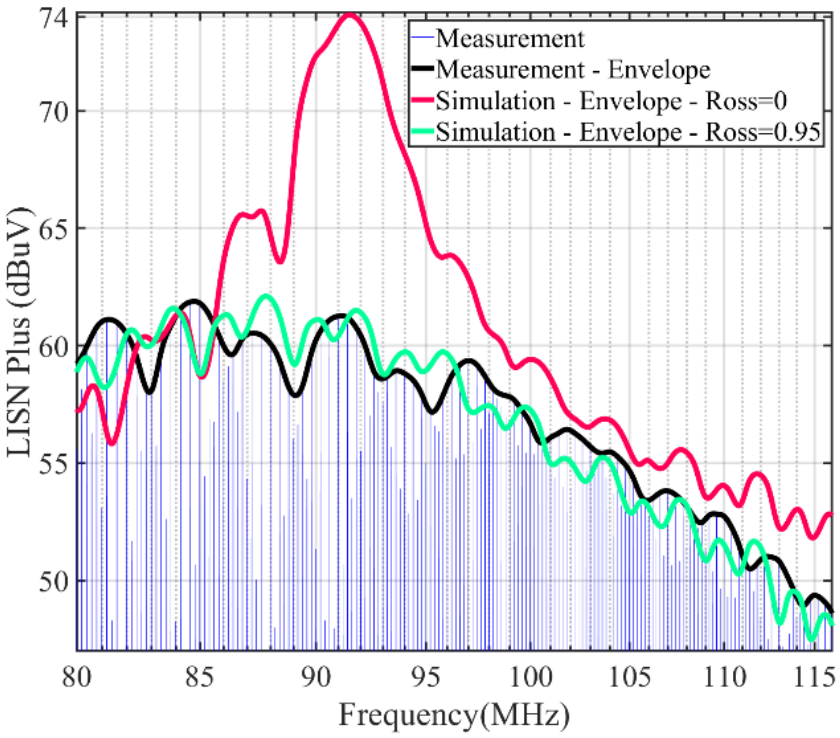
Fig. 3.26: LTspice simulation setup for conducted EMI modeling including load and LISN networks.


Measurement
Measurement - Envelope
Simulation - Envelope - Ross=0
Simulation - Envelope - Ross=1.2
LISN Plus (dBuV)
Frequency (MHz)
80
75
70
65
60
55
50
20
40
60
80
100
120
150

(a)

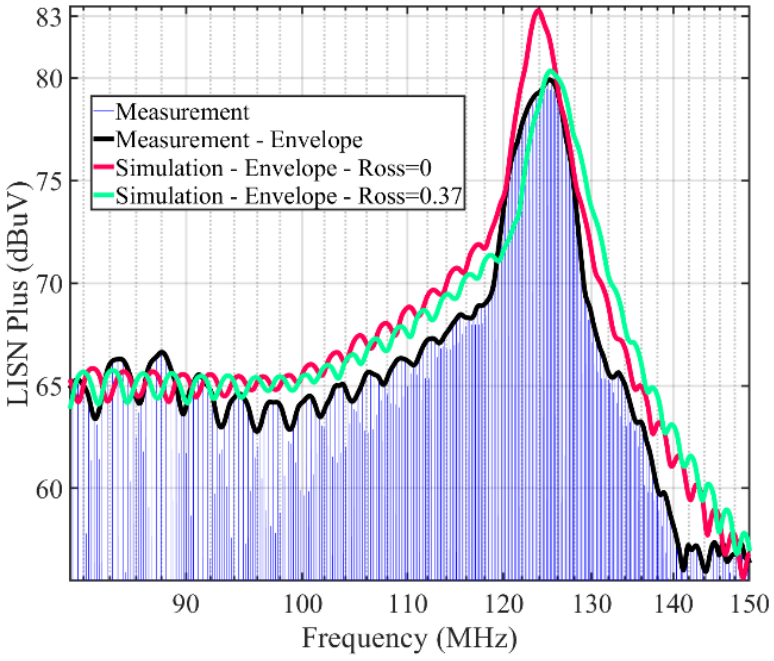

Measurement
Measurement - Envelope
Simulation - Envelope - Ross=0
Simulation - Envelope - Ross=1.2
LISN Plus (dBuV)
Frequency (MHz)
74
72
70
68
66
64
62
60
58
56
70
80
90
100
110
120

(b)

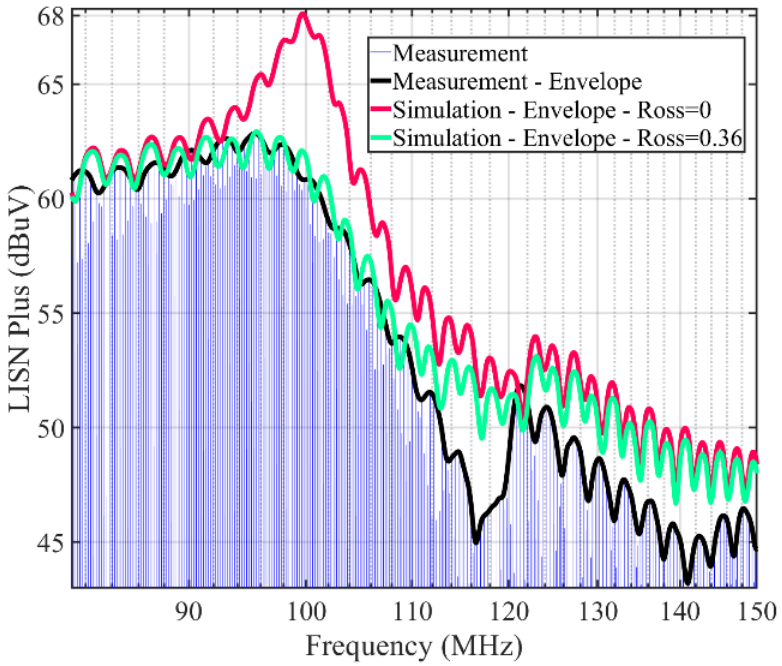


(c)

Fig. 3.27: Simulated vs. measured conducted EMI for the IGOT60R070D: (a) Full band at 100 V (b) Zoom at 100 V. (c) Zoom at 60 V.



(a)



(b)

Fig. 3.28: Simulated vs. measured conducted EMI: (a) TP65H150G4LSG at 100 V. (b) GS66508T at 60 V.

2.4.7 Conclusion

This paper presents a detailed investigation into the role of the resistive component of the output capacitance, ROSS, in the EMI behavior of GaN-based power converters. A high-precision extraction methodology based on S-parameter measurements was developed, validated against known passive components, and applied to several commercially available GaN devices. Results demonstrate that ROSS is strongly voltage-dependent and varies significantly among different device types and manufacturers. A compact behavioral model incorporating voltage-dependent ROSS was implemented in LTspice and validated through time-domain switching measurements and conducted EMI experiments. The inclusion of ROSS in the transistor model substantially improved the correlation between simulated and measured switching node waveforms and EMI spectra, reducing prediction errors by up to 14 dB near the resonance frequencies. Across all tests, ROSS was found to be a dominant parameter governing the damping of parasitic oscillations and the suppression of resonance-driven conducted EMI peaks. These findings highlight the need to incorporate ROSS into device modeling, design optimization, and device selection processes, particularly for high-frequency, EMC-critical applications. By bridging the gap between device-level physics and system-level EMI performance, the proposed methodology provides a practical pathway toward predictive EMC design in GaN-based power electronics. Future work will focus on extending the ROSS modeling to dynamic switching conditions and exploring its impact on radiated EMI behavior and overall system robustness.

2.4.8 My Scientific Contribution

This paper presents a comprehensive investigation into the influence of the resistive component of output capacitance (ROSS) on the electromagnetic compatibility (EMC) performance of GaN-based power converters. The study demonstrates that ROSS can significantly contribute to resonance phenomena commonly observed in electromagnetic interference (EMI) measurements. A behavioral compact model of a GaN high-electron-mobility transistor (HEMT) was developed and implemented in LTspice, incorporating nonlinear junction capacitances, dynamic on-state resistance, and a voltage-dependent ROSS. The ROSS parameter was experimentally extracted through S-parameter measurements using a calibrated transmission line setup, covering frequencies up to several hundred megahertz. The model was validated on three different GaN devices through both time-domain and frequency-domain measurements using a custom half-bridge test platform.

My specific contributions to this work include:

- Originating the research concept
- Designing and building the R_{OSS} measurement setup
- Developing the time-domain and frequency-domain measurement setups
- Performing all measurements, simulations, and modeling of the GaN devices

.

2.5 A PCB Based High Resistance GHz Bandwidth Voltage Pick Up for Detecting Switching Voltage

M. Gholizadeh, S. Sadeghi, A. Pak, J. Hansen, and D. Pommerenke, "A PCB-based high-resistance GHz-bandwidth voltage pick-up for detecting switching voltage," in *Proc. 2023 Int. Symp. Electromagn. Compat. (EMC Europe)*, Sep. 4, 2023, pp. 1–6.

2.5.1 Abstract

The sub-nanosecond switching of GaN transistors at high voltages challenges existing methods of transient voltage measurement. A novel printed circuit board based implementation of a capacitively compensated resistive divider is presented in this paper. The geometry balances capacitive coupling to the high voltage side with capacitive coupling to ground and longitudinal capacitances along the resistors by symmetry. Using five 2 watt resistors a 3 GHz bandwidth is achieved at 5 kOhm. An equivalent circuit derived from the geometry and the full-wave model are validated by measurements.

2.5.2 Introduction

In the design, testing and in EMC investigations of power electronics there is a need to capture voltages up to 1000 V and currents of many 10s of Ampere with GHz bandwidth. A typical situation is the characterization of disturbances of GaN and SiC transistors in the wireless command, communication and control bands and for measurements required to generate simulation models of these transistors. A prominent example is the design of power modules for electric vehicles with DC link voltages of 400 V or 800 V, and the need to monitor their switching waveforms e.g. in a double pulse test to characterize and reduce electromagnetic emission [47]-[50]. Fast high voltage pulse measurements are also typical in ion mobility spectrometry (IMS) and mass spectrometry [51].

Commercial DC high-voltage probes are limited in their ability to measure voltages. This is because the maximum voltage that can be measured drops rapidly as frequencies increase [52], [53]. High input currents are usually generated in the high-voltage probe due to the strong frequency dependence of the input impedance, and therefore affects the measured signal in a significant way. This will result in an inaccurate measurement of the waveform of the signal and is due to the parasitic capacitance in parallel with the input impedance.

For measuring fast high-voltage pulses, AC high-voltage probes are better suited since the transmission characteristics corresponds to a high-pass filter. Nevertheless, high-pass filters severely limit DC use. It is not possible to measure both AC and DC with AC high voltage probes for high DC and superimposed high AC applications [51].

A variety of such solutions is discussed in the literature. The authors in [50] present the basic principle of the RC divider voltage sensing circuit. The voltage measurement is performed with a simple PCB-based high bandwidth RC voltage divider and a high bandwidth passive voltage probe. They achieve a bandwidth of 150 MHz for the input impedance of 100 kΩ.

Van den Bossche and Bozalakov [54] present a probe based on resistive dividers and achieve a flat frequency response by tuning the parasitic capacitance between the resistors and the ground of the PCB in which they are mounted. They achieve a 3dB bandwidth of 10 MHz for an input impedance of 8 kV.

In [51], a resistive voltage divider with additional compensation capacities to extend the linear bandwidth is proposed. Frequency compensation is realized with PCB traces that form a compensation electrode located on adjacent PCB layers. The authors could achieve a bandwidth of 88 MHz, while maintaining a DC input impedance of 10 MΩ.

In this paper we present a modified capacitive compensation approach for resistive voltage dividers. It is simple and cost- effective to implement using only SMD resistors based on a special PCB design [55] (p. 154). Frequency compensation is realized with PCB traces below the series resistors, which introduces more parasitic capacitance referenced to the trace (high voltage) and thus balances the parasitic capacitance referenced to the trace and that referenced to GND (low voltage). To achieve optimal compensation to have a flat frequency response over a wide frequency range, the gap between traces and below the resistors is optimized using electromagnetic simulation with the software CST Studio Suite [56]. The equivalent circuit of the realized structure is proposed and compared with the full-wave simulated and measured results from an optimized prototype.

2.5.3 Proposed Method

Resistive voltage dividers tend to have a highly non-linear transfer function due to the increasing influence of parasitic and stray capacitances with increasing frequency. The non- linear transfer function is dependent on the topology and the resistors that are used and consists of a low-pass filter with additional GHz high-pass component.

In order to achieve a flat frequency response, we need to understand the parasitic coupling mechanisms between the resistors and the PCB on which they are mounted. We start with an equivalent circuit model and give analytical formulae to parameterize its elements. We show how to achieve a flat frequency response by suitable choice of the element values.

2.5.3.1 Proposed Equivalent Circuit

Fig. 3.29 shows five SMD resistors soldered in series on a microstrip transmission line with all the parasitic capacitors that can be taken into account (the parasitic capacitors are only shown for the first two resistors). The parasitic capacitors can be divided into those referenced to the trace ($Cs1$, $Cs2$ and CM shown in blue) and those referenced to GND ($Cg1$ and $Cg2$ shown in red).

$Cs1$, $Cs2$ and CM are the parasitic capacitances of the resistors and $Cg1$ and $Cg2$ are the parasitic capacitances formed by GND and the resistors. The proposed equivalent circuit of a resistor above GND with all parasitic capacitors is shown in Fig. 3.30. The resistor values and the impedances of the

capacitors are much larger than the inductances associated with the resistors. Thus, the inductances are not considered in the resistor equivalent circuit. To simplify, all capacitors are considered to be parallel plate capacitors ($C = \varepsilon 0 \varepsilon r A/d$) and they are calculated according to Table 3.4 where R is the value of the individual resistances. In the figure, CM is the approximated parallel plate capacitor between the two metallic edges of the resistor. Since the SMD resistor itself is divided by three regions in respect to its parasitic capacitors ($Cs1$ and $Cs2$) the resistive value (R) is also divided according to the three regions ($R1$ and $R2$). $CS1$ is less than what can be calculated from the parallel plate formula, because the stress voltage increases linearly along the surface. We choose to divide the parallel plate capacitance formula by 2 and later check in simulation the validity of this assumption. CM is assumed to be $(CMmin + CMma)/2$ since we take the maximum and minimum estimates and average them.

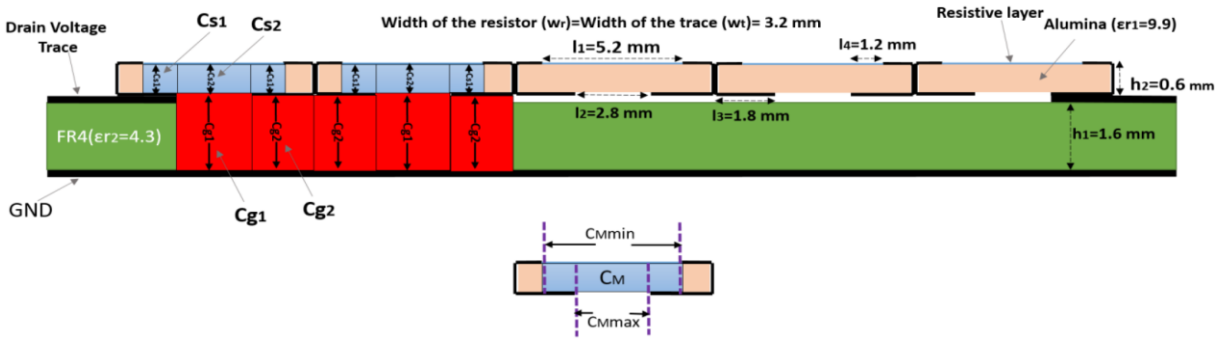


Fig. 3.29: Schematic of five SMD resistors soldered in series on a microstrip transmission line with all the parasitic capacitors (the parasitic capacitors are only shown for the first two resistors and avoided in the other section not to clutter the drawing).

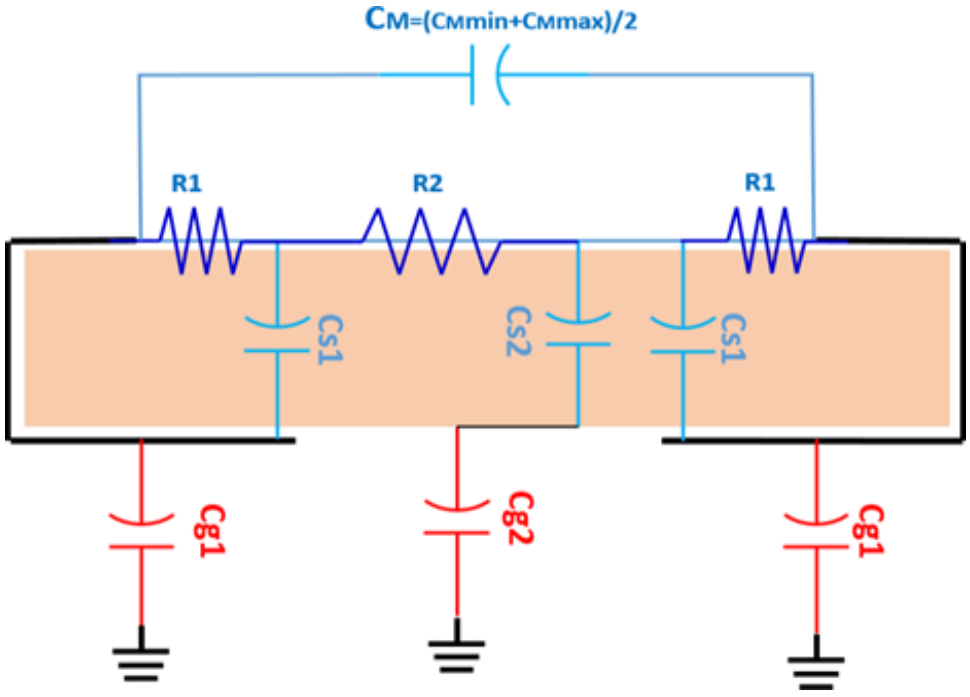


Fig. 3.30: Proposed equvalent circuit of a resistor above GND accounting for all parasitic capacitors.

Table 3.4: Parameter of the equvalent circuit shown in Fig. 3.30.

Parameter	Formula
R1	$\frac{l4}{l1} * R$
R2	$\frac{l2}{l1} * R$
Cs1	$\frac{\varepsilon_0 \varepsilon_{r1}(l_4 w_r)}{2 * h_2}$
Cs2	$\frac{\varepsilon_0 \varepsilon_{r1}(l_2 w_r)}{h_2}$
Cg1	$\frac{\varepsilon_0 \varepsilon_{r2}(l_2 w_r)}{h_1}$
Cg2	$\frac{\varepsilon_0 \varepsilon_{r2}(l_3 w_r)}{h_1}$
CMmin	$\frac{\varepsilon_0 \varepsilon_{r1}(h_2 w_r)}{l_1}$
CMmax	$\frac{\varepsilon_0 \varepsilon_{r1}(h_2 w_r)}{l_2}$

2.5.3.2 The Novel Twist

Fig. 3.32 shows the simulation results of the structure in Fig. 3.29 in Keysight ADS [56] using the proposed resistor equivalent circuit. In this figure, the effect of the capacitor referenced to the trace and those referenced to GND are shown separately. As can be seen, in such structures the effect of the parasitic capacitors referenced to GND (red curve) dominates the effect of those referenced to the trace (blue curve). Therefore, if the effect of the capacitors referenced to the trace can be somehow increased, then some level of balance can be achieved.

One way to increase the impact of the capacitors that are referenced to the trace is to place some of the resistors on top of the trace and the others on top of a section where the trace is omitted. In fact, they are on top of GND (Fig. 3.31). The newly introduced capacitors between the resistors and the trace (C_{t1}= $\varepsilon_0 \varepsilon r_3 (l_3 w_r)/ h_3$ and C_{t2}= $\varepsilon_0 \varepsilon_{r3} (l_2 w_r) / h_3$) can significantly increase the total capacitance with respect to the trace and the structure can have a flat frequency response up to a few GHz only by optimizing the gap length under the resistors (lg). Of course, one can do the optimization for all the three variable parameters , and $h3$ and $\varepsilon r3$ of Cti . However, for simplicity, the dielectric layer parameters ($h3$ and $\varepsilon r3$) are chosen to have fixed values. Then, the flatness of the frequency response is a function of lg only.

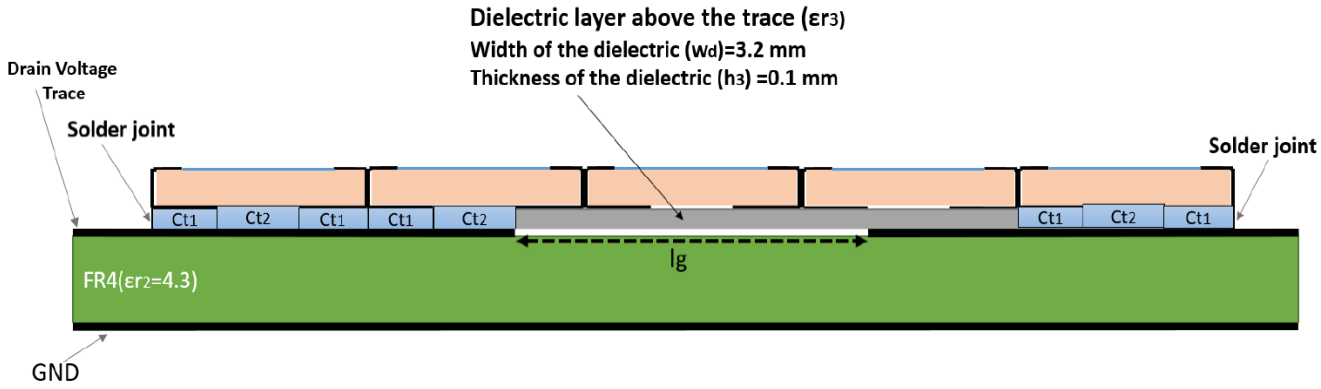


Fig. 3.31: Enhanced PCB layout for resistive voltage probe showing alternating placement of SMD resistors above trace and ground planes. This configuration increases capacitance referenced to the high-voltage trace (Ct1, Ct2) to balance parasitic capacitances and achieve a flat frequency response up to several GHz.

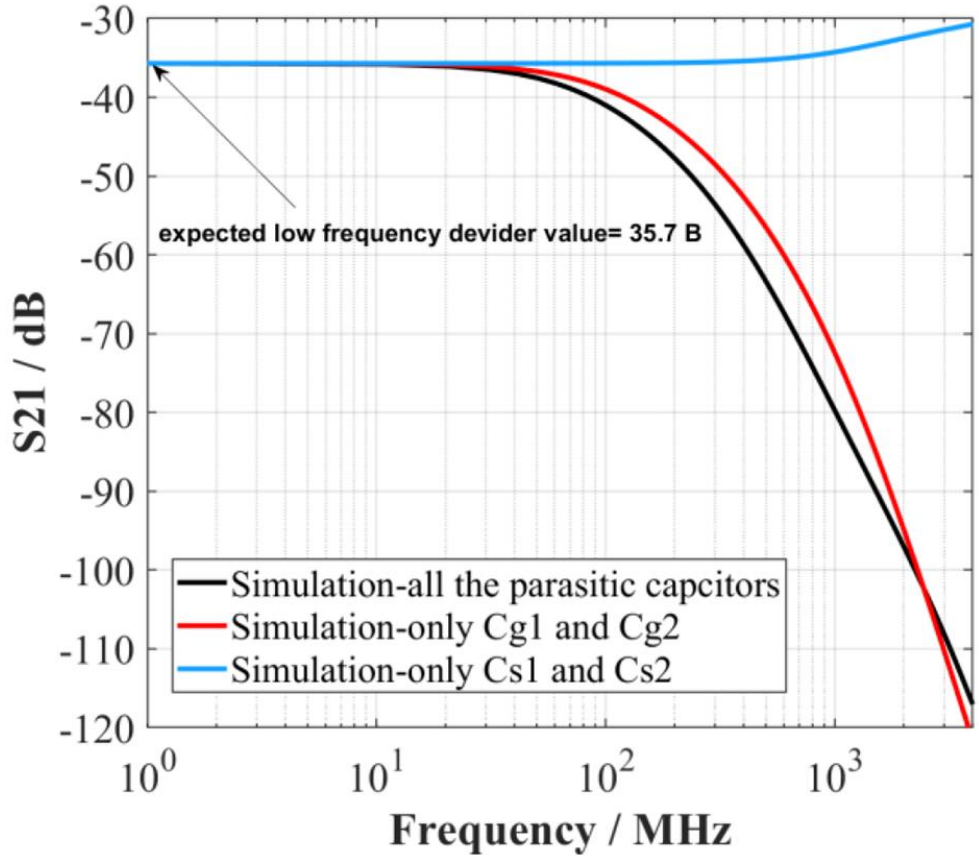


Fig. 3.32: Simulated and measured results of the structure shown in Fig. 3.29.

2.5.3.3 Full Wave Model Setup and Verification

To optimize the length of the gap below the resistors ( ), we generate a full-wave simulation of the structure in the software CST Studio Suite [11]. This requires a reliable full- wave model of the resistance. Fig. 3.33 shows the proposed full- wave model of the SMD resistors, with the dimensions taken from the data sheet [57]. The model consists of perfect electric conductor (PEC) parts at the edges, dielectric layer (Alumina $\varepsilon r3$= 9.9), and a sheet lumped element on top of the dielectric layer connecting the two metallic parts. We validate the CST model of the resistors using a structure with one and with two resistors in series in the center of a microstrip transmission line and above the GND. We simulate and measure S11 and S21 of this structure and compare the results in Fig. 3.24. Up to 4 GHz, the proposed full-wave model of the resistor deviates from the measurements less than 3 dB. As a consequence, we can use this 3D model of the resistors in the 3D simulation of the entire voltage pick up to optimize the length lg.

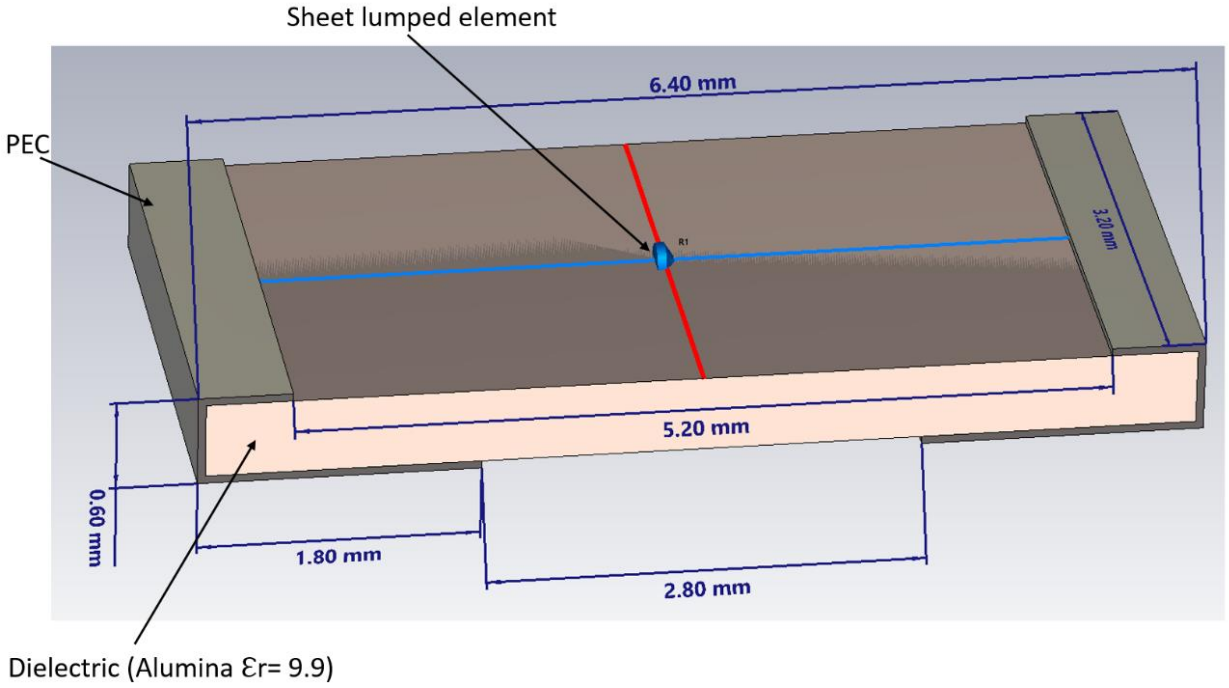


Fig. 3.33: Full wave model of the resistor.

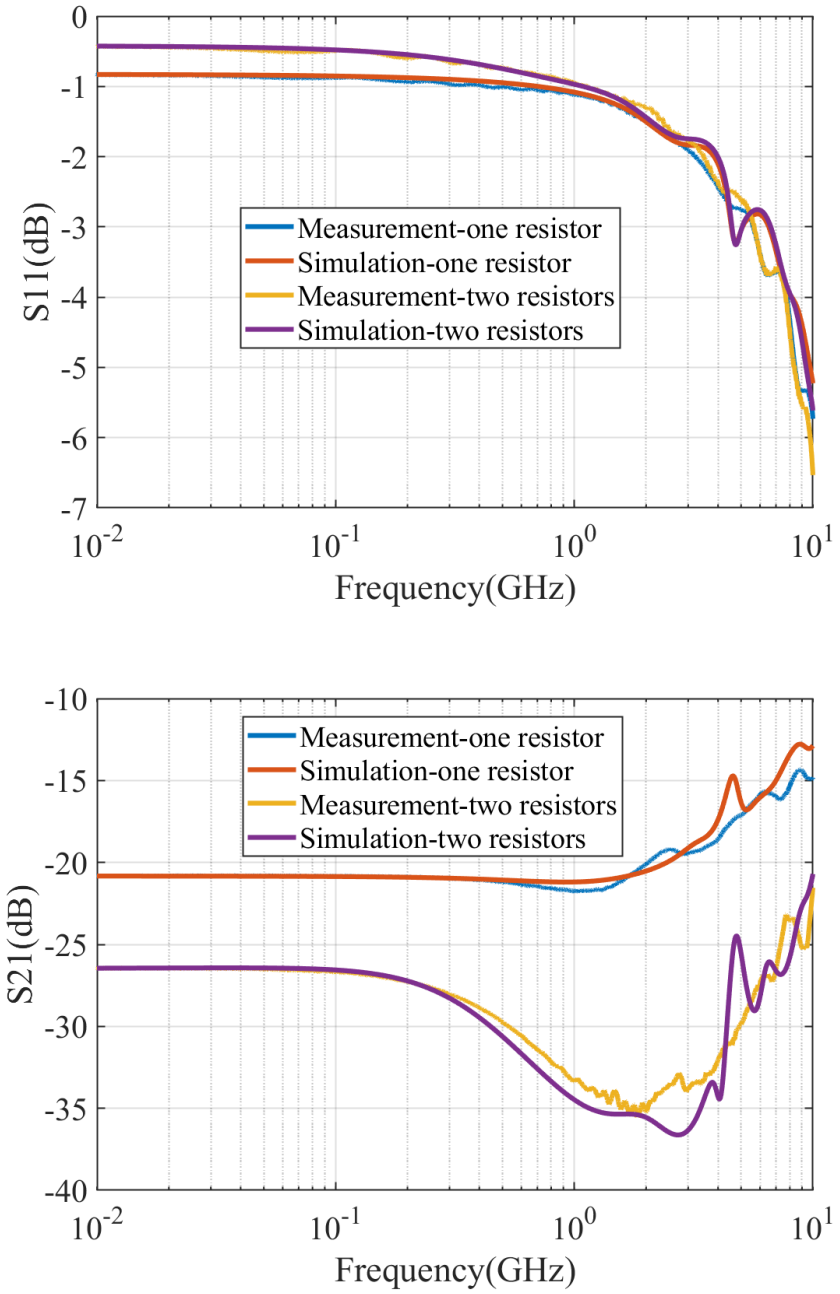


Fig. 3.34: Comparison between simulated and measured results of one/two resistors in series placed in the center of a microstrip transmission line and above the GND (S_11 and S_21).

2.5.4 Capacitance Optimization and Realization in Hardware

We generate a 3D simulation model of the structure shown in Fig. 3.31. We use fixed dielectric layer parameters $wd = 3.2\ mm$, $h3 = 0.1\ mm$ and $\varepsilon r3 = 3$. The model is used to optimize the length lg of the opening below the resistors. Considering a deviation of ±3 dB from a flat frequency response, the optimum length is obtained as $(optimum) = 10\ mm$ (see Fig. 3.31).

Based on this optimization, a probe is designed using the geometric parameters of the simulation model with five 1kΩ resistors in series (SMD 1K OHM 1% 2W 2512). A picture of this 5 kΩ probe is shown in Fig. 3.35. The $S21$ of this probe is measured and simulated, using both CST and ADS simulations. The equivalent circuit of the ADS simulations is shown in Fig. 3.27.

Fig. 3.36 shows the comparison between simulation and measurement. Tolerating a deviation of ±3 dB from a flat frequency response, the probe works well up to 3 GHz. As can be seen, the full wave simulation of CST Studio Suite follows the measurement with a deviation of less than 1.5 dB. The ADS simulation which uses the simple equivalent circuit models of the resistors deviates more than 3d B above 500 MHz.

Using full wave simulation, it is easy to check the bandwidth as a function of the resistance value of the probe. Here we kept the resistor size, traces etc. just changed the resistor values to understand the trace-off between resistor value and bandwidth for one layout geometry. No further optimization was performed. The full-wave simulation results for the trade-off between bandwidth and probe resistance values are shown in Fig. 3.38 for five resistors in series. The bandwidth (±3 dB deviation from a flat response) decreases from 4.5 GHz for a 1 kΩ probe to 0.55 GHz for a 100 kΩ probe.

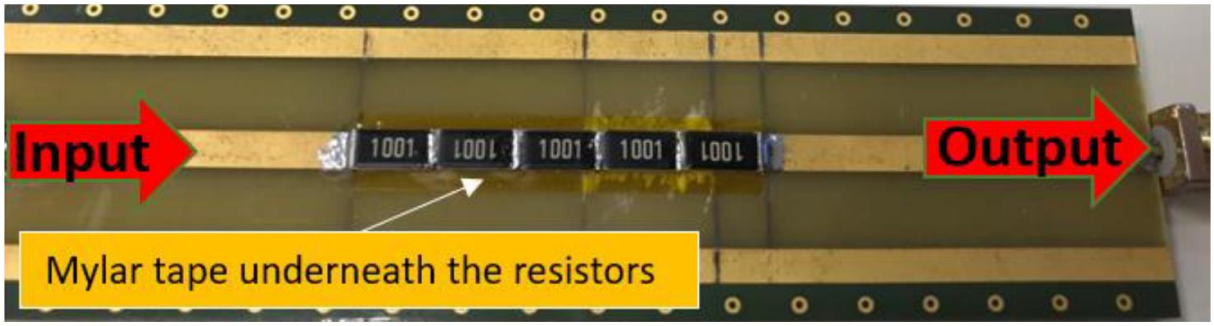


Fig. 3.35: Fabricated high-resistance voltage probe consisting of five 1 kΩ SMD resistors (2512 package) soldered in series on a microstrip transmission line. The design implements capacitive balancing through optimized PCB geometry to achieve a flat frequency response and 3 GHz bandwidth.

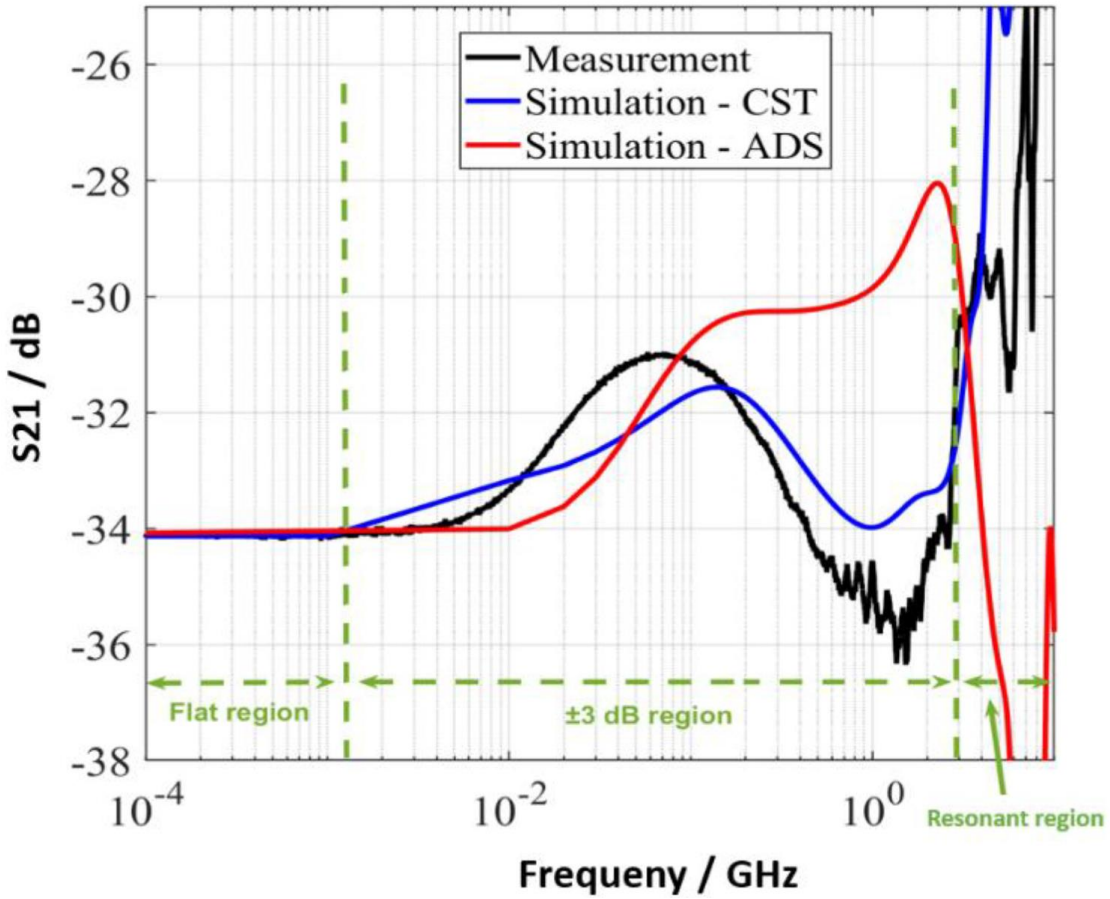


Fig. 3.36: Simulation and measurement of the structure shown in Fig. 3.32 (5 KOhm probe).

2.5.5 Transient Voltage Behavior

While most publications analyze the frequency response and show transfer pulse data, they do not analyze the instantaneous stress on the individual resistors. Fig. 3.39 shows a full wave simulation of the voltage levels across the resistors when a 300 ps fast pulse step of 1000 V is applied (5 kΩ probe). As can be seen, the voltage across $R1$, $R4$, and $R5$ increases smoothly from 0 V to 200 V. However, the voltage across $R2$ and $R3$ converges to 200V after 15 ns only after a strong overshoot (700V - 800V). The fast pulse with a 300 ps rise time causes ringing in the voltages across the resistors in both the full wave and ADS models. The ringing frequency is both for ADS and the full wave simulation about 1.2 GHz. We associate it with the traces under the resistors. They form a capacitively loaded resonator. This frequency does not appear in the transfer function S21. We would expect that the triangular compensation structure used in [51] also resonates as a capacitively loaded transmission line.

The data shows ringing mainly over the center resistors. The simulated voltages reach 800 V at 1.2 GHz for a 1kV step function. However, multiple loss mechanisms are not included in this simplified calculation, so the actual ringing should be highly attenuated. The ringing needs further investigation.

Eventually we investigate whether the strong voltage overshoot could yield to sparking. Sparking takes at least nanoseconds to develop. For about 2 nanoseconds there is most of the voltage drop across *R*2 and *R*3. However, this is not long enough to spark over. The DC breakdown of the resistor structure, estimated from its length, disregarding thermal limits is larger than 3kV estimated from the distance of 3.2mm. The total resistor chain has 3 x 3.2mm gaps and the gap between the trace ends is 10mm. Sparking should certainly not occur below 10 kV without any potting material, such as spray on silicon rubber. The other limit is the short- term change of resistance values, usually specified by the voltage coefficient. For the anti/surge resistors used there is no voltage coefficient provided by the manufacturer, but a maximal pulse voltage of 600 V is specified for every resistor. Based on this analysis we conclude that the short-term limit is above 3 kV. The thermal limit is 230V rms for 5 kΩ. We conclude that sparking in this structure is unlikely.

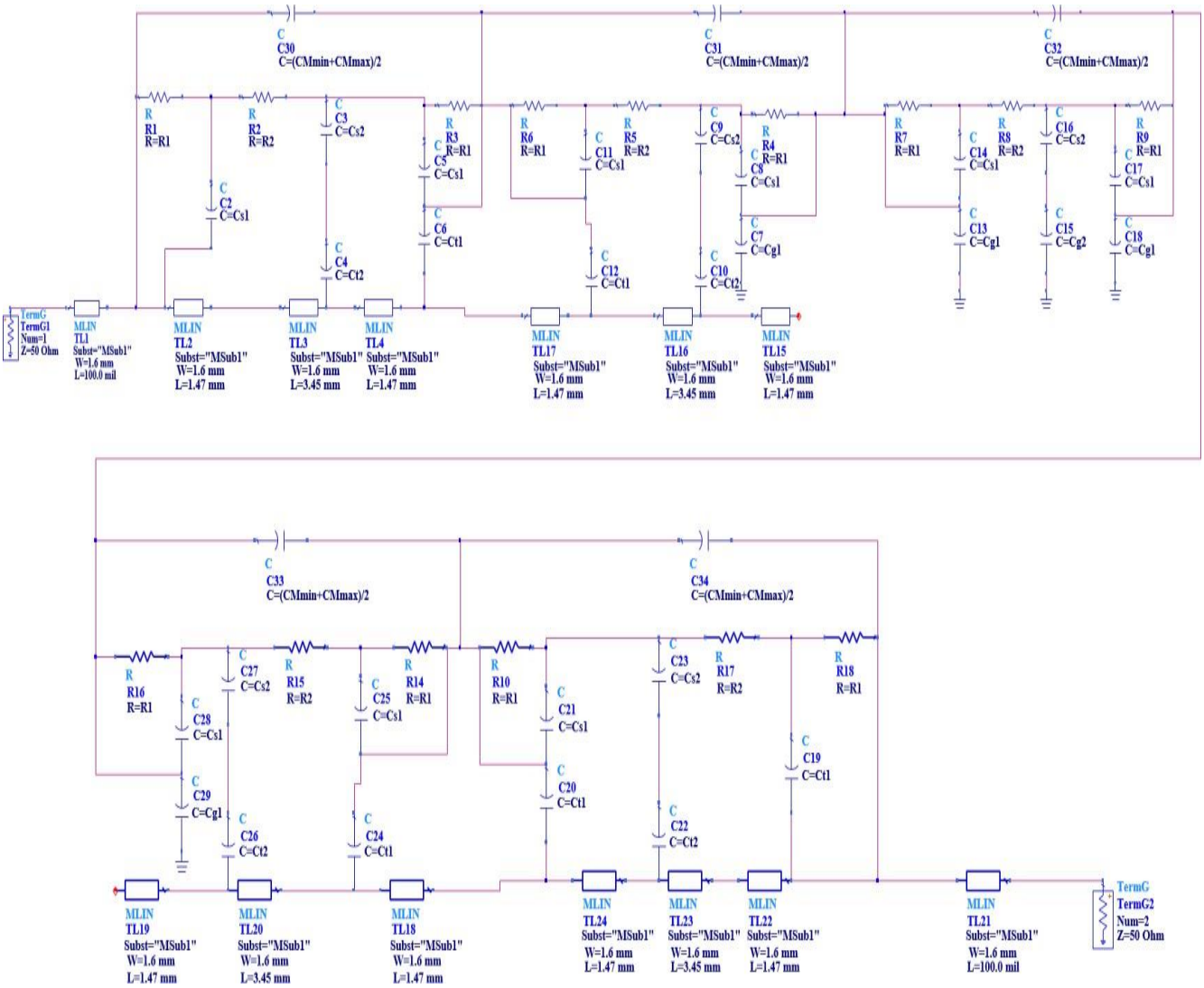


Fig. 3.37: Equivalent circuit of the structure shown in Fig. 3.32 in ADS.

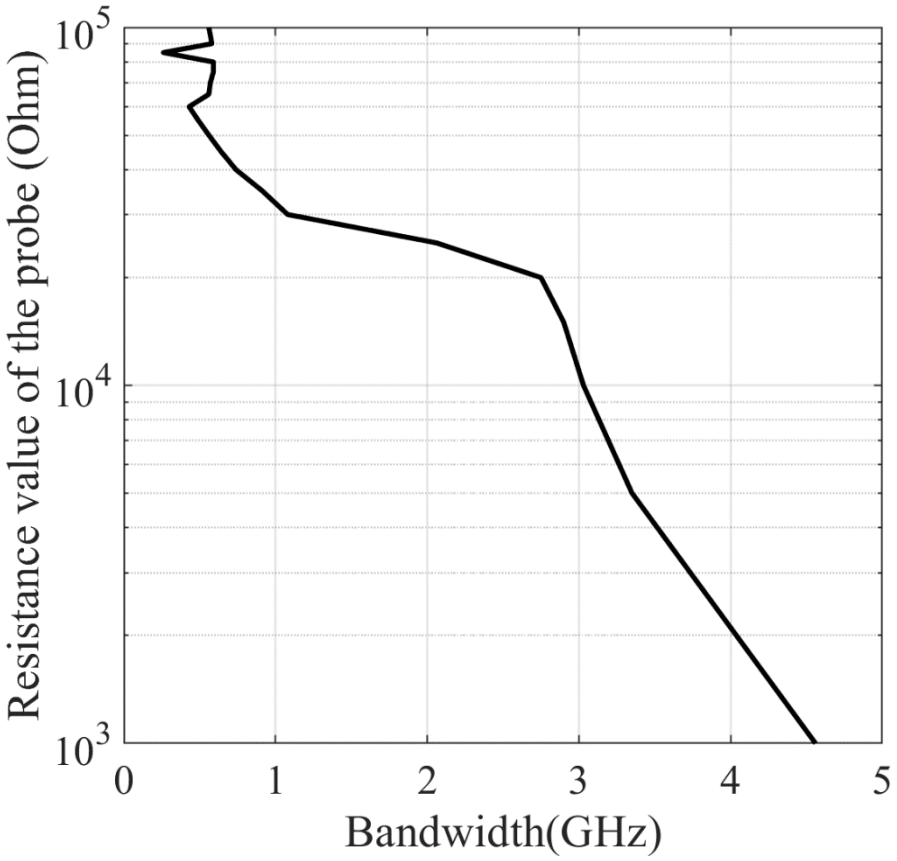


Fig. 3.38: Full wave simulation: bandwidth vs. the resistance value of the probe (5 resistors in series).

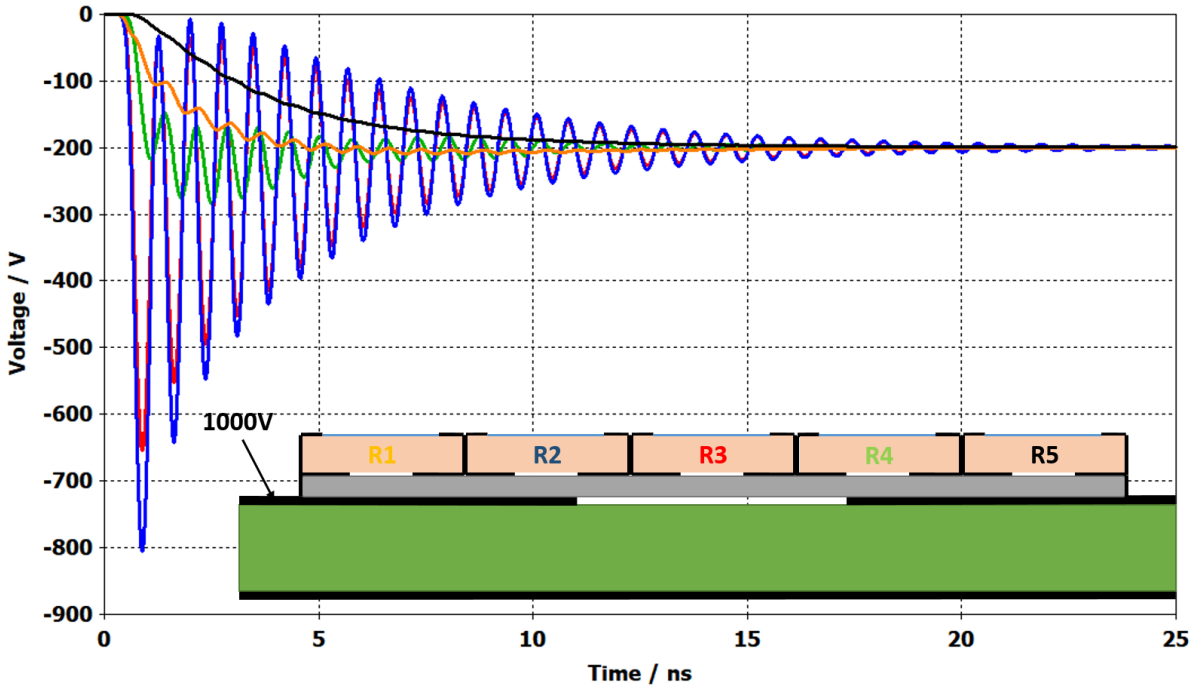


Fig. 3.39: Full wave simulation: voltage distribution over each resistor (1000V is applied). The color of the resistor in the inset is identical to the color of its corresponding voltage graph.

2.5.6 Conclusion

An integrated high voltage probe with GHz bandwidth has been presented using a novel design. The design is based on tuning the parasitic capacitances referenced to the trace and those referenced to the ground of the PCB on which they are mounted. SMD resistors (SMD 1K OHM 1% 2W 2512) are used to realize a 5 kΩ voltage pick up probe. The equivalent circuit and full-wave model of the given structure are proposed and results show good agreement with measurements. It has been shown that a flat frequency response with a 3 dB bandwidth of 3 GHz can be obtained for the given structure. The trade-off between the bandwidth and the probe resistance is investigated using full-wave simulation and it is shown that a bandwidth of 600 MHz with an input impedance of 10 kΩ can be achieved. The method can be applied to resistors of different sizes. The probe can be integrated on a PCB and used for EMC investigations of power electronics like monitoring switching waveforms of very fast devices (GaN).

2.5.7 My Scientific Contribution

This paper presents a novel PCB-based implementation of a capacitively compensated resistive divider, designed to achieve symmetrical capacitive coupling and minimize measurement distortion. The performance of the design is validated through both equivalent circuit modeling and full-wave electromagnetic simulations, supported by experimental measurements.

My specific contributions to this work include:

- Proposing the implementation method for an optimizable voltage probe in both simulation and measurement
- Conducting the full-wave and circuit-level simulations
- Performing the experimental measurements
- Analyzing and interpreting the results

2.6 PCB Integrated GHz Bandwidth Resistive Voltage and Current Probes for Characterization of Wide Bandgap Semiconductor Devices

M. Gholizadeh, S. Sadeghi, and D. Pommerenke, “A PCB-based high-resistance GHz-bandwidth voltage pick-up for detecting switching voltage,” *IEEE Trans. Instrum. Meas.*, accepted on Jul. 13, 2025.

2.6.1 Abstract

Broadband (GHz) voltage and current sensors are required to measure the transient behavior of gallium nitride (GaN) devices due to their sub-nanosecond switching speed. In the case of asymmetric structures, achieving GHz bandwidth becomes even more challenging, even with traditional circular current probe designs. This paper discusses the advantages and drawbacks of PCB-based resistive voltage and current probes, focusing on the trade-offs between bandwidth and voltage pick-up resistance, as well as those between resistance and bandwidth in resistive current measurements. It also addresses the challenges and solutions for asymmetrical current sensor designs. A capacitively compensated resistive voltage divider (3 GHz/5 kΩ) is proposed, optimized through full-wave simulations and validated with S-parameter measurements. Additionally, a shunt resistor composed of several parallel surface-mount device (SMD) resistors achieves 1.2 GHz/20 mΩ for the symmetric current sensor design and 1 GHz/5 mΩ for the asymmetric design, achieved through parasitic mutual inductance minimization. This paper is an extended version of a work presented at EMC Europe 2023 [59].

2.6.2 Introduction

The sub-nanosecond switching speed of GaN devices allows power electronic converters to operate at multi-megahertz speeds. However, this also presents significant challenges for measuring switching current and voltage, which are very important for evaluating switching performance [58]. A typical example is the design of power modules for electric vehicles with DC link voltages of 400 V or 800 V, and the need to monitor their switching waveforms e.g. in a double pulse test to characterize and reduce electromagnetic emission [47]-[49], [59].

Accurate characterization of wide bandgap (WBG) devices, including GaN and silicon carbide (SiC), demands voltage and current probes that meet stringent bandwidth and electrical performance requirements. According to the established relationship $t_r f_{BW} \approx 0.35$, where t_r and f_{BW} represent rise time and bandwidth, respectively, a measurement bandwidth at least five times greater than the signal bandwidth is required to limit amplitude error to below 2% [63], [66], [93]. This translates to minimum bandwidth requirements of approximately 100 MHz for SiC Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) and at least 500 MHz for GaN High- Electron-Mobility Transistors (HEMTs).

Beyond bandwidth, voltage probes must withstand high voltages, while current probes must minimize both insertion and mutual inductance to avoid altering the circuit's natural switching behavior. Current probes must also accurately capture high-speed signals without introducing measurement artifacts and be compact enough for seamless integration into high-density, PCB-level power module layouts. For resistive current sensing in particular, achieving ultra-low resistance in the milliohm range is critical to minimize power dissipation. Although higher resistance can improve bandwidth, it increases losses and compromises measurement accuracy—highlighting the inherent challenge of achieving both GHz-level bandwidth and low resistance simultaneously [92], [93].

2.6.2.1 Voltage Measurement Challenges

For voltage measurement, resistive voltage dividers (RVDs) are widely used due to their simplicity and high impedance. However, at frequencies exceeding a few MHz, parasitic effects from the resistors and the PCB can introduce a frequency-dependent voltage ratio. Because of the high resistance values, parasitic capacitances tend to dominate over inductances. Parasitic capacitance to ground introduces low-pass behavior, while bridging capacitances between resistor segments introduce high-pass behavior, leading to distortion in the frequency response (Fig. 3.40). Compensation techniques using SMD capacitors or planar PCB electrodes have demonstrated limited bandwidths: 10 MHz at <1 kV [60], 150 MHz at 300 V [50], and 88 MHz at 2.5 kV [51]. Notably, [51] employs a multilayer PCB with a compensation electrode, discrete capacitors, active buffering, and electromagnetic shielding—requiring highly precise layout. Despite these efforts, bandwidth remains insufficient for fast-switching applications. As summarized in Fig. 3.41 and Table 3.5, most RVDs—whether in the literature or commercially available—fail to exceed 100 MHz bandwidth at voltages above 2 kV [62]–[65].

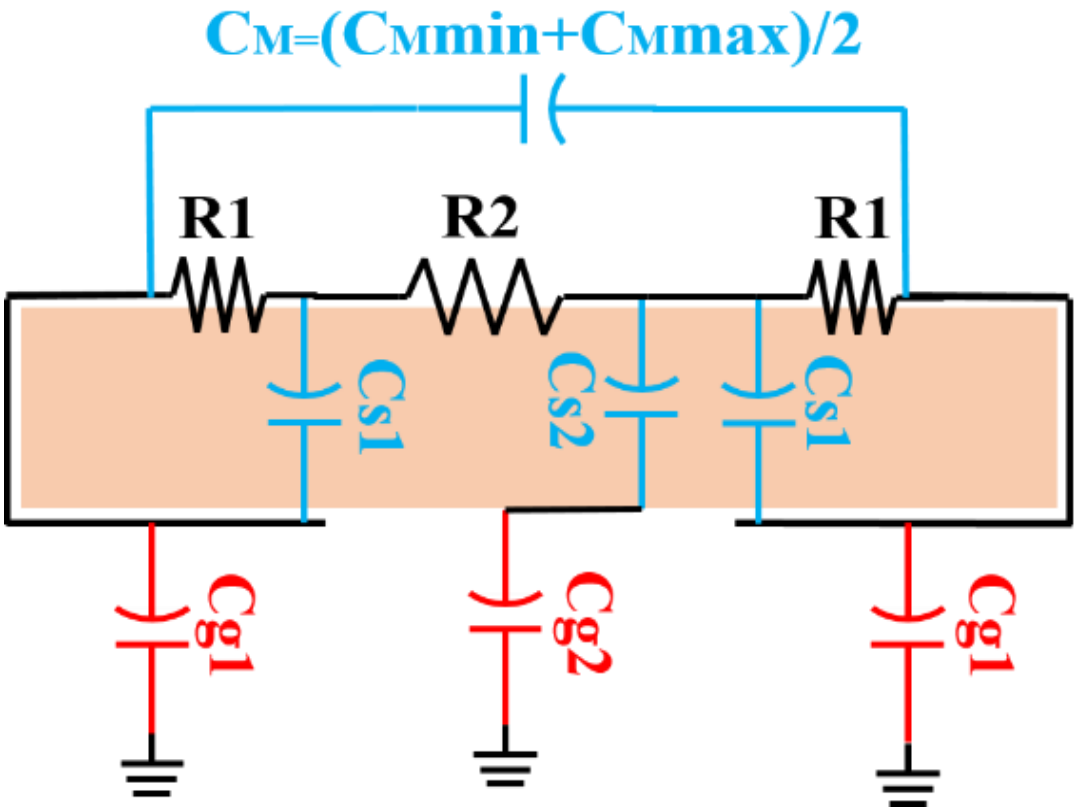


Fig. 3.40: Suggested equivalent circuit of a SMD resistor above GND, taking into account parasitic capacitances. All capacitors are modeled as parallel plate capacitors, described by the formula $C=\varepsilon_0\varepsilon_r A/d$. Further details can be found in [59].

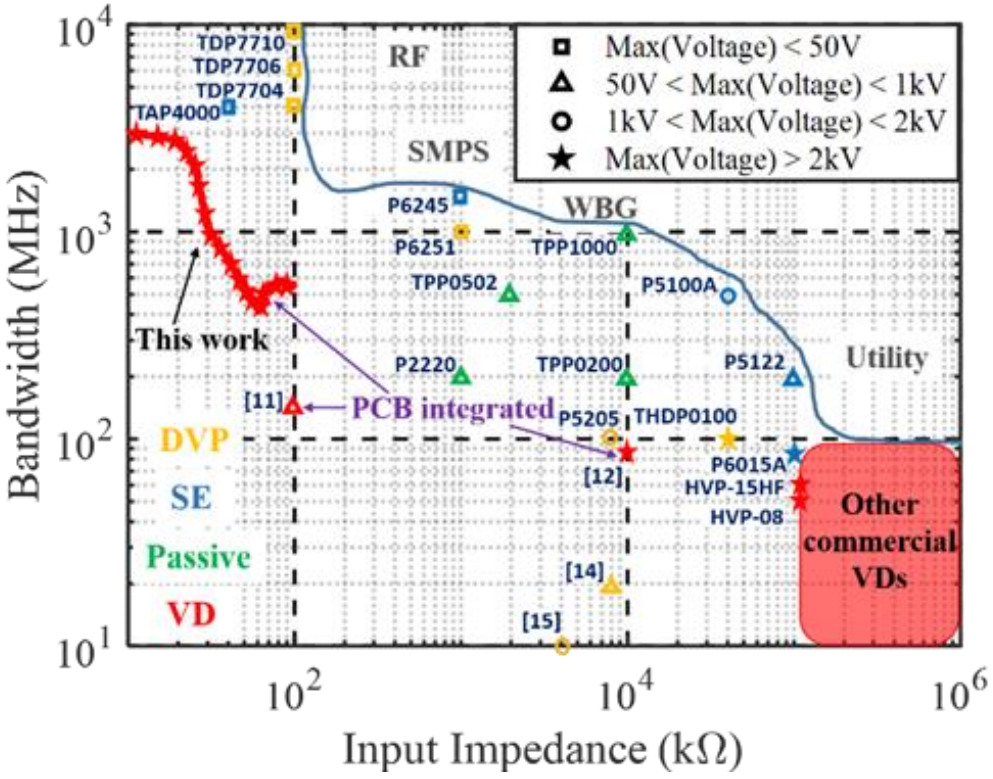


Fig. 3.41: Performance limitations and application trends of commercial and non-commercial voltage probes (differential voltage probe (DVP), single ended (SE), voltage divider (VD)). The commercial probes are identified by their model numbers.

Table 3.5: Comparison of the RVD Sensors in Research.

	Input resistance (kΩ)	Maximum voltage (kV)	BW (MHz)	Integrated in PCB/External probe	Divider type
[60]	---	1	10	Integrated	RC
[61]	100	0.3	150	Integrated	RC
[51]	10000	2.5	88	Integrated	R
This work	1-100 (see Fig. 3.51)	3	4500 - 550	Integrated	R

2.6.2.2 Current Measurement Challenges

Current measurement methods typically fall into two categories: inductive sensors and resistive shunts. Inductive sensors, such as Rogowski coils and current transformers, offer galvanic isolation and straightforward implementation but suffer from poor low-frequency response and often require model-based compensation at the data processing stage [66]–[79]. Resistive shunts, which directly convert current to voltage via Ohm's law, provide high-speed measurement but introduce parasitic inductance that can distort switching behavior (Fig. 3.42). The performance of resistive shunts is often quantified by insertion inductance ($L_i - M$) —the added inductance observed when comparing layouts with and without the shunt—and mutual inductance (M), which quantifies the unwanted coupling from the switching loop into the measurement signal. As resistance decreases, the bandwidth of the shunt degrades due to a mutual inductance–dependent transfer function: $G = \frac{V}{I} = R + j\omega M$, yielding a +20 dB/decade gain slope and the 3 dB bandwidth $f_r = \frac{R}{2\pi M}$.

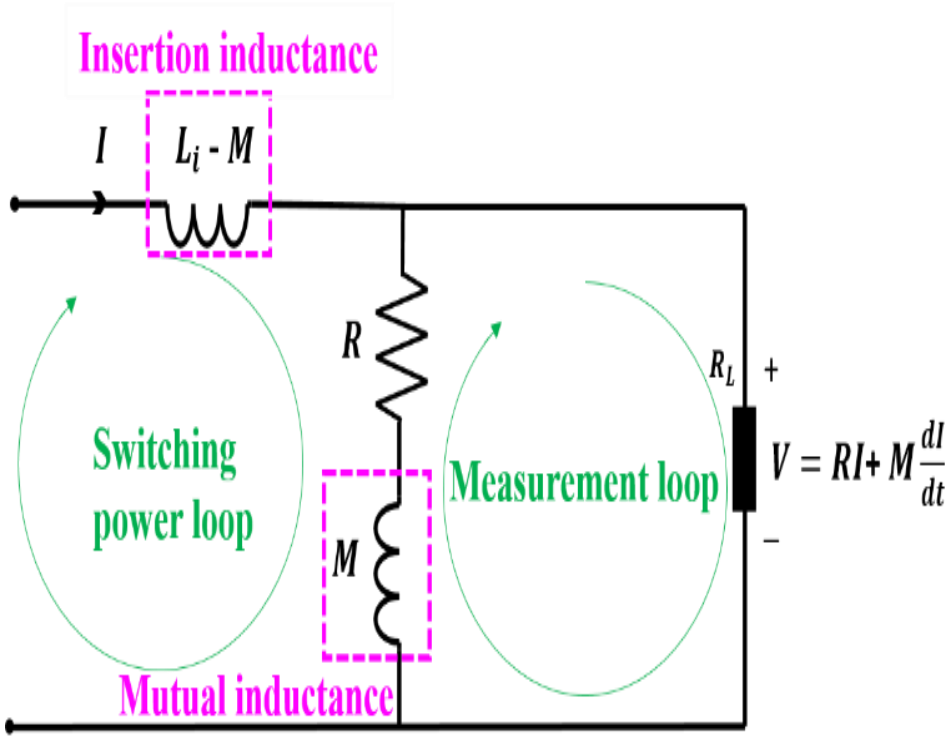


Fig. 3.42: Resistive current sensor equivalent circuit [36].

Resistive shunts exist in coaxial and SMD-based formats. Coaxial shunts can achieve GHz bandwidths but are bulky and unsuitable for integration into PCB-level power modules [80]–[84]. SMD-based shunts—using multiple resistors in parallel and a central sense wire—are more compact but typically limited to <200 MHz at 0.1 Ω resistance [85]–[87]. To overcome these limitations, various strategies have been proposed to mitigate magnetic coupling and reduce mutual inductance, including strategic resistor spacing [88], vertical orientation [89], and flipped placements [90]. While these techniques have achieved >1 GHz bandwidth, they often increase probe resistance or require more PCB area. For instance, [89] reports a circular SMD-based

coaxial structure with vertically mounted resistors, but reducing resistance from 110 mΩ to 10 mΩ results in a bandwidth drop from 2.23 GHz to just 125 MHz. Moreover, integrating circular coaxial geometries—pure or SMD-based—into conventional power modules is difficult due to their large footprint (Fig. 3.43) [92].

Recent approaches have explored RC compensation [91], post-resistor filtering and amplification [92], and impedance-matched transmission lines [93], pushing bandwidths to 3 GHz. However, these designs are often complex, costly to fabricate, and not well-suited for compact or high-density PCB layouts. Fig. 3.44 compares bandwidth and resistance trade-offs among academic and commercial SMD shunt solutions.

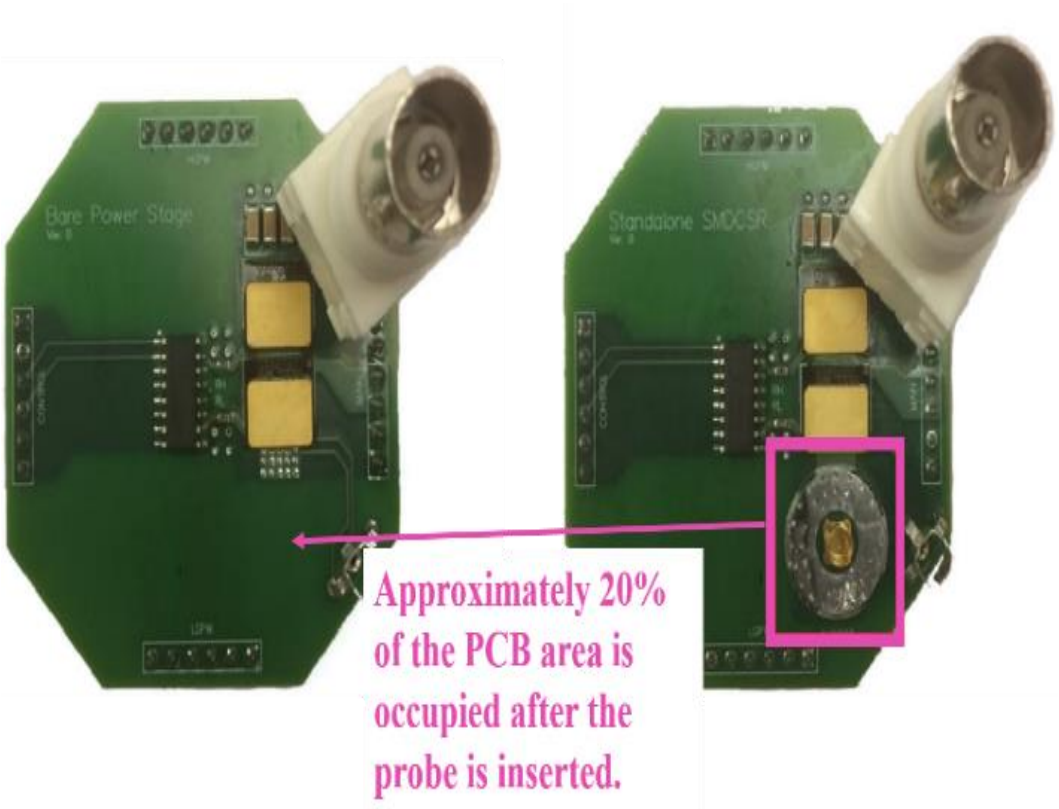


Fig. 3.43: PCB space required for circular coaxial current probe reported in [89].

2.6.2.3 Research Gap

Despite extensive efforts, a technical gap remains between the requirements for WBG device characterization and the capabilities of existing voltage and current sensors. Specifically, no compact, PCB-integrated voltage probe provides GHz-level bandwidth with high-voltage isolation (>2 kV), and no current probe achieves GHz bandwidth at ultra-low resistance (a few mΩs) —particularly under asymmetric current flow conditions common in real-world modules [92].

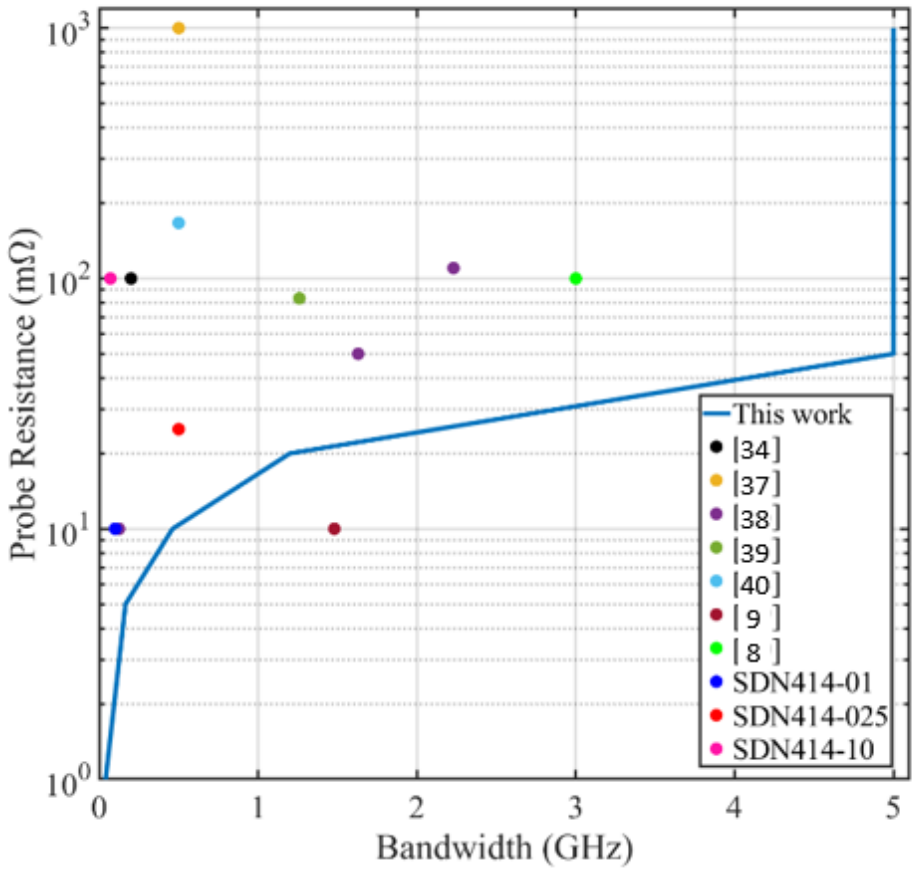


Fig. 3.44: State of the art of the SMD current shunt sensors (for the SDN414 sensors, the measured bandwidth reported in [93] is considered). For "This work", the full-wave simulation results of the symmetric structure shown in Fig. 3.53, which were conducted up to 5 GHz, are used.

2.6.2.4 Paper Contributions

This paper builds on our prior work presented in [59], which introduced full-wave modeling of SMD resistors. Here, we extend that foundation to develop and validate a scalable methodology for both voltage and current probes tailored to the demands of WBG device characterization. The main contributions of this work include:

- Full-wave electromagnetic modeling of SMD resistors
- 3D simulation and parametric optimization using CST Studio Suite
- Equivalent circuit modeling in ADS
- Novel analysis of resistance–bandwidth trade-offs for both voltage and current probes

Our proposed voltage probe achieves a 3 GHz bandwidth at 5 kΩ, surpassing all previously reported

PCB-integrated RVDs, which are typically limited to sub-150 MHz (see Table 3.5). For current sensing, we present a novel rectangular SMD-based shunt capable of supporting both symmetric and asymmetric current paths—the latter addressed for the first time in the literature. By increasing the number of parallel resistors and minimizing mutual inductance, the design achieves 1.2 GHz bandwidth at 20 mΩ and 1 GHz at 5 mΩ, representing a significant advancement over the state of the art. Together, these contributions offer a validated, high-performance solution for non-intrusive, GHz-bandwidth voltage and current measurement—addressing critical unmet needs in high-speed WBG power electronics testing.

2.6.3 Proposed Voltage Sensor

This section summarizes key findings from our previously published conference paper [59], providing an overview of the proposed voltage sensor design. To achieve a flat frequency response for RVDs, it is essential to understand the parasitic coupling between the resistors and the PCB on which they are mounted. In this section, we use an equivalent circuit model and provide analytical formulas to characterize its components to show how selecting appropriate element values can lead to a flat frequency response.

2.6.3.1 The Novel Twist

Using the proposed resistor equivalent circuit (Fig. 3.20), Fig. 3.45 shows the Keysight ADS [56] simulation results of five SMD resistors soldered in series on a microstrip transmission line with the parasitic capacitors. To simplify, all capacitors are considered to be parallel plate capacitors ($C = \mathcal{E}_0 \mathcal{E}_r A/d$) [59]. In this figure, the effect of the capacitors referenced to the trace and those referenced to GND is shown separately. As can be seen, in such structures, the effect of the parasitic capacitors referenced to GND (red curve) dominates over the effect of those referenced to the trace (blue curve). To achieve balance, increasing the effect of the capacitors referenced to the trace is key. One strategy to enhance this impact is to position some resistors directly on the trace, while placing others in sections where the trace is absent, typically on the ground (Fig. 3.46). The introduction of new capacitors ($C_{t1} = \frac{\mathcal{E}_0 \mathcal{E}_{r3}(l_3 w_d)}{h_3}$ and $C_{t2} = \frac{\mathcal{E}_0 \mathcal{E}_{r3}(l_2 w_d)}{h_3}$) between the resistors and the trace can boost the overall capacitance referenced to the trace, resulting in a structure capable of achieving a flat frequency response to a few GHz only by optimizing the gap length under the resistors (l_g).

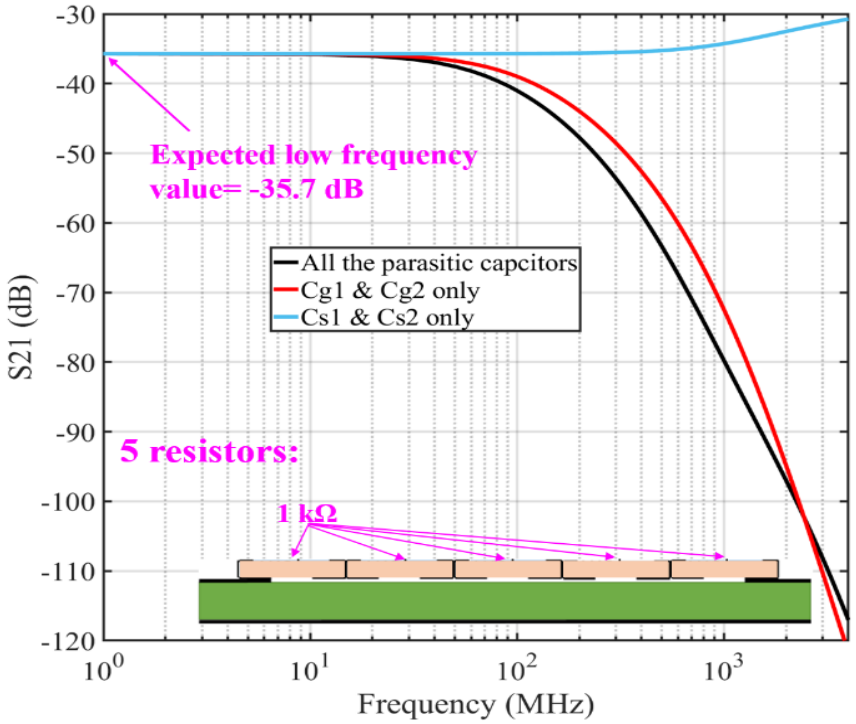


Fig. 3.45: Simulation results of five SMD resistors soldered in series on a microstrip transmission line (simulated in Keysight ADS).

2.6.3.2 Full-wave Model Setup and Verification

The full-wave model of the SMD resistors is shown in Fig. 3.46, using the dimensions specified in the data sheet (thick film 2512) [96]-[97]. The model consists of perfect electric conductor (PEC) elements at the edges, a dielectric layer of Alumina (Alumina $\varepsilon_{r3} = 9.9$), and a sheet lumped element on the dielectric layer connecting the two metallic parts. The CST model of the resistors has been validated with configurations featuring one and two resistors in series at the center of a microstrip transmission line and above GND. Simulated and measured S parameters for this structure are compared in Fig. 3.47. Up to 4 GHz, the proposed full-wave model of the resistor deviates from the measurements by less than 3 dB. Consequently, this 3D model of the resistors is suitable for use in the 3D simulation of the entire voltage pick-up system to optimize l_g.

The cases with just one and two resistors are considered for only model validation by measurements, but in reality more resistors (5 herein) are used for the voltage sensor. The implemented 5 kΩ voltage probe on a PCB is shown in Fig. 3.48. Fig. 3.49 shows the comparison between simulated and measured S21. Tolerating a deviation of ±3 dB from a flat frequency response, the probe works well up to 3 GHz. As can be seen, the full wave simulation of CST Studio Suite follows the measurement with a deviation of less than 1.5 dB. The circuit simulation (ADS simulation) which uses the simple equivalent circuit models of the resistors deviates more than 3 dB above 500 MHz.

The full-wave simulation results illustrating the trade-off between bandwidth and probe resistance are presented in Fig. 3.50 for a series configuration of five resistors. In this analysis, the resistor size, trace layout, and other design parameters were kept constant, with only the resistor values varied to evaluate their impact on bandwidth for a given layout geometry. No additional optimization was performed. The bandwidth, defined as the ±3 dB deviation from a flat response, decreases from 4.5 GHz for a 1 kΩ probe to 0.55 GHz for a 100 kΩ probe.

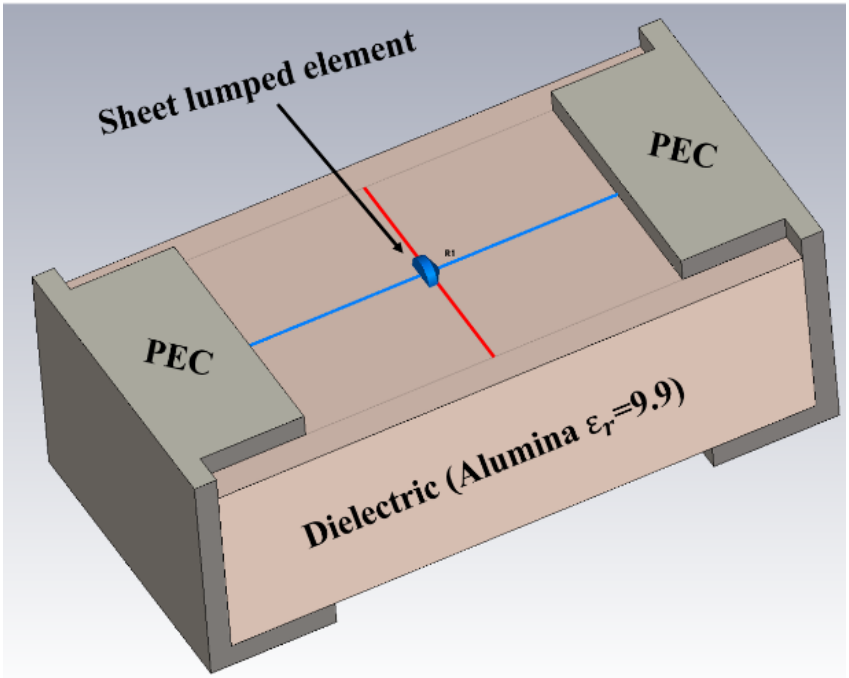
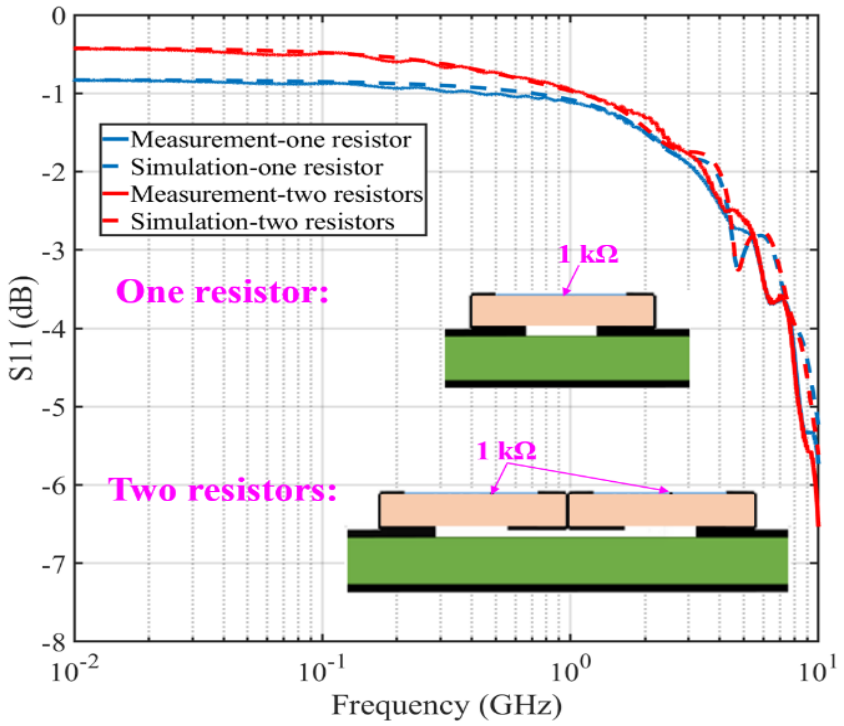
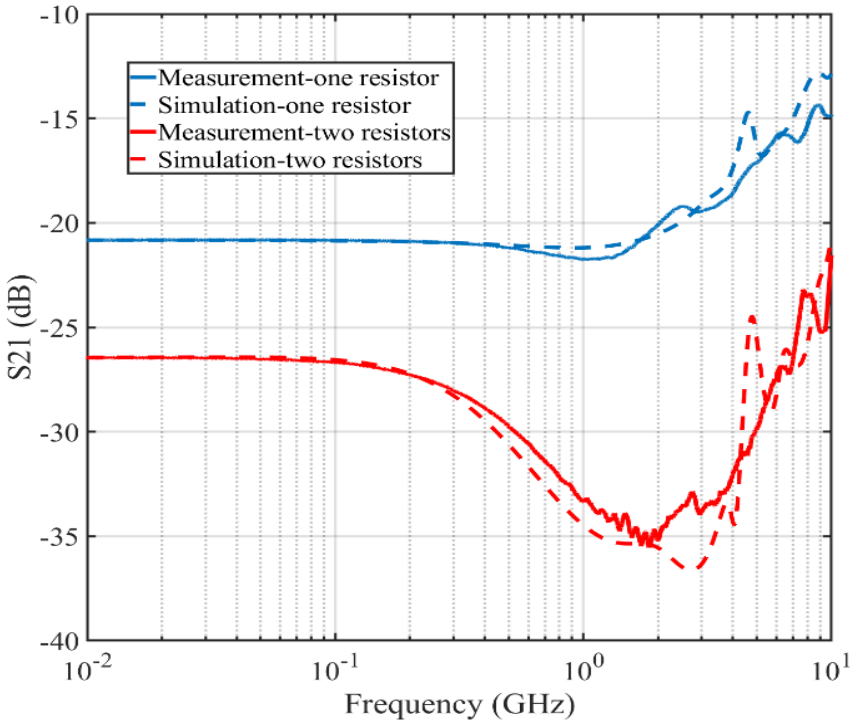


Fig. 3.46: Full wave model of the resistor. The dimensions are extracted from datasheet.



(a)



(b)

Fig. 3.47: Comparison between simulated and measured results of one/two resistors in series placed in the center of a microstrip transmission line and above the GND. (a) S11. (b) S21.

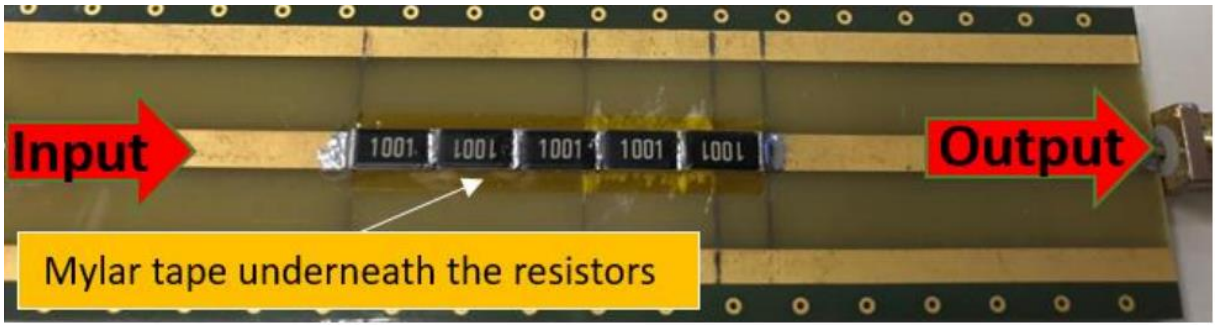


Fig. 3.48: Fabricated high-resistance voltage probe consisting of five 1 kΩ SMD resistors (2512 package) soldered in series on a microstrip transmission line. The design implements capacitive balancing through optimized PCB geometry to achieve a flat frequency response and 3 GHz bandwidth [59].

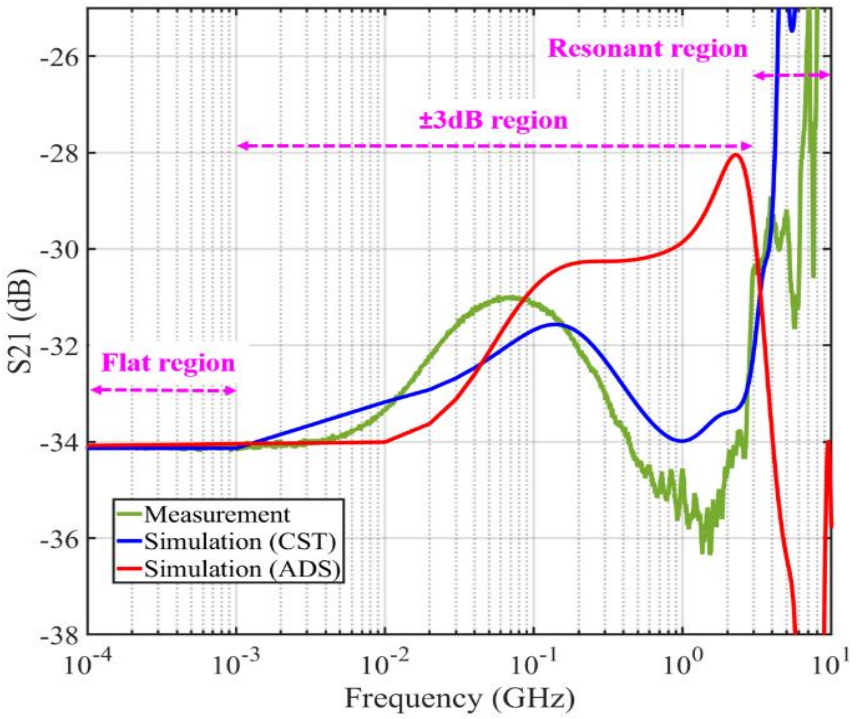


Fig. 3.49: Simulation and measurement of the structure shown in Fig. 3.48 (5 KOhm probe) [59].

Fig. 3.50: Full wave simulation: bandwidth vs. the resistance value of the voltage probe (5 resistors in series).

2.6.4 Proposed Current Sensor

2.6.4.1 Motivation and Concept

The frequency response of a resistive current probe is governed by the transfer function $G = R + j\omega M$, where R is the resistance and M is the mutual inductance between the resistor paths. While mutual inductance can enhance high-frequency signal amplitude, it also introduces phase distortion and limits bandwidth. Reducing R to minimize power dissipation typically worsens this effect by lowering the 3 dB bandwidth $f_r = \frac{R}{2\pi M}$, creating a fundamental trade-off.

A common strategy to achieve high bandwidth is to reduce M through flux cancellation [86]-[89]. In circular SMD current probes, this is accomplished by feeding current symmetrically from the center, as shown in Fig. 3.51. In this ideal scenario, current flows radially outward, and the magnetic fields generated by each resistor path cancel one another, resulting in near-zero mutual inductance ($M \approx 0$) and enabling GHz-level bandwidth with minimal signal distortion.

However, in real-world applications—such as GaN and SiC-based power modules—current typically enters/exits from the one side of the probe, creating an asymmetric feeding condition. This breaks the symmetry required for flux cancellation, leading to non-zero mutual inductance ($M \neq 0$) and significantly limiting bandwidth. Despite its practical relevance, this limitation of circular current probes under asymmetric conditions has not been adequately addressed in the literature. Existing approaches either assume ideal symmetry or increase the resistance to regain bandwidth, at the cost of higher power loss (see

Fig. 3.44).

To address this limitation, we propose a novel rectangular SMD-based resistive shunt optimized for both symmetric (Fig. 3.52) and, in particular, asymmetric current paths (Fig. 3.58). The structure achieves GHz-level bandwidth at ultra-low resistance (a few milliohms) without the need for compensation networks, active circuitry, or complex layouts. Its geometry aligns with typical unidirectional PCB current flow and supports efficient one-dimensional scaling (extending the probe length) to preserve a compact footprint—unlike circular coaxial probes that require two-dimensional expansion to add resistors. This approach not only reduces the probe resistance but also suppresses mutual inductance through several key mechanisms:

- Reduced current per path: More parallel resistors divide the total current, decreasing dI/dt per path and thereby weakening the local magnetic fields that contribute to mutual inductance between the resistor paths.
- Enhanced partial flux cancellation: In both configurations—particularly under asymmetric feeding—adjacent paths with opposing current directions enable partial magnetic field cancellation, significantly reducing net coupling. This effect is not achievable in circular probes under asymmetric conditions.

This combination of low resistance, GHz bandwidth, and compatibility with asymmetric feeding represents a key innovation not previously reported in the literature. The following sections present simulation and experimental validation of the proposed architecture, demonstrating its effectiveness and practical integration potential.

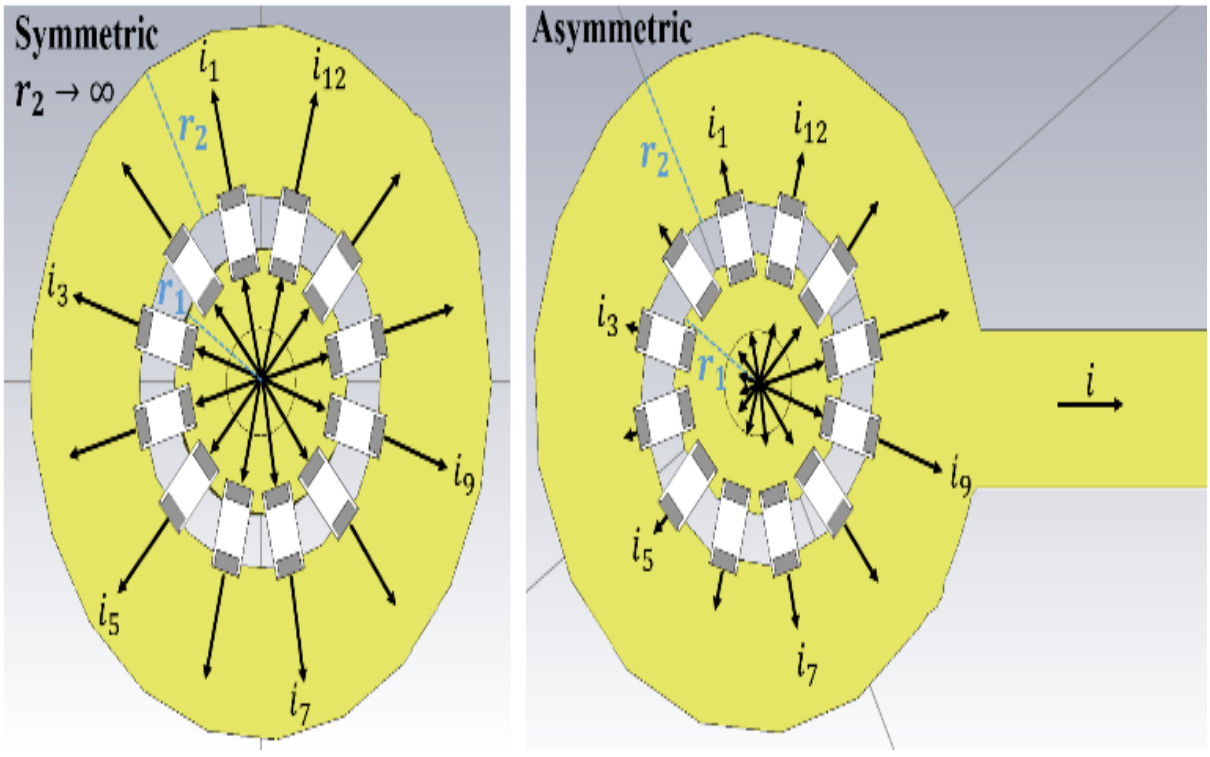


Fig. 3.51: Symmetric and asymmetric feeding in circular SMD shunt. Longer arrows indicate higher currents.

2.6.4.2 Rectangular Probe Design with Symmetric Feeding (the test board)

The Fig. 3.52 presents a 3D design of the proposed rectangular current probe. SMD resistors are arranged in a rectangular configuration within the current's series path. The current flows from the left side trace of the bottom layer (there is an SMA connector (port 1) on the left side to excite the signal), through a central via to the top layer, passing through the resistors before returning to the ground layer (middle layer) via additional vias. A standard SMA connector (port 2) is located at the center to capture the voltage across the sense resistors. The design utilizes the full-wave model of the SMD resistors, as illustrated in Fig. 3.46, based on the dimensions specified in the data sheet for thick film 0402 resistors [98]. Key design variables include the number of resistors in parallel (*N*), which effectively determines the length of the current probe (l_{probe}), as well as the resistance value of each resistor. To illustrate this, several variations were simulated using CST Studio Suite and S21 is analyzed. For a 20 mΩ probe, we explored seven configurations involving 12 or 24 resistors, four of which are presented in Fig. 3.53:

- 12 resistors with zero distance (there is no gap between the resistors, *d=0*).
- 24 resistors with zero distance (Fig. 3.53(a)- *d=0*).
- 12 resistors stacked-6 resistors placed directly on top of another 6, *d=0*.
- 24 resistors stacked-12 resistors placed on top of another 12 (Fig. 3.53(d), *d=0*).
- 12 resistors arranged on the side (Fig. 3.53(c), *d=0*).
- 12 resistors spaced apart to occupy a larger area (Fig. 3.53(b), *d=0.6 mm*).
- 24 resistors oriented upside down (the resistive layer faces the bottom side, *d=0*).

The simulation results are displayed in Fig. 3.54. It is evident that an increased l_{probe} leads to a higher bandwidth, with configurations using 24 resistors achieving a bandwidth of 600 MHz, while those with 12 resistors attain 100 MHz. The bandwidth increases from 100 MHz to 160 MHz when the 12 resistors are spaced 0.6 mm apart, compared to when the distance is 0 mm, as the effective l_{probe} is slightly larger than $l_{1+}l_2 + \cdots + l_6$. When the 24 resistors with zero distance are oriented upside down, the bandwidth improves further to 1.2 GHz.

To evaluate the bandwidth as a function of probe resistance, 36 resistors are considered, and only their resistance values are varied to assess the trade-off between resistance and bandwidth for a given layout geometry. As shown in Fig. 3.55, the 3 dB bandwidth decreases from 5 GHz with a 50 mΩ probe to 0.041 GHz with a 1 mΩ probe. For probe resistances above 50 mΩ, a bandwidth exceeding 5 GHz is achievable (simulations were conducted up to 5 GHz).

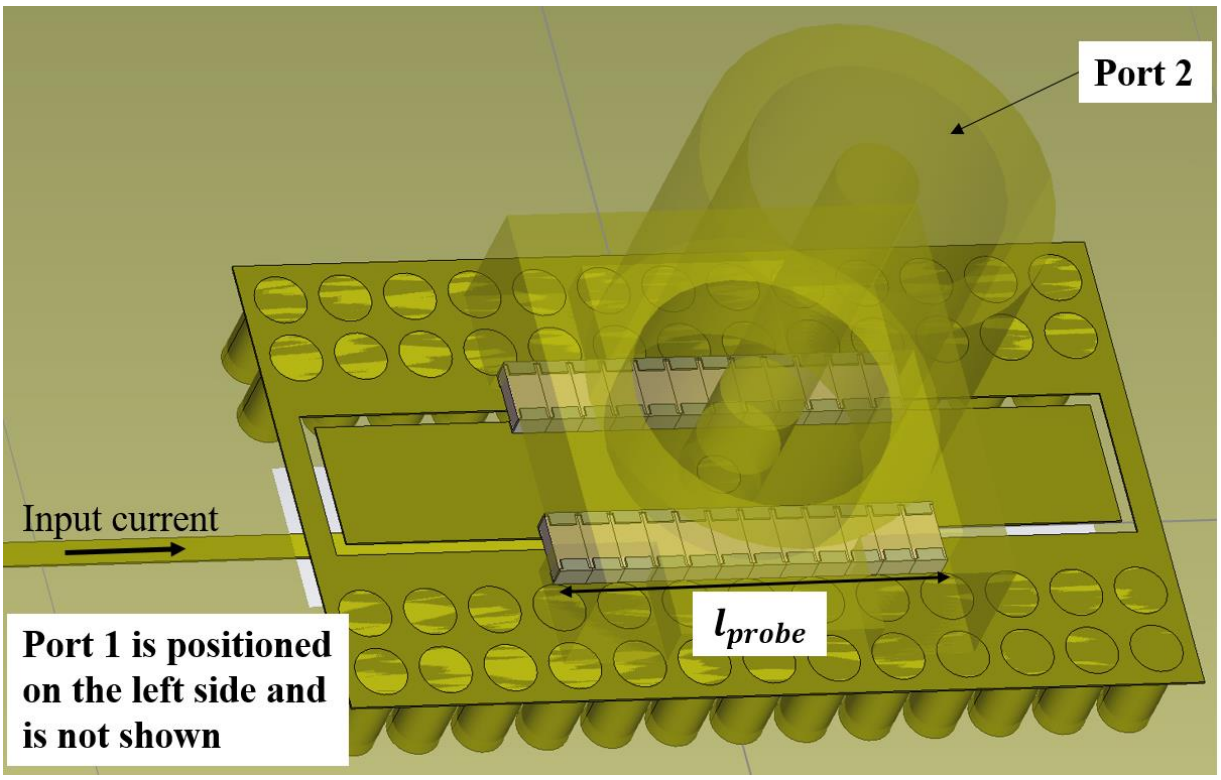


Fig. 3.52: Proposed rectangular structure for the current probe: introducing extra asymmetry by increasing the length of the current probe l_{probe}.

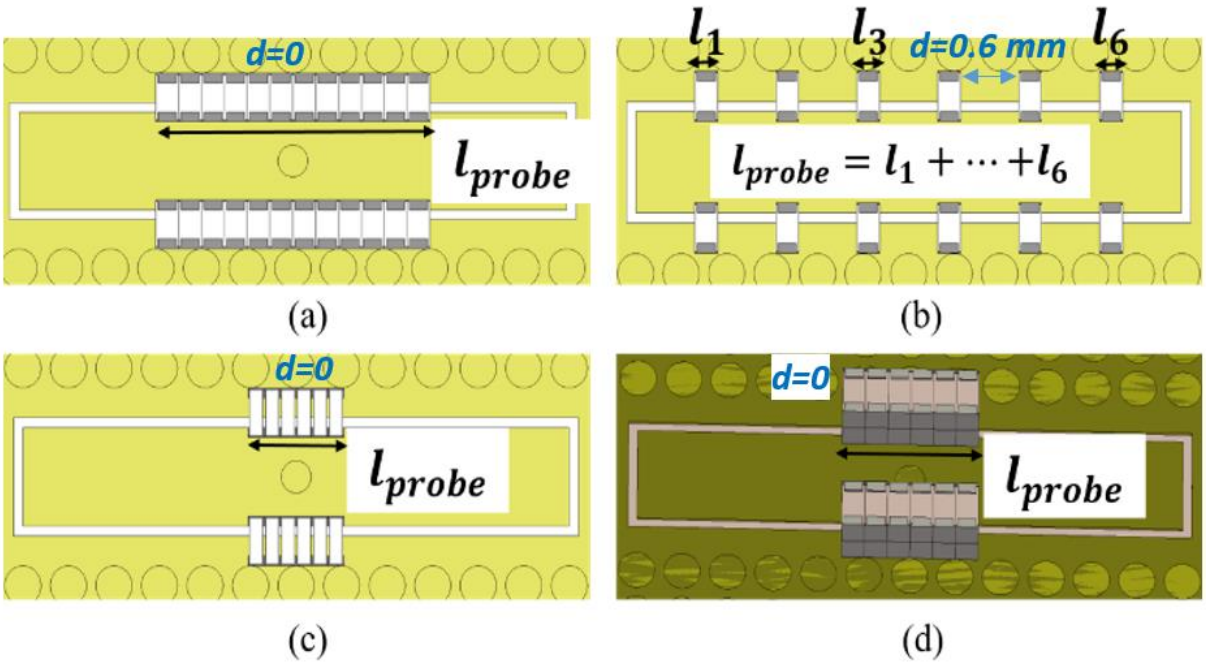


Fig. 3.53: 20 mΩ probe. (a) 24 resistors. (b) 12 resistors (16). (c) 12 resistors (located on the side). (d) 24 resistors (12 on top of 12).

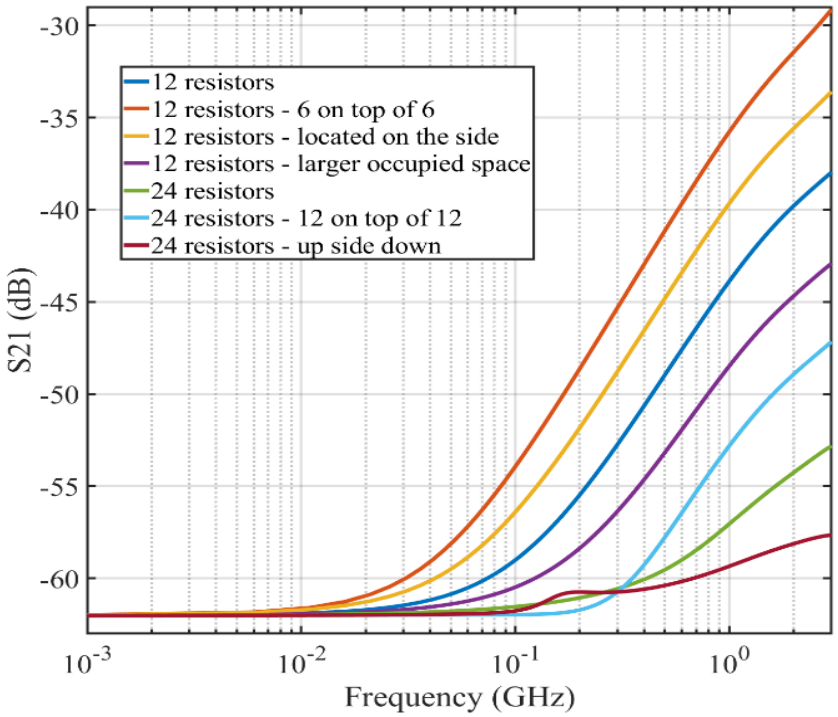


Fig. 3.54: Simulated results for a 20 mΩ probe, showcasing various configurations with 12 or 24 resistors.

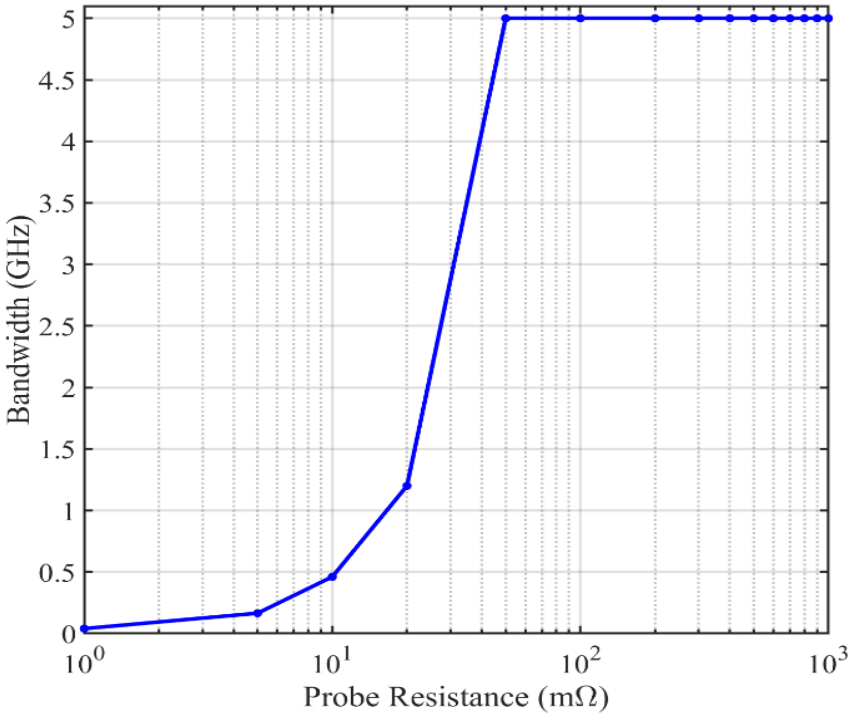


Fig. 3.55: Full wave simulation: bandwidth vs. the resistance value of the current probe (structure shown in Fig. 3.52)

2.6.4.3 Proposed Equivalent Circuit for Rectangular Probe Design with Symmetric Feeding (the test board)

Fig. 3.56 shows the equivalent circuit for the rectangular 20 mΩ probe (12 × 240 mΩ) depicted in Fig. 3.52.

To estimate the inductances, a commonly used rule of thumb is that the path length between two points, measured in millimeters, roughly corresponds to an inductance value ranging from 0.2 nH to 1 nH. In this case, we consider 0.2 nH/mm. For example, on the test board, the path length of the input current (referred to as the main current in the power loop) that can couple into the measurement loop (on the resistor side) is given by the sum of $(d_{i1} + d_{i2})$ (in mm), as shown in Fig. 3.56. This trace section couples with the thick trace carrying the resistors within the measurement loop. However, this coupling can be minimized by reducing the rectangular gap in the ground layer. The corresponding inductance, L_i, is thus $0.2 \times (d_{i1} + d_{i2})$ (in nH). The value of L_i in our structure is 1.14 nH. It is clear that resistors with the same path length in the rectangular configuration exhibit identical L_m (L_{m1}=L_{m6}=L_{m7}= L_{m12}=0.8 nH, L_{m2}=L_{m5}=L_{m8}= L_{m11}=1.12 nH and L_{m3}=L_{m4}=L_{m9}= L_{m10}=1.33 nH).

Within the measurement loop (on the thick trace), a series inductance L_m is assigned to each resistor, with the mutual inductance between them and the power loop (L_i) represented as $M_{1j} = n\sqrt{L_i L_{mj}}$, where $j = 1, \dots, 12$. To simplify the circuit, it is assumed that the coupling coefficient n is the same for all paths. The coupling between resistor paths within the measurement loop is represented by $N_{s,t} = k_{s,t}\sqrt{L_{ms} L_{mt}}$, where $s = 1, \dots, 12$ and $t = 1, \dots, 12$. A first-order estimation of this coupling coefficient is as follows:

- We know that the magnetic field around an infinitely long straight wire has an inverse relationship to the radial distance, given by $H = {\mu_0 I}/{2\pi r}$. Hence, the largest value should be assigned to adjacent resistors, such as between R_1 and R_2 $(k_{1,2})$, …, R_{11} and R_{12} $(k_{11,12})$. In this case, we consider $k_{1,2} = \cdots = k_{11,12} = 0.6$ which physically makes sense for two paths coupling at a distance of $d = 0.5\,mm$ (the distance between the centers of two adjacent resistors).
- Then, we distribute the remaining coupling coefficients based on the coupling distance. For instance, the distance between the centers of R1 and R2 is d, while the distance between R1 and R3 is 2d, so $k_{1,2} = 2 \times k_{1,3}$. Moreover, based on this assumption, $n = 0.1k_{1,2}$ is obtained.

In this structure, some of the coupling between the resistor paths will be canceled by others due to symmetry, causing the corresponding coupling coefficients, k_{st}, to be negative. For example, $k_{1,2} = -k_{2,3} = k_{3,4} = \cdots = -k_{10,11} = k_{11,12}$. A similar approach can be applied to the circular configuration probe design. In the circular probe, it is assumed that all coupling between the resistors' paths cancels out due to symmetry, and only the coupling between the measurement loop and the power loop is considered, with $n = 0.1k_{12}$ and L_m=0.8 nH and L_i=1.14 nH.

Fig. 3.57 shows a comparison between ADS circuit simulations and CST results for circular and rectangular probes with 12 and 24 resistors, demonstrating good agreement.

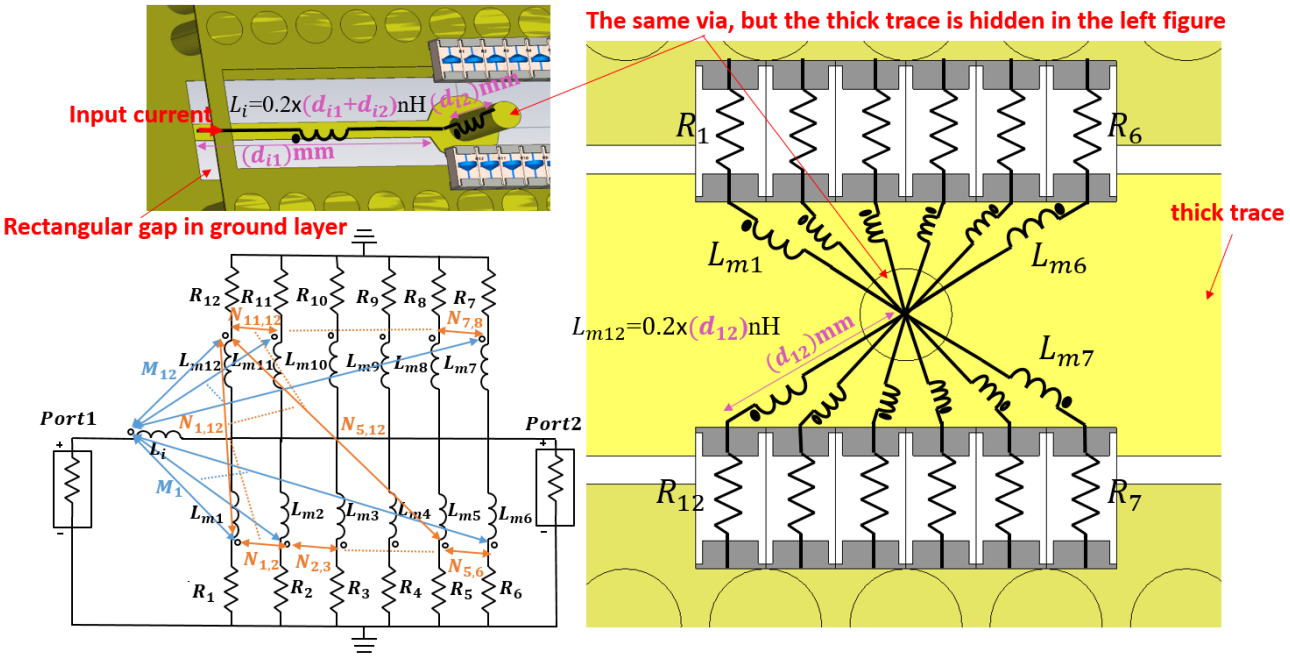


Fig. 3.56: Equivalent circuit of the proposed current probe.

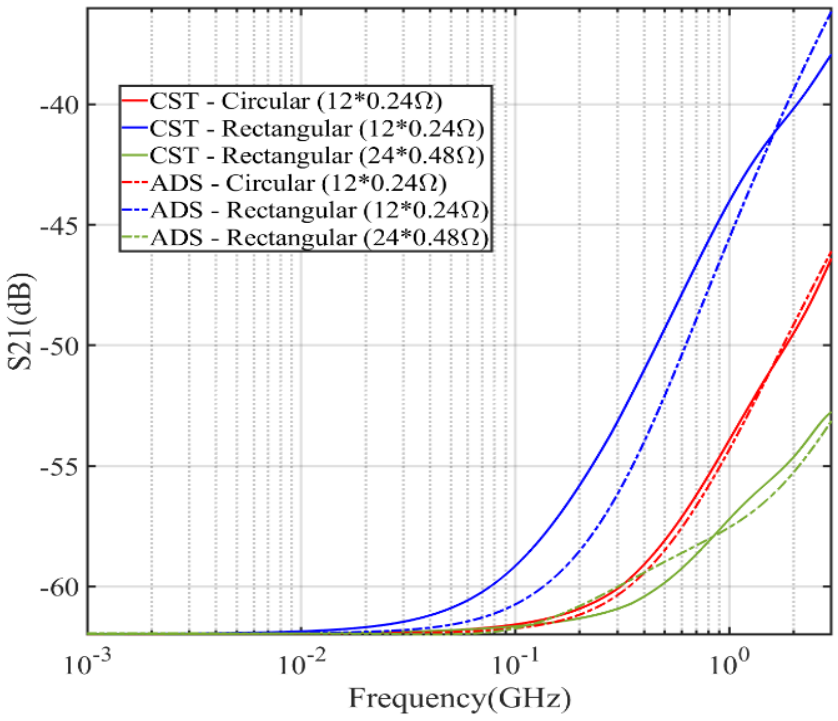


Fig. 3.57: Equivalent circuit (ADS) and full wave (CST) simulation results for the structures shown in Fig. 3.52 (20 mΩ probe).

2.6.4.4 Rectangular Probe Design with Asymmetric Feeding

Fig. 3.58 illustrates the proposed rectangular current probe, which is fed asymmetrically. The length of the arrows indicates the relative current flowing through each resistor, with shorter electrical lengths corresponding to higher current levels. To simulate and analyze the performance of the rectangular probe in this asymmetric configuration, the ODB++ file of a PCB designed for a half-bridge (HB) circuit ([41]) is imported into CST Studio Suite, as shown in Fig. 3.59.

In the 3D model, to evaluate the frequency response of the current probe, all components except for the high-side FET (HS-FET) and the high-side current sensor (HS-CS) are removed. For simplification, the low-side FET (LS-FET) and the low-side current sensor (LS-CS) in the main loop are shorted. The current path created for this simulation (representing the main loop of the HB circuit) is indicated by the black arrows. The current is introduced via a discrete port (port 1) placed between the drain and source of the HS-FET. It flows through the vias, passing the shorted LS-CS, LS-FET, and DC-link capacitor, before entering the HS-CS. After passing through the sense resistors, it returns via the central vias to the HS-FET drain. A standard SMA connector is positioned at the center of the HS-CS to capture the voltage across the sense resistors, with a discrete port located at the SMA connector (port 2). The circuit diagram of the main loop of the HB circuit is also presented on the right side of Fig. 3.59.

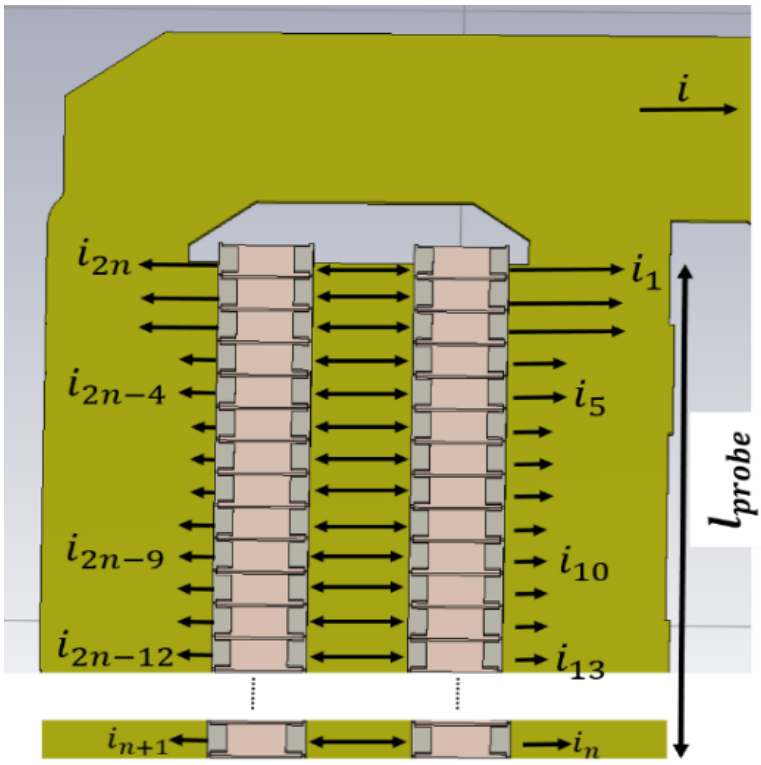


Fig. 3.58: Proposed rectangular structure for the current probe: introducing extra asymmetry by increasing the number of the resistors in parallel. Longer arrows indicate higher currents.

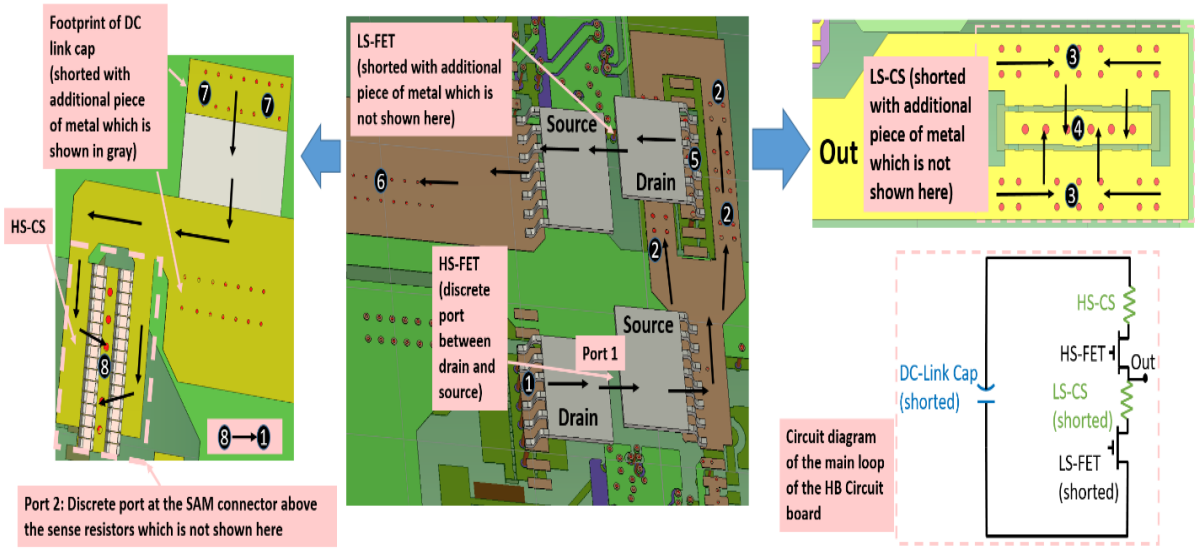


Fig. 3.59: ODB++ file of the HB PCB imported into CST. Black arrows only show the current path.

Fig. 3.60 displays the simulated S21 for the HS-CS. As indicated, the number of resistors (l_{probe}) increases from 12 to 32 to achieve a GHz bandwidth with a minimal probe resistance. A lower probe resistance necessitates an increase in the number of resistors to maintain a GHz bandwidth. Specifically, using 32 resistors in parallel can achieve a 5 mΩ probe with a bandwidth of 1 GHz, while with only 12 resistors, the probe resistance is limited to 100 mΩ with a bandwidth of 1.015 GHz.

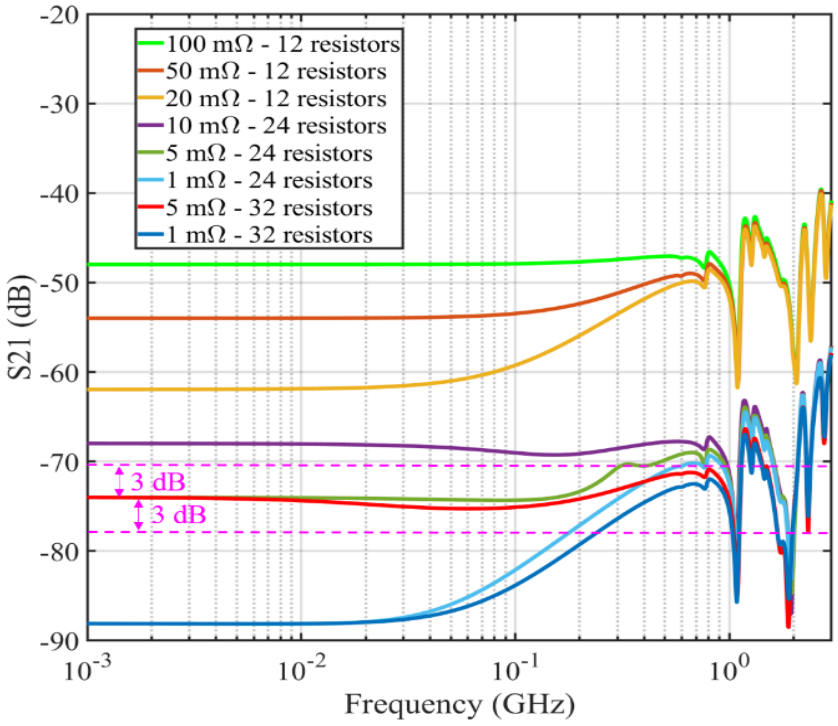
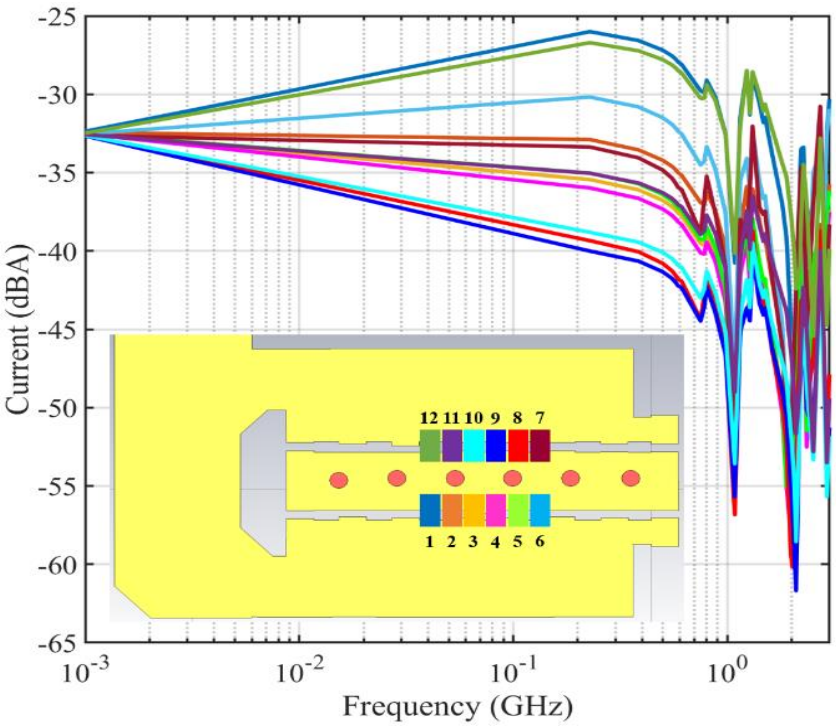


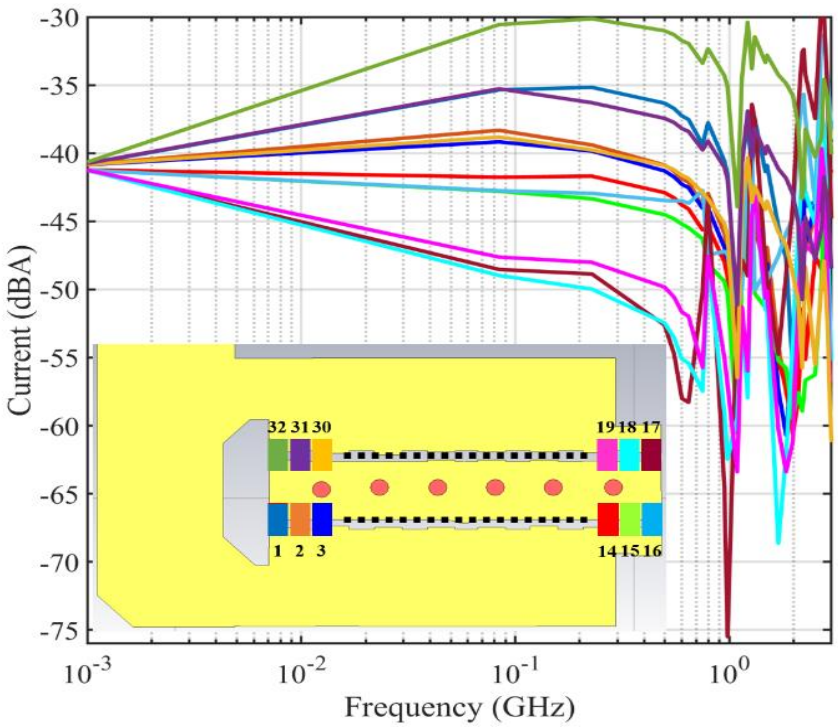
Fig. 3.60: Simulated S21 for HS-CS (structure shown in Fig. 3.59).

Fig. 3.61 demonstrates how the current distribution through the sense resistors changes as the number of resistors (l_{probe}) increases from 12 to 32. It is important to note that:

- Resistors with shorter electrical lengths in the current path carry more current.
- There is an increase in current through the resistors located at the corners of the structure, as high-frequency currents tend to flow more through these corner resistors.



(a)

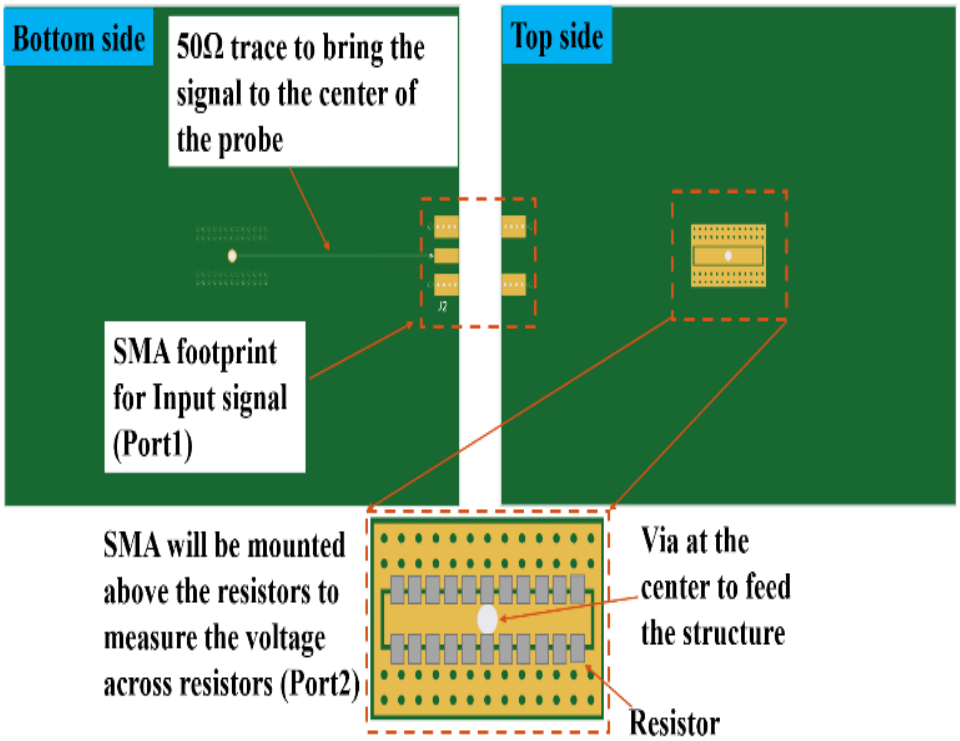


(b)

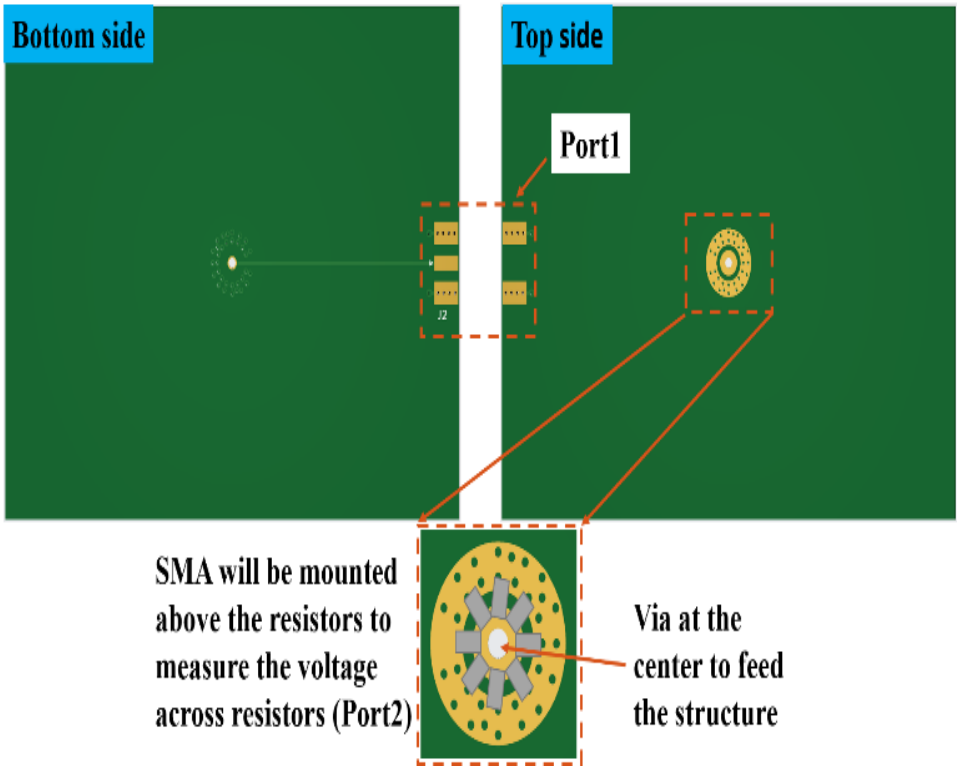
Fig. 3.61: current through the sense resistors (lumped elements in the full wave simulation) for the structure shown in Fig. 3.59. (a) 12 resistors. (b) 32 resistors.

2.6.4.5 Experimental results and analysis

Measuring the frequency response of the probe (HS-CS) directly on the HB board is challenging due to common mode currents on the SMA connector located above the sense resistors (as the shield of the SMA connector is not referenced to ground). Hence, the setup depicted in Fig. 3.52 is utilized for measurements. Based on this configuration, PCBs are designed to implement both conventional circular probes and the proposed rectangular probes, allowing for the measurement of their frequency responses (see Fig. 3.62).



(a)



(b)

Fig. 3.62: PCB layout used for characterization. (a) Proposed rectangular probe. (b) Conventional circular probe.

Fig. 3.63 shows full-wave simulated and measured S21 for a 20 mΩ probe resistance. Both results demonstrate that while a circular SMD arrangement achieves GHz bandwidth at higher resistances (e.g., 100 mΩ), it fails at lower resistances like 20 mΩ. In contrast, our rectangular design maintains GHz bandwidth (1.2 GHz at 20 mΩ for 36 resistors in parallel) by introducing additional asymmetry, which reduces mutual inductance (M) and results in a flatter frequency response across the GHz range.

As an example, a line with a +20 dB/decade slope is shown for the rectangular probe with 12 resistors, and the corresponding uncompensated mutual inductance is also calculated. Notably, the uncompensated mutual inductance decreases from 44 pH for 12 resistors to 7 pH for 36 resistors in the proposed rectangular probes.

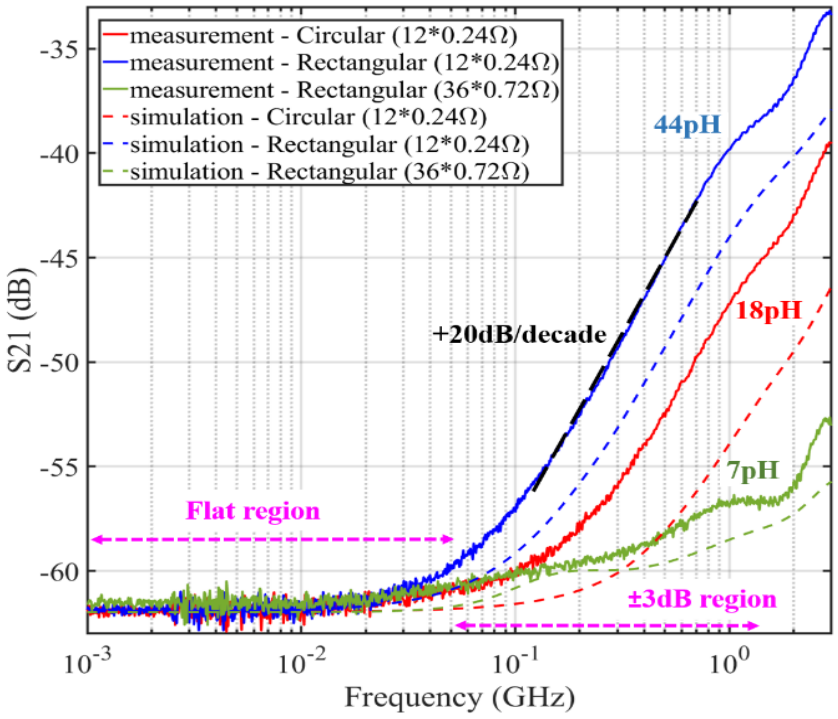


Fig. 3.63: Simulated and measured results for the structures shown in Fig. 3.62 (20 mΩ probe).

2.6.4.6 Limits

The design process for resistive current and voltage probes is outlined using 0402 and 2512 SMD resistors, respectively; however, this approach can be adapted to resistors of various package sizes. The ability to increase the voltage handling of the voltage probe and the current handling of the current probe is constrained by the power, voltage, and current ratings, as well as the thermal capacity of each individual resistor. For example, the resistors used in the design of the voltage probe have a maximum operating voltage of 300 V [97]. Considering a pulse with a 50 percent duty cycle, the maximum voltage handling of the implemented 5 kΩ probe (shown in Fig. 3.48) is $V(\mathrm{Max}) = 300 \times 2 \times 5 = 3\ \mathrm{k\Omega}$.

Additionally, the available space for arranging sufficient resistors in series for the voltage probe or in parallel for the current probe imposes constraints on these parameters. Naturally, a larger occupied

space will increase the insertion inductance of the probes. For the current probe, the frequency response—especially at low resistance values—can be improved as long as there is enough space to incorporate more resistors in parallel. The trade-off between resistance and bandwidth for a given layout geometry, for both the voltage and current probes, has been discussed, with the results shown in Fig. 3.50 and Fig. 3.55, respectively.

2.6.5 Conclusion

This paper presents a novel PCB-based GHz bandwidth resistive voltage and current probes. The voltage probe balances parasitic capacitances, which arise from the resistors to the high-voltage trace and from the resistors to ground. Based on full-wave simulations and utilizing SMD resistors, a 5 kΩ voltage probe with a 3 dB bandwidth of 3 GHz is realized. The investigation into the trade-off between bandwidth and probe resistance shows designs achieving 4.5 GHz bandwidth at 1 kΩ and 0.55 GHz at 100 kΩ for the same resistor configuration.

Additionally, we propose a shunt resistor made of parallel SMD resistors with increased bandwidth and a rectangular shape, optimized similarly to the voltage divider. Full-wave simulations and measurements show that while a circular SMD resistor arrangement achieves GHz bandwidth at higher resistances (e.g., 100 mΩ), it fails at lower resistances (e.g., 20 mΩ). Our rectangular design maintains GHz bandwidth by introducing asymmetry (1.2 GHz/20 mΩ). A trade-off analysis shows the 3 dB bandwidth decreases from 5 GHz at 50 mΩ to 0.041 GHz at 1 mΩ, with bandwidths over 5 GHz achievable for resistances above 50 mΩ. Full-wave simulations of asymmetric feeding yielded a 1 GHz bandwidth for a 5 mΩ probe with 32 SMD resistors.

2.6.6 My Scientific Contribution

This paper analyzes the trade-offs involved in PCB-based resistive voltage and current probes, particularly the relationship between bandwidth and resistance. It specifically addresses the challenges in asymmetrical current sensor designs. A capacitively compensated voltage divider with GHz-level bandwidth is proposed, optimized through full-wave simulations and validated using S-parameter measurements. Additionally, a high-bandwidth current shunt—constructed from parallel SMD resistors—is presented, achieving GHz performance through minimized parasitic mutual inductance.

My specific contributions to this work include:

- Proposing an implementation method for an optimizable voltage probe in both simulation and measurement

- Designing the structure of the GHz-bandwidth current probe with minimized parasitic mutual inductance
- Designing and fabricating the test PCBs for current probe evaluation
- Proposing the equivalent circuit model for the current probe
- Conducting simulations, experimental measurements, data analysis and interpreting the result

2.7 ESD Susceptibility Analysis: Coupling to Traces and Interconnect

M. Gholizadeh, S. M. Mousavi, D. Pommerenke, A. Pak, G. Fellner, and J. Min, "ESD susceptibility analysis: Coupling to traces and interconnect," in *Proc. 2021 IEEE Int. Joint EMC/SI/PI and EMC Europe Symp.*, Jul. 26, 2021, pp. 1018–1023.

2.7.1 Abstract

ESD susceptibility scanning is an effective method for finding the causes of ESD soft failures in electronic systems. A local probe is used to scan the system for sensitive areas. However, the voltages induced by the probe are often unknown. This paper quantifies the induced voltages from different probes when injecting into traces and flex cables and compares the values to the induced voltages caused by an IEC 61000-4-2 ESD gun in the contact mode. The goal is to guide the reader in selecting the voltage levels and probes during susceptibility scanning in a way that they relate to ESD gun injection and avoid levels that are likely to cause hard failure.

2.7.2 Introduction

ESD susceptibility scanning is a powerful method to investigate the root cause of ESD soft-failures in electronic systems [99]. It is described as a standard practice by the ESDA Association [100]. It can be applied to compare different designs, e.g., a manufacturer has changed the IC process or the package, or to troubleshoot systems which fail to pass ESD testing, such as IEC 61000-4-2. To identify sensitive ICs and modules, electric and/or magnetic field probes are excited by strong pulse sources, e.g., 2 kV, using a 500 ps rise time TLP. The probes are moved along potentially sensitive structures, e.g., above a PCB, along flex cables, to identify which structure leads to soft failures. This type of soft failure is compared to the soft failure observed during IEC 61000-4-2 testing to determine which local structure is sensitive and probably causing a soft failure in IEC 61000-4-2 testing.

A core difficulty is not knowing how large the induced voltage is. Partial treatment of this question is given in [101-104], however, it does not relate to the interconnect. The voltages induced in the traces or other interconnect depend on a set of parameters such as the probe geometry, the distance of the probe to the structure, the geometry of the structure and the pulse amplitude and rise time. The user can select all, but the geometry of the structure. The probe influences the coupling [105-109]. The local geometry is often only known by inspection from the top of a PCB. While an exact knowledge of the coupling can only be determined by full wave simulation or measurement of the specific structure, a general guidance can be obtained by measurement and simulations on similar structures.

Inducing a voltage of less than 100 mV is unlikely to even cause a bit error, while inducing voltages of 100 V or more is likely to damage, either directly or by causing a latch-up. The induced voltages are proportional to the TLP voltage if the rise-time does not change with voltage. The range mentioned above is large. An approximate knowledge of the induced voltages is sufficient to select a start value for the TLP settings that, allows to induce significant voltage, without taking the risk of causing damage.

Experimentally, this paper investigates the correlation between TLP settings (pre charge voltage) and the desired level of TLP induced signals in traces and flex cables. The goal is to give guidance to the user of the susceptibility scanning in the selection of the appropriate TLP settings. A set of typical probes has been used for testing.

2.7.3 Methods and Structures investigated

2.7.3.1 Probes

The EMC laboratories own a variety of probes that are mainly used for EMI measurements. Some of them are intended for hand scanning and some of them can be attached to scanning systems. As these are near field probes. Thus, one can distinguish between electric- and magnetic field probes. All probes also partially couple to other field components. This is especially strong in non-shielded magnetic field probes. For ESD voltage coupling, the shield is often omitted which allows the movement of the current carrying part of the probe closer to the DUT and thus increase the coupling.

Furthermore, the orientation of the field is relevant. If Z is defined as the axis along the probe's body, then, most of the EMI probes are H_x oriented (or H_y if they are rotated by 90 degree) and the most of the E-field probes, such as an open coax [105] are E_z oriented. In addition, a horizontal loop will create a field that is H_z oriented while a symmetric structure that has the characteristics of a dipole (e.g., two small patches on the left and the right side of a PCB) and driven differential will create an E_x field. Again, rotation of the probe leads to an E_y field. The paper concentrates on the more common probes, some are shown in Fig. 3.64.

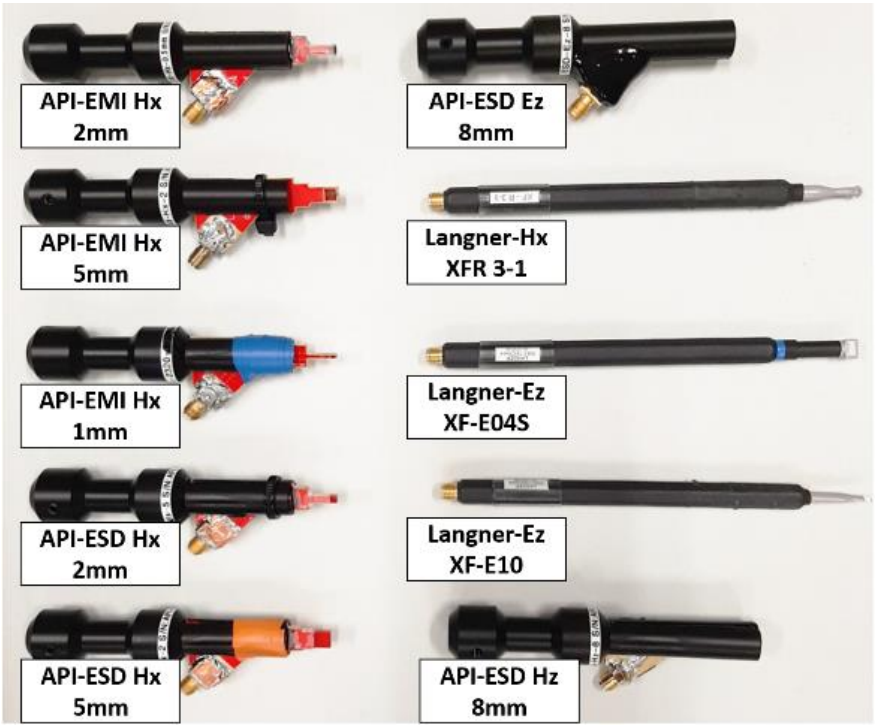


Fig. 3.64: Probes used in this investigation (http://www.amberpi.com).

2.7.3.2 PCBs

As test objects, flex cable connected boards (different pitch and connectors) and traces have been selected. They are shown in Fig. 3.65, Fig. 3.71 and Fig. 3.74.

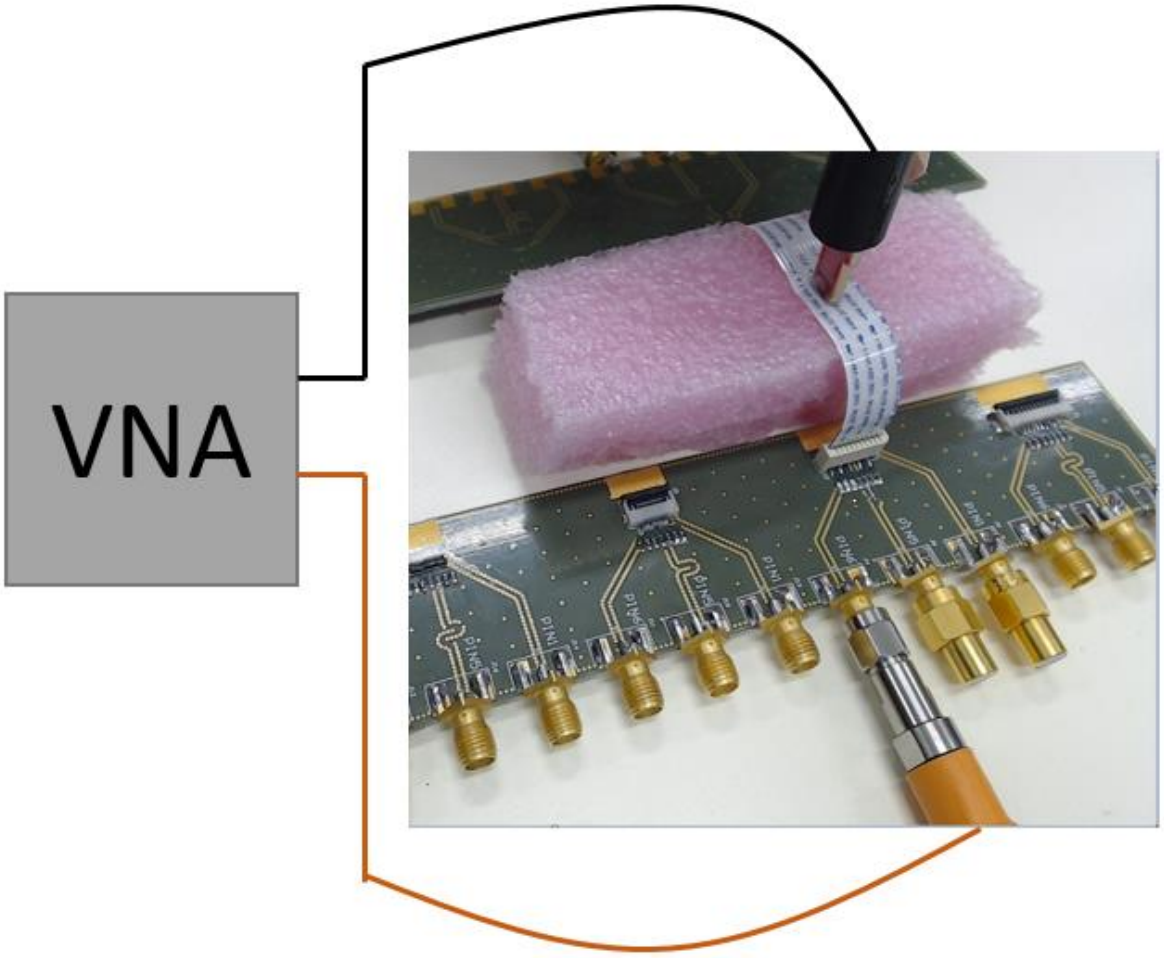


Fig. 3.65: Setup used to couple to a flex cable. The probe is at the location of the maximal coupling amplitude.

2.7.3.3 Test Methods

The goal is to determine the coupling of probes to different flex cables. This is to guide the user of an ESD scanning system. The user needs to estimate the induced voltages as a function of probe, distance, TLP voltage etc. The data gives the estimations of the induced voltages if the probes are used to induce voltage into the flex cables and traces. Knowing the approximately induced voltage helps in setting the TLP voltage range to one where soft failures are likely, but damaging effects are not likely. Thus, after a probe is selected and the actual PCB or flex cables are inspected, a good range of TLP voltage settings can be estimated.

2.7.3.4 Frequency Domain

The frequency domain measurements are performed using a VNA (Vector Network Analyzer). As most of the spectral energy of ESD is confined to less than 2 GHz and the rise time of the TLP used for pulse creation was about 500 ps, we limited the frequency range to 2 GHz. The setup for coupling to a flex cable is shown in Fig. 3.65. In this setup, three traces on the board 2 (pin 1,5 and 6) and two traces on the board 1 (pin 5 and 6) are terminated in 50 Ω and port 1 of the VNA is connected to the pin 1 from the input side. The rest of the traces (7 traces) are shorted to GND on both sides using 0 Ohm resistors (detailed information of the PCBs is shown in Fig. 3.74). While the magnitude of the coupled signal varies strongly from probe to probe, all show similar features.

The frequency response, Fig. 3.66, follows a 20 dB/dec slope as expected from a first order coupling response. Above about 100 MHz, the curve flattens. This is a result of the low pass filtering which is caused by the inductance of the flex cable trace and the 100 Ω terminations (50+50 Ω). A complex behavior with many resonances is visible above 200 MHz. This includes board-to-board resonances and resonances of GND connected flex cable traces. Only full wave simulation would be able to relate the details of the physical structure to each resonance.

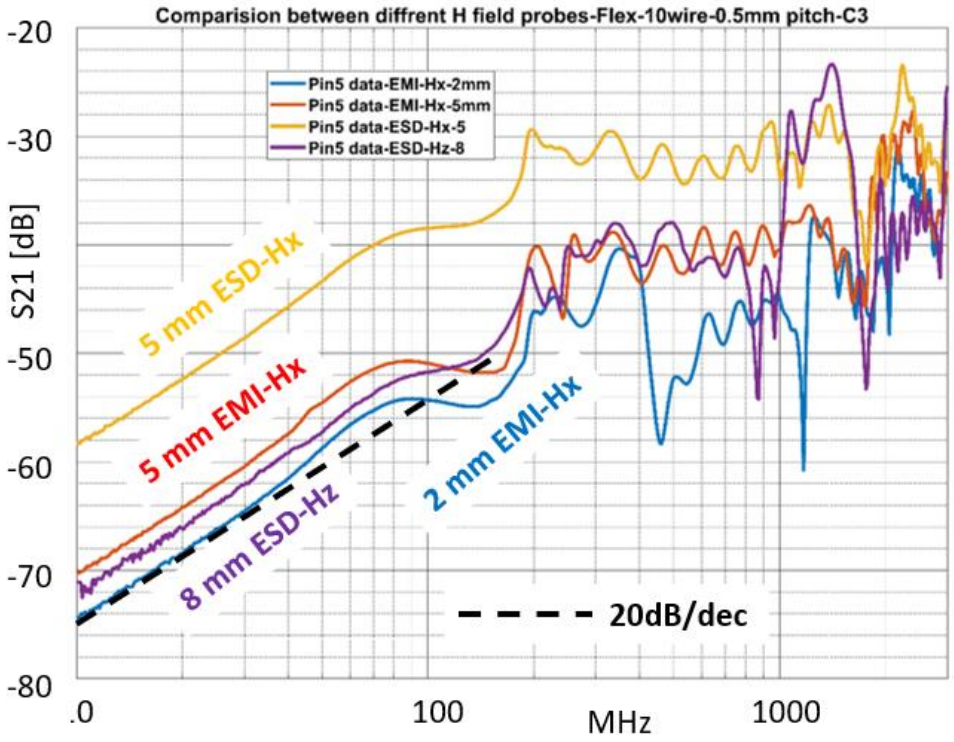


Fig. 3.66: S21 obtained from measurements of the coupling of probes to a flex cable having 1 mm pitch. The trace coupled to is terminated with 50 Ω on the both ends (the detailed information of the two PCBs are shown in Fig. 3.74).

2.7.3.5 Time Domain

E-field and H-field probes couple differently to a trace. Depending on the probe selected, the TLP will inject a current or couple a voltage into a trace which is close to the probe. If it is an H-field probe, the probe will cause a voltage along the trace. It is induced by the magnetic field of the probe which couples into the loop area between the trace and its GND. An E-field probe will inject a current into the trace by the capacitive coupling from the probe to the trace. The difference is well visible in Fig. 3.67.

To obtain this data, we placed probes on a microstrip trace and measured the voltage induced by connecting both ends of the microstrip to the two channels of the oscilloscope.

The E-field probe's current injection leads to the same polarity on both channels, while inducing a voltage along the microstrip (for the length of the microstrip that is underneath the probe) leads to pulses of opposite polarity on the scope.

A horizontal loop (unshielded Hz-probe) shows a more complex behavior. If the loop is centered above the trace, the magnetic field coupling at the left and right of the trace is canceling each other, however, some E-field coupling remains. If the probe is moved to a position that its current carrying wire of the probe is above the microstrip, then, its magnetic field coupling will be dominant as illustrated in Fig. 3.68.

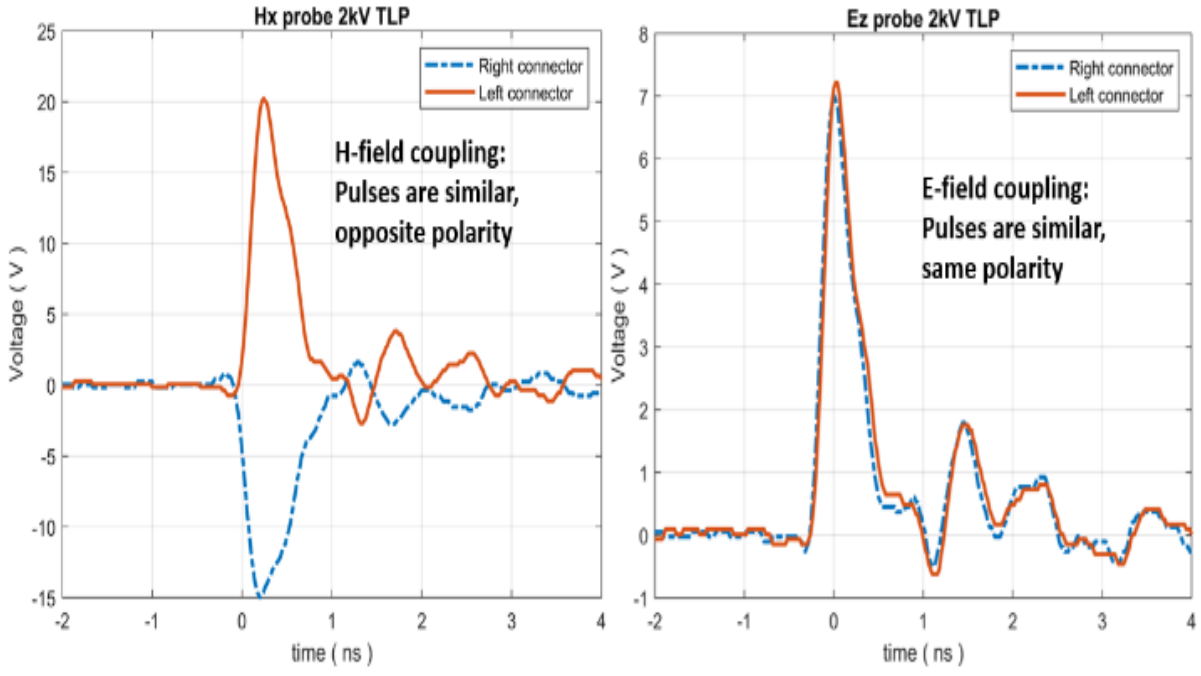


Fig. 3.67: S21 obtained from measurement of the coupling of probes to a flex cable having 1 mm pitch. The trace coupled to is terminated with 50 Ω on both sides.

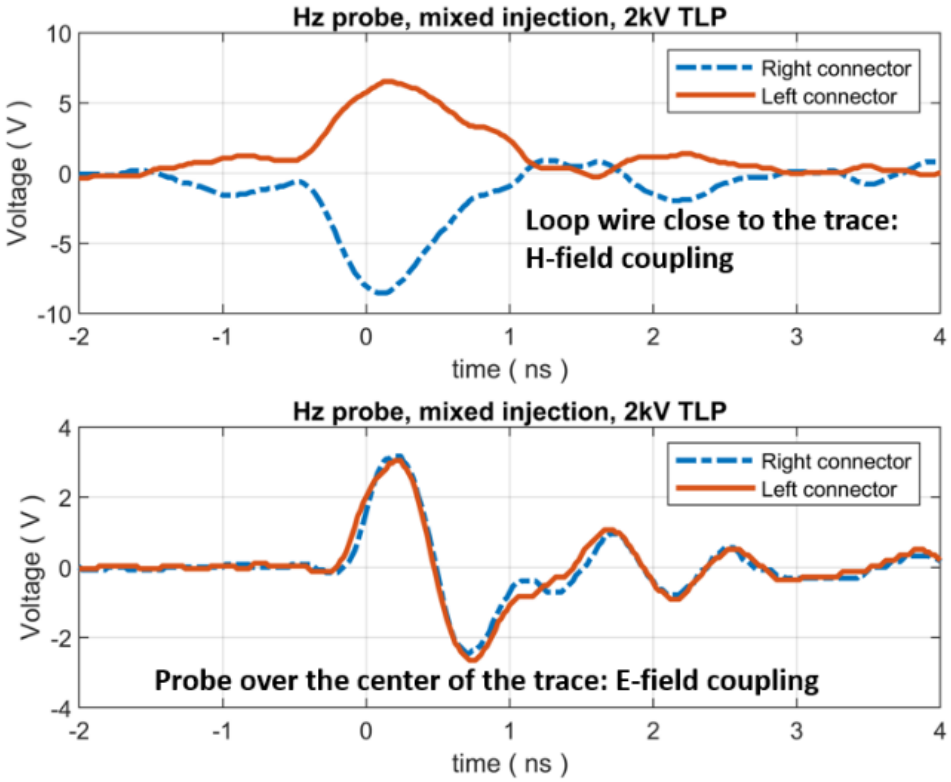


Fig. 3.68: Coupling of an unshielded horizontal loop of 8 mm to a microstrip for two positions.

2.7.4 Results

If the goal is to recreate the soft failures observed during a system level IEC test by local scanning, it is important to estimate the voltage induced by a certain TLP voltage setting and the selected probe. As the peak voltage depends on the di/dt or dv/dt at the probe, the rise time of the TLP is important. The TLP selected shows a rise time of about 500 ps. It is realized using an SF6/N2 relay as switch. The relay is the same as the ones used in most ESD generators.

The reaction of the DUT depends on the voltage. If we roughly assume that the voltages less than 0.1 V will lead to no soft-failures and the voltages more than 100 V may carry the risk of latch-up or damage, then, a lower and upper bound is given. To facilitate the coupling, the probes have been held against different microstrip traces. The width of the microstrip trace and its distance to the ground plane was varied to consider different layout situations. The voltage is expressed as “TLP charge voltage setting to achieve 1 V induced voltage”.

The data shown in Fig. 3.69 indicate that TLP voltages from 20 V to 170 V will induce 1 V in the microstrip traces. Indicated by “A” we see a general tendency: It is easier to couple to the 90 Ω trace relative to the 42 Ω trace. Less TLP voltage is needed for the same induced voltage of 1 V. The reason lies in the layout. For the 90 Ω trace, layer 2, the normal GND of this 4-layer board is removed. Thus, the return path is about 1.4 mm below the trace. The 76 Ω trace has the same return plane as the 42 Ω trace, but its width is more narrow. This increases the TLP voltage needed for coupling 1 V, indicated by “B” comparing the red and the blue bars.

The effect of using a shielded probe, designed for EMI vs. using a probe that has no shielding to allow closer coupling to a trace, is indicated by “C”. It compares the two probes of the same size, 5 mm, one with a shield (EMI) and the other without a shield (ESD). The needed TLP voltage approximately doubles. If the TLP can be charged to 5 kV (often limited by the connectors used) then the first and the last probe, Fig. 3.69, will induce about 250 V. This value has a rather high chance to cause damage (e.g. gate oxide damage).

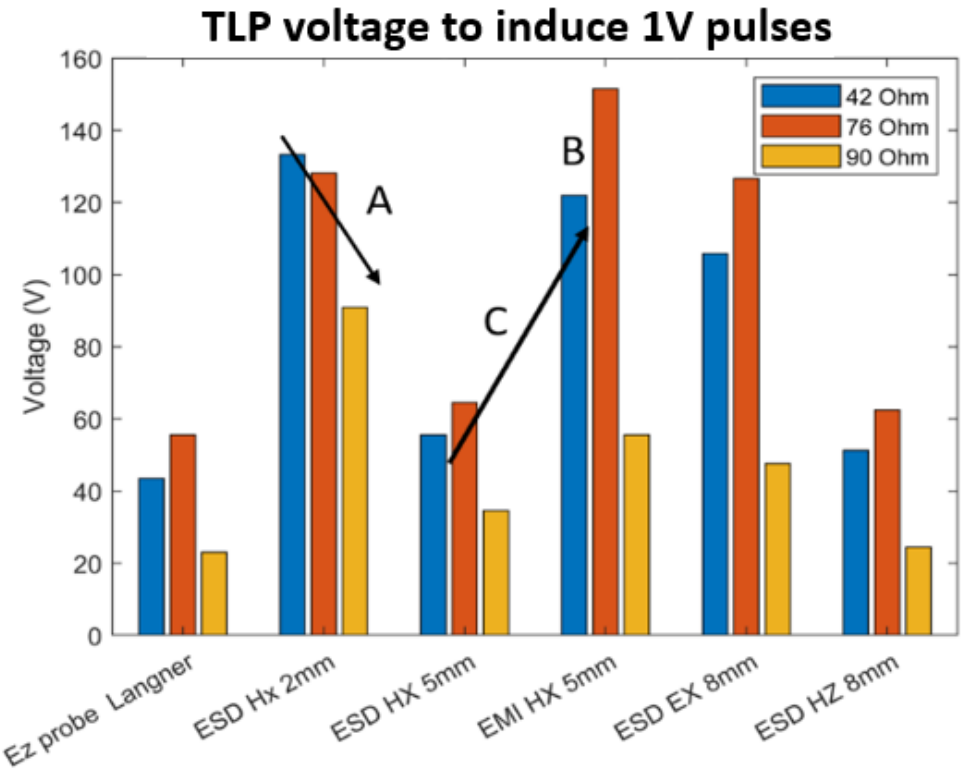


Fig. 3.69: TLP charge voltage for achieving 1 V of induced voltage for different traces and probes.

2.7.4.1 Effect of Flex Pitch

To create the data shown in Fig. 3.70, different flex cables have been mounted between the boards. The probes are held against the flex at the position of maximal coupling and the peak induced voltage is measured. It is normalized to the TLP voltage. By this normalization, we express the TLP voltage that is needed to achieve 1 V of induced voltage. Due to reciprocity, there is no difference between injecting into the probe and measuring at the trace or injecting into the trace and measuring at the probe. In this setup, three traces on the board 2 (pin 1,5 and 6) and two traces on the board 1 (pin 1 and 6) are terminated in 50 Ω and the output of the TLP is connected to the pin 5 from board 1. The rest of the traces (7 traces) are shorted to GND on both sides using 0 Ω resistors (detailed information of the PCBs is shown in Fig. 3.74). The output of the different probes is connected to the oscilloscope. Two pitches are used: 0.5 mm and 1 mm.

The larger 5 mm probe (indicated by “A”) designed for maximal coupling (no shield) needs less than 50 V TLP charge voltage to couple 1 V into the 1 mm pitch flex cable. Comparing the 0.5 mm

to the 1 mm pitch (“B”), we see stronger coupling to the wider pitch flex. This is a result of using other traces of the flex as return path. Thus, the loop area, needed for coupling, is reduced if the pitch is tight.

Often, no test setup is available to determine the coupling into a flex cable. However, microstrip traces are available in most labs. How predictive is the coupling into a microstrip towards coupling into a flex? Indicated by “C” a relative good match can be seen. In general, the 1 mm pitch flex coupled 25% less than the 50 Ω microstrip while the 0.5 mm pitch flex coupled similar to the microstrip. Thus, the microstrip is a good predictor for other none-shielded flex cables.

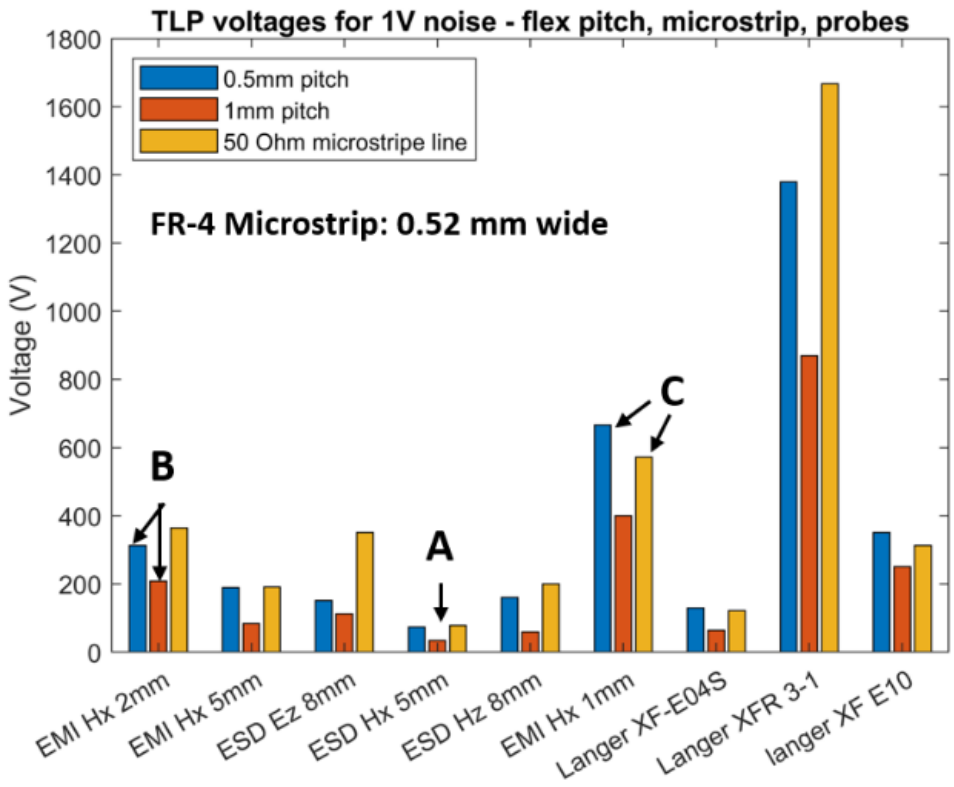


Fig. 3.70: Coupling of different probes to flex cables compared to coupling to a 50 Ω microstrip line.

2.7.4.2 Shielding the Flex Cable

From an EMC point of view, flex cables form weak points in board-to-board connections. Their field confinement is low. Thus, they may excite board-to-board modes for EMI and allow ESD current, injected into one of the connected boards, to couple and create a voltage between the PCB GND and a trace.

The Flex cables are often shielded to improve field confinement. This reduces EMI and ESD coupling. However, the shield is often not connected, or only connected on one side. How good is this? In this experiment, the ESD gun is discharged at 1 kV contact mode into the not grounded board, while the other board is connected to a large ground plane. Two traces on the flex connection, one at the edge and one in the middle are connected to the oscilloscope, Fig. 3.71.

As shown in Fig. 3.72, the trace at the edge of the flex will couple stronger. This is a consequence of the partial shielding of the center trace by its neighboring traces.

Here, all, except three traces are connected to the ground on both sides (detailed information of the two PCBs is shown in Fig. 3.74).

Just adding a copper tape as a "shield" directly onto the flex, but not connecting it to PCB ground, reduces the voltages, especially for the edge pin. Adding a GND to the shield connection, but only on the one side did not reduce the coupling, it even increased the coupling for the center pin. Using a one sided shield on the flex, but grounding it on both PCBs reduced the coupling by about 8x relative to the unshielded case. Moving to a both sided shield with best connection, reduced the coupling further to about 20x below the value of the unshielded case. The data indicates that the adding a "shield" to a flex, but not grounding it (this is often done as bandage), is reducing the coupling, however, far less is achieved compared to the both-sided ground connection.

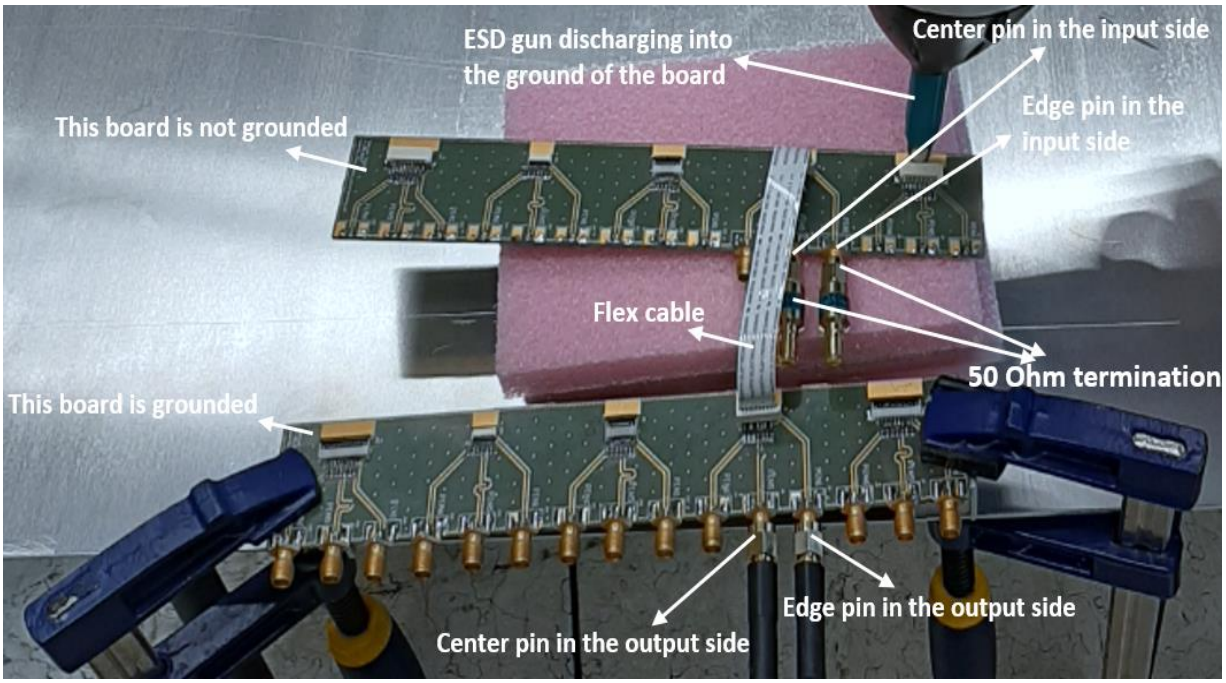


Fig. 3.71: Test setup for board-to-board coupling of an ESD pulse for a flex cable connection.

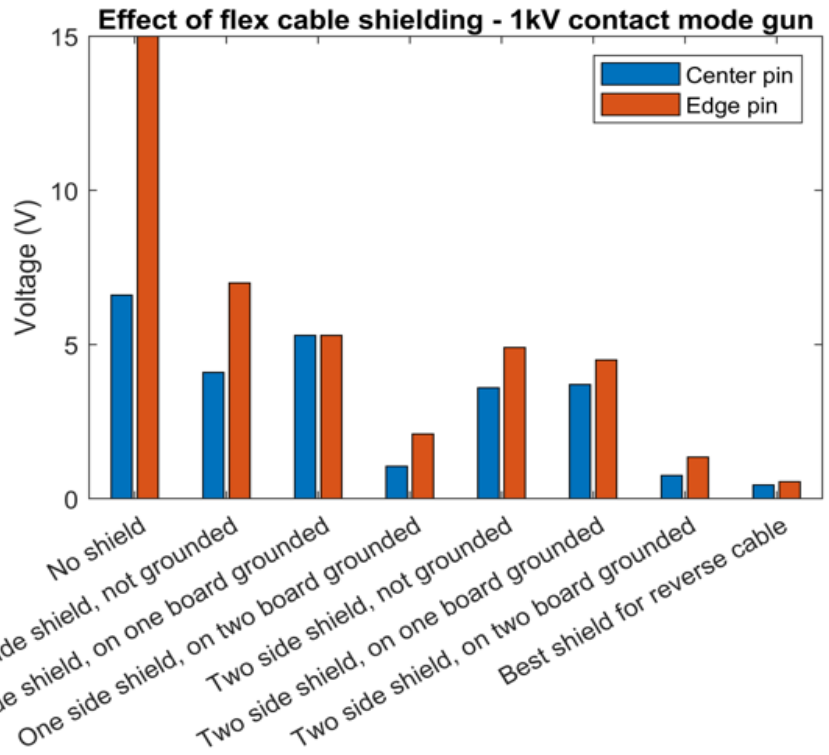


Fig. 3.72: Peak voltage induced by a 1 kV ESD discharge in contact mode into the not grounded board connected by the flex cable to the other board (the other board is connected to a large ground plane) for different shielding conditions.

2.7.4.3 Using other traces in a flex as return current traces

The effect of using neighboring traces as return paths for reduced coupling is presented in Fig. 3.73. The edge trace receives a stronger coupled signal.

The effect of using other traces as return is further investigated by changing the load condition of the traces. The following changes have been performed:

- Base condition: Three traces terminated in 50 Ω on both sides (pin 1,5 and 6), 7 traces shorted to GND on both sides using 0 Ω resistors (detailed information of the PCBs is shown in Fig. 3.74)
- Removing the 0 Ω resistors one by one, leaving the traces open
- Adding 100 pF instead of the 0 Ω resistors. This method provides a return path for higher frequency signals, but still allows to use the same trace for lower speed signaling. Thus, reduces ESD coupling, without designating additional traces as GND. It is common design practice.

The data in Fig. 3.73 show that up to 50 V can be induced, relative to board GND, on a trace for a 1 kV ESD. With increasing number of return paths (identified by “A”) the voltage is reduced by about 3x.

Using slow speed traces as ESD return is successful. Identified by “B”, there is no difference in the voltage, if grounding on both sides is compared to using 100 pF capacitors instead of the 0 Ω resistors.

The effect of grounded neighboring traces on the induced voltage is identified by “C”. For C1 the next grounded trace is away from the center trace, therefore, the center and the edge trace receive about the same voltage. However, if many returns exist, the difference between the edge and center trace increases to about 2x, Identified by “C2”.

As Fig. 3.73 shows, a 1 kV ESD pulse in contact mode induced about 7 V (center pin). In scanning one tries to reproduce the induced voltage from the ESD gun by a local probe driven by a TLP. It is interesting to know at which TLP voltage setting will the induced voltage be similar. To measure this, a 10-wire-1mm pitch flex cable has been mounted between the boards. The output of the TLP is connected to different probes. The probes are held against the flex and the peak value of the induced voltage is measured (Fig. 3.74).

Fig. 3.75 shows the TLP voltage needed for inducing the same voltage of 7 V. The values vary from a few hundred volt for the probe which shows the best coupling to 6 kV for a very small probe indicating the importance of probe selection in near field scanning.

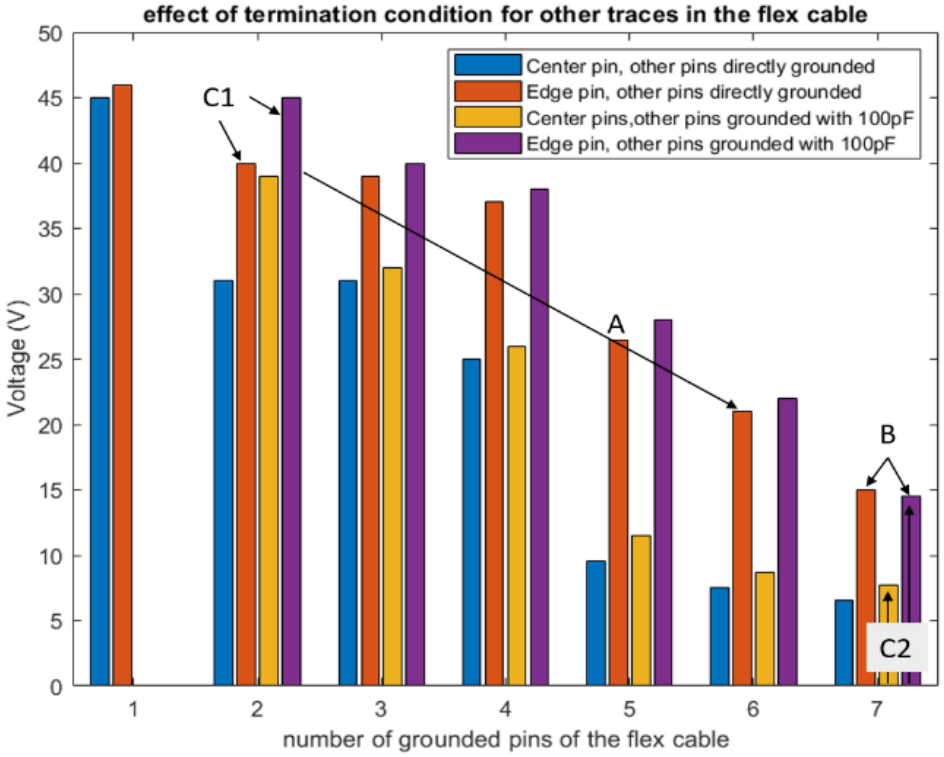


Fig. 3.73: Effect of using other traces on the flex cable as return paths on the induced voltage by a 1 kV contact mode ESD to one board of a board-to-board connection by a 10 pin, 1 mm flex cable of 100 mm length.

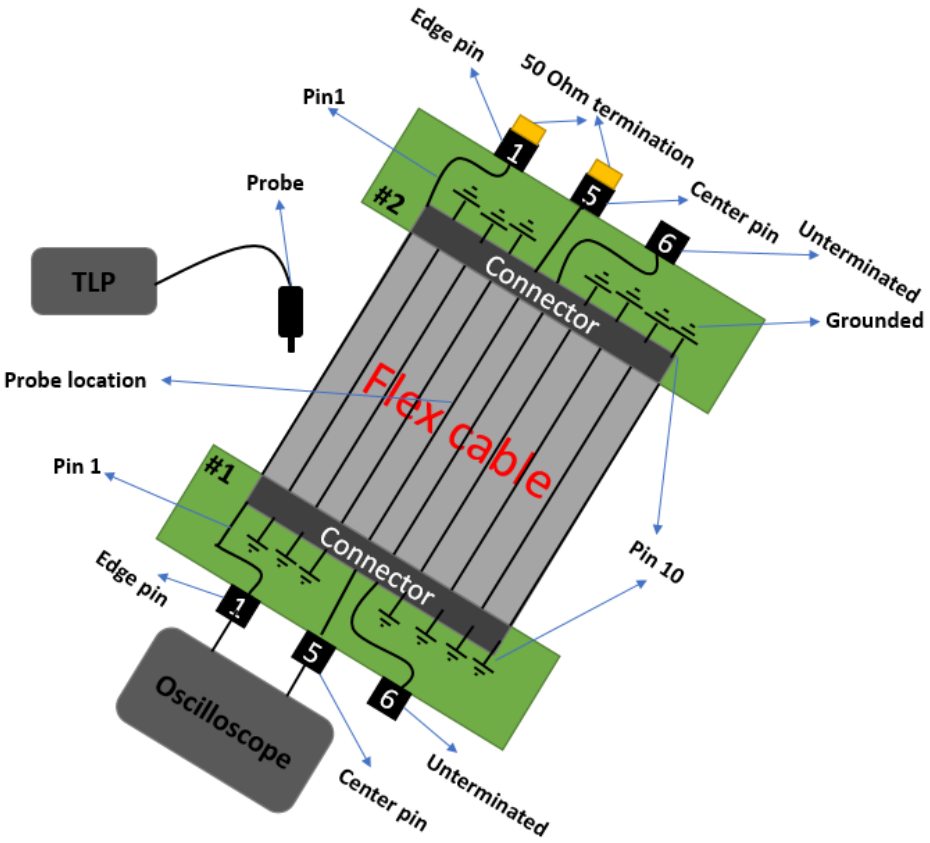


Fig. 3.74: Test setup for board-to-board coupling of an ESD pulse for a flex cable connection.

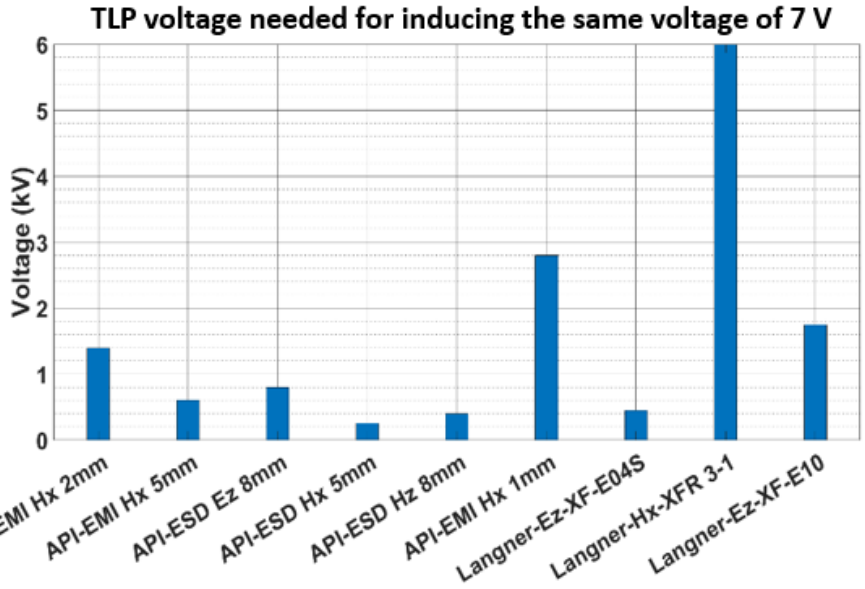


Fig. 3.75: The TLP voltage needed for inducing the same voltage (7 V into the center pin of the Flex cable) as a 1 kV ESD pulse in contact mode induces when using a mm size probe.

2.7.5 Conclusion

This paper shows experimental results for coupling into traces and flex cables. The data was collected to guide the users of the susceptibility scanning in selecting the TLP settings and probes for the coupling voltage levels that are sufficient to cause disturbances, but do not pose a strong risk of damage to the scanned DUT.

The data validates the basic coupling mechanisms via the field: the coupling follows the time derivative of the current that flows through a magnetic field probe and the time derivative of the voltage between an E-field probe and GND. Thus, using a TLP having a sub-nanosecond rise time, a voltage or current pulse having a width of less than 1 ns is induced. This pulse width is also observed for coupled ESD gun voltages, e.g., if an ESD gun is discharged to GND of a system.

The data shows that the TLP settings of a few hundred volts, when selecting a probe in the mm range, is a good starting point for the soft-failure analysis.

Investigations on the flex cables shows strong coupling if the ESD is injected into one board which is connected to another board by the flex cable. A 1 kV ESD pulse in contact mode induced about 5 V. A similar induced voltage was achieved when by using a mm size H-field probe with a 500 V TLP discharge pulse .

As all coupling is geometry driven, the paper can only give a general guideline on the equivalence and TLP settings.

2.7.6 Acknowledgement

We want to thank Phyo Aung from Amber Precision Instruments for support in PCB design.

2.7.7 My Scientific Contribution

This paper investigates and compares the induced voltages generated by various probes and an IEC 61000-4-2 ESD gun in contact mode, with the aim of guiding the selection of appropriate voltage levels and probes during susceptibility scanning. The goal is to ensure a meaningful correlation with real ESD events and to avoid voltage levels likely to cause hard failures.

For this research, I was responsible for designing and setting up the test configurations, conducting the measurements, and performing the data analysis and interpretation of the results.

2 Cumulative Part of the Dissertation

3 Conclusion

This dissertation presents a cumulative body of work aimed at addressing key challenges in electromagnetic compatibility (EMC) across fast-switching power electronics and electrostatic discharge (ESD)-sensitive systems. Through five peer-reviewed contributions, this work explores predictive modeling, high-bandwidth measurement, and ESD susceptibility analysis, with a particular focus on GaN-based power converters and PCB-level signal interfaces.

In the first part of the thesis, a compact behavioral model is developed for GaN transistors, enabling efficient and accurate prediction of conducted emissions up to 300 MHz. By reducing the complexity of parameter extraction and incorporating layout parasitics, the model offers practical utility during early-stage converter design. The modeling framework is further refined through the introduction of the resistive component of the output capacitance, R_{OSS}—a parameter often excluded from datasheets yet shown to significantly affect switching waveform damping and EMI spectral peaks. An S-parameter-based method is proposed to extract R_{OSS}, and its integration into the behavioral model leads to a measurable improvement in EMI prediction accuracy, especially in the 30–150 MHz range.

Building on the need for accurate waveform capture in fast-switching circuits, a new voltage probe was designed using a symmetrical PCB layout with a resistive divider structure. The probe achieves 3 GHz bandwidth while maintaining a high input impedance, offering minimal capacitive loading and a flat frequency response. Its performance was validated through both simulation and experimental testing, making it a reliable tool for high-voltage, high-frequency measurement in GaN converter environments.

The work on voltage probing is extended with the introduction of a compact PCB-based current probe in a subsequent study. The current probe employs a resistive shunt geometry optimized for minimal mutual inductance and wide bandwidth. The integrated current probe allow for high-fidelity capture of switching transients in both symmetrical and asymmetrical layouts. The proposed structures for current and voltage probes represent compact, low-disturbance solution suitable for switching loss analysis, waveform characterization, and EMI validation in state-of-the-art power electronics.

The final contribution of this thesis focuses on ESD susceptibility at the board and interconnect level. Using near-field probes and TLP excitation, the study systematically characterizes the voltages induced in PCB traces and flex cables. These values are compared to those generated by standardized IEC 61000-4-2 ESD gun discharges, offering guidance on the selection of probe types and voltage levels for safe and effective susceptibility scanning. The results emphasize the importance of understanding coupling mechanisms and the potential for overstress during diagnostic procedures.

In conclusion, this dissertation delivers a comprehensive set of methods and tools that support the development of robust, emission-aware electronic systems. By combining predictive modeling, GHz-bandwidth measurement, and practical susceptibility diagnostics, the work advances the state of EMC

engineering in both power conversion and system-level reliability contexts. These contributions lay the groundwork for further research into compact, high-speed EMI and ESD analysis methods that meet the demands of next-generation electronic systems.

List of Figures

List of Tables

Acronyms

DUT Device Under Test
EM Electromagnetic
EMC Electromagnetic Compatibility
EMI Electromagnetic Interference
ESD Electrostatic Discharge
FEM Finite Element Method
GND Ground
ADS Advanced Design System
HEMT High Electron Mobility Transistor
LISN Line Impedance Stabilization Network
MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor
RVD Resistive Voltage Divider
SMD Surface Mount Device
SPICE Simulation Program with Integrated Circuit Emphasis
TLP Transmission Line Pulsing
VNA Vector Network Analyzer
WBG Wide Bandgap
GaN Gallium Nitride
SiC Silicon Carbide
ESR Equivalent Series Resistance
JFET Junction Field Effect Transistor
IC Integrated Circuit
PCB Printed Circuit Board
PEC Perfect Electrical Conductor
RF Radio Frequency
RLC Resistor, Inductor, Capacitor
SMA Sub-Miniature Version
SMT Surface Mount Technology

References

[1] C. Riener, H. Hackl, J. Hansen, A. Barchanski, T. Bauernfeind, A. Pak, B. Auinger, ”Broadband Modeling and Simulation Strategy for Conducted Emissions of Power Electronic Systems Up to 400 MHz,” in Electronics 2022, 11, 4217.

[2] I. Castro et al., “Analytical Switching Loss Model for Superjunc- tion MOSFET With Capacitive Nonlinearities and Displacement Cur- rents for DC–DC Power Converters,” in IEEE Transactions on Power Electronics, vol. 31, no. 3, pp. 2485-2495, March 2016, doi: 10.1109/TPEL.2015.2433017.

[3] M. Turzynski and W. J. Kulesza, “A Simplified Behavioral MOSFET Model Based on Parameters Extraction for Circuit Simulations,” in IEEE Transactions on Power Electronics, vol. 31, no. 4, pp. 3096-3105, April 2016, doi: 10.1109/TPEL.2015.2445375.

[4] Z. Duan, T. Fan, X. Wen and D. Zhang, “Improved SiC Power MOSFET Model Considering Nonlinear Junction Capacitances,” in IEEE Transac- tions on Power Electronics, vol. 33, no. 3, pp. 2509-2517, March 2018, doi: 10.1109/TPEL.2017.2692274.

[5] P. Hillenbrand, M. Beltle, S. Tenbohlen, and S. Mo¨nch, ”Sensitivity analysis of behavioral MOSFET models in transient EMC simulation,” 2017 International Symposium on Electromagnetic Compatibility - EMC EUROPE, Angers, France, 2017, pp. 1-6, doi: 10.1109/EMCEu- rope.2017.8094762.

[6] Fuchs, M., Spielberger, L., Odreitz, K. et al. Fast and simple model generation for superjunction power MOSFETs. Elektrotech. Inftech. 138, 48–52 (2021). https://doi.org/10.1007/s00502-020-00860-3

[7] A. Endruschat, C. Novak, H. Gerstner, T. Heckel, C. Joffe and M. Ma¨rz, “A Universal SPICE Field-Effect Transistor Model Applied on SiC and GaN Transistors,” in IEEE Transactions on Power Electronics, vol. 34, no. 9, pp. 9131-9145, Sept. 2019, doi: 10.1109/TPEL.2018.2889513.

[8] IGOT60R070D1 600V CoolGaNTM enhancement-mode Power Transistor. Available online: https://www.infineon.com/dgdl/ Infineon-IGOT60R070D1-DataSheet-v02 12-EN.pdf?fileId= 5546d46265f064ff016685fa65066523 (accessed on 10 October 2022).

[9] K. Odreitz, “Power MOSFET Modeling for EMC Simulation,” Master’s thesis, Institute of Electronics, Graz University of Technology, Graz, Austria, 2021. Available online:

https://diglib.tugraz.at/download.php? id=61541c9b2c8b0&location=browse

[10] CISPR 25:2021 Vehicles, boats and internal combustion engines - Radio disturbance characteristics - Limits and methods of measurement for the protection of on-board receivers, Available online: https://webstore.iec. ch/publication/64645 (accessed on 6 October 2022).

[11] Dassault Syste`mes, CST Studio Suite, Electromagnetic Field Simula- tion Software. Available online: https://www.3ds.com/products-services/ simulia/products/cst-studio-suite/. (accessed on 23 February 2023).

[12] H. Shichman and D. A. Hodges, ”Modeling and simulation of insulated- gate field-effect transistor switching circuits,” in IEEE Journal of Solid-State Circuits, vol. 3, no. 3, pp. 285-289, September 1968, doi: 10.1109/JSSC.1968.1049902.

[13] Grover, F. W. ”Inductance Calculations, 1946, re-publication.” (2004).

[14] Hochvolt-Netznachbildung NNHV 8123-200 Single path high volt- age AMN (LISN) NNHV 8123-200. Available online: https://www. schwarzbeck.de/Datenblatt/k8123-200.pdf (accessed on 10 October 2022).

[15] M. C. J. Weiser, V. Köhnlein, and I. Kallfass, "A flexible setup for dynamic on-state resistance measurements of GaN HEMTs with one-factor-at-a-time capability," IEEE Trans. Power Electron., vol. 39, no. 6, pp. 7086–7095, Jun. 2024, doi: 10.1109/TPEL.2024.3376313.

[16] R. Zhang, J. P. Kozak, Q. Song, M. Xiao, J. Liu, and Y. Zhang, "Dynamic breakdown voltage of GaN power HEMTs," in Proc. IEEE Int. Electron Devices Meeting (IEDM), Dec. 2020, pp. 23.3.1–23.3.4, doi: 10.1109/IEDM13553.2020.9371904.

[17] J. P. Kozak, R. Zhang, Q. Song, J. Liu, W. Saito, and Y. Zhang, "True breakdown voltage and overvoltage margin of GaN power HEMTs in hard switching," IEEE Electron Device Lett., vol. 42, no. 4, pp. 505–508, Apr. 2021, doi: 10.1109/LED.2021.3063360.

[18] G. Zulauf, S. Park, W. Liang, K. N. Surakitbovorn, and J. Rivas-Davila, "COSS losses in 600 V GaN power semiconductors in soft-switched, high- and very-high-frequency power converters," IEEE Trans. Power Electron., vol. 33, no. 12, pp. 10748–10763, Dec. 2018, doi: 10.1109/TPEL.2018.2800533.

[19] G. Zulauf, Z. Tong, J. D. Plummer, and J. M. Rivas-Davila, "Active power device selection in high- and very-high-frequency power converters," IEEE Trans. Power Electron., vol. 34, no. 7, pp. 6818–6833, Jul. 2019, doi: 10.1109/TPEL.2018.2874420.

[20] A. Jafari et al., "Comparison of wide-band-gap technologies for soft-switching losses at high frequencies," IEEE Trans. Power Electron., vol. 35, no. 12, pp. 12595–12600, Dec. 2020, doi: 10.1109/TPEL.2020.2990628.

[21] M. Samizadeh Nikoo, A. Jafari, N. Perera, and E. Matioli, "Measurement of large-signal COSS and COSS losses of transistors based on nonlinear resonance," IEEE Trans. Power Electron., vol. 35, no. 3, pp. 2242–2246, Mar. 2020, doi: 10.1109/TPEL.2019.2938922.

[22] N. Perera, M. S. Nikoo, A. Jafari, L. Nela, and E. Matioli, "COSS loss tangent of field-effect transistors: Generalizing high-frequency soft-switching losses," IEEE Trans. Power

Electron., vol. 35, no. 12, pp. 12585–12589, Dec. 2020, doi: 10.1109/TPEL.2020.2990370.

[23] M. S. Nikoo, A. Jafari, N. Perera, and E. Matioli, "New insights on output capacitance losses in wide-band-gap transistors," IEEE Trans. Power Electron., vol. 35, no. 7, pp. 6663–6667, Jul. 2020, doi: 10.1109/TPEL.2019.2958000.

[24] Q. Song, R. Zhang, Q. Li, and Y. Zhang, "Investigation on physical origins of output capacitance loss in cascode GaN HEMTs," in Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC), Orlando, FL, USA, 2023, pp. 651–655, doi: 10.1109/APEC43580.2023.10131161.

[25] Q. Song, R. Zhang, Q. Li, and Y. Zhang, "A simple and accurate method to characterize output capacitance losses of GaN HEMTs," in Proc. IEEE Energy Convers. Congr. Expo. (ECCE), Oct. 2022, pp. 1–6, doi: 10.1109/ECCE50734.2022.9948018.

[26] M. Guacci et al., "On the origin of the COSS-losses in soft-switching GaN-on-Si power HEMTs," IEEE J. Emerg. Sel. Topics Power Electron., vol. 7, no. 2, pp. 679–694, Jun. 2019, doi: 10.1109/JESTPE.2018.2885442.

[27] Q. Song, R. Zhang, Q. Li, and Y. Zhang, "Output capacitance loss of GaN HEMTs in steady-state switching," IEEE Trans. Power Electron., to be published, Mar. 2023.

[28] K. Kam, D. Pommerenke, A. Bhargava, B. Steinfeld, C.-W. Lam, and F. Centola, "Quantification of self-damping of power MOSFET in a synchronous buck converter," IEEE Trans. Electromagn. Compat., vol. 53, no. 4, pp. 1091–1093, Nov. 2011, doi: 10.1109/TEMC.2011.2157165.

[29] L. Lai, X. Jiang, C. Li, and W. Luo, "A monolithic gallium nitride-based two-phase synchronous buck converter with high operating frequency," *Electron. Lett.*, vol. 59, no. 7, p. e12768, Apr. 2023, doi: 10.1049/ell2.12768.

[30] R. N. Tripathi, "Dead-time evaluation with switching frequency for GaN-based non-inverting buck-boost DC–DC converter using FPGA-based high-frequency control," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 1, pp. 496–504, Mar. 2024.

[31] Q. Zhao and G. Stojcic, "Characterization of Cdv/dt induced power loss in synchronous buck DC–DC converters," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1508–1513, Jul. 2007.

[32] L. Gill, S. DasGupta, J. C. Neely, and R. J. Kaplar, "A review of GaN HEMT dynamic ON-resistance and dynamic stress effects on field distribution," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 517–537, Jan. 2024.

[33] K. Li, A. Videt, N. Idir, P. L. Evans, and C. M. Johnson, "Accurate measurement of dynamic on-state resistances of GaN devices under reverse and forward conduction in high-frequency power converter," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9650–9660, Sep. 2020.

[34] K. Wang, B. Li, H. Li, X. Yang, and A. Qiu, "Characterization and modeling of frequency-dependent on-resistance for GaN devices at high frequencies," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4925–4933, May 2020.

[35] R. Li, X. Wu, S. Yang, and K. Sheng, "Dynamic on-state resistance test and evaluation of GaN power devices under hard- and soft-switching conditions by double and multiple pulses," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1044–1053, Feb. 2019.

[36] K. Li, P. L. Evans, and C. M. Johnson, "Characterisation and modeling of gallium nitride power semiconductor devices dynamic on-state resistance," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5262–5273, Jun. 2018.

[37] F. Yang, C. Xu, and B. Akin, "Experimental evaluation and analysis of switching transient's effect on dynamic on-resistance in GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 10121–10135, Oct. 2019.

[38] B. Kohlhepp, D. Kübrich, M. Tannhäuser, A. Hoffmann, and T. Dürbaum, "Test setup for dynamic ON-state resistance measurement of high- and low-voltage GaN-HEMTs under hard and soft switching operations," *IEEE Trans. Instrum. Meas.*, vol. 69, no. 10, pp. 7740–7751, Oct. 2020.

[39] K. Li and S. Sen, "A fast and accurate GaN power transistor model and its application for electric vehicle," *IEEE Trans. Veh. Technol.*, vol. 73, no. 4, pp. 4541–4553, Apr. 2024.

[40] K. Li, P. L. Evans, C. M. Johnson, A. Videt, and N. Idir, "A GaN-HEMT compact model including dynamic RDSon effect for power electronics converters," *Energies*, vol. 14, no. 8, 2021.

[41] M. Gholizadeh, K. Odreitz, C. Riener, A. Pak, D. Pommerenke, and J. Hansen, "Modeling a GaN transistor and its impact on conducted emission up to 300 MHz," in *Proc. Int. Symp. Electromagn. Compat. (EMC Europe)*, Krakow, Poland, 2023, pp. 1–6, doi: 10.1109/EMCEurope57790.2023.10274374.

[42] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial GaN power devices and GaN-based converter design challenges," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016.

[43] F. W. Grover, *Inductance Calculations*, New York, NY, USA: Dover, 2004 (original work published 1946).

[44] Infineon Technologies, "IGOT60R070D1 600V CoolGaN enhancement-mode power transistor," Datasheet, [Online]. Available: https://www.infineon.com/dgdl/Infineon-IGOT60R070D1-DataSheet-v02_12-EN.pdf. [Accessed: Oct. 10, 2022].

[45] International Electrotechnical Commission, "CISPR 25:2021 Vehicles, boats and internal combustion engines – Radio disturbance characteristics – Limits and methods of measurement for the protection of on-board receivers," [Online]. Available: https://webstore.iec.ch/publication/64645. [Accessed: Oct. 6, 2022].

[46] Schwarzbeck Mess-Elektronik, "High voltage AMN (LISN) NNHV 8123-200," [Online]. Available: https://www.schwarzbeck.de/Datenblatt/k8123-200.pdf. [Accessed: Oct. 10, 2022].

[47] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si— Evaluation of potentials for performance improvement of inverter and DC–DC converter systems by SiC power semiconductors," IEEE Trans. Ind. Electron., vol. 58, no. 7, pp. 2872–

2882, Jul. 2011. [Online]. Available: http://ieeexplore.ieee.org/document/5560803/

[48] Z. Zhang et al., "Methodology for switching characterization evaluation of wide band-gap devices in a phase-leg configuration," in Proc. IEEE Appl. Power Electron. Conf. Expo., Mar. 2014, pp. 2534– 2541. [Online].

[49] M. R. Ahmed, R. Todd, and A. J. Forsyth, "Analysis of SiC mosfets under hard and soft-switching," in Proc. IEEE Energy Convers. Congress Expo., Sep. 2015, pp. 2231–2238. [Online]. Available: http://ieeexplore.ieee.org/document/7309974/

[50] Garrido, David, et al. "Simple and affordable method for fast transient measurements of SiC devices." IEEE Transactions on Power Electronics 35.3 (2019): 2933-2942.

[51] Winkelholz, Jonas, et al. "Resistive High-Voltage Probe with Frequency Compensation by Planar Compensation Electrode Integrated in Printed Circuit Board Design." Electronics 11.21 (2022): 3446.

[52] PMK Mess- & Kommunikationstechnik GmbH. PHV Series. Available online:http://www.pmk.de/files/downloads/PHV%20S eries%20Datasheet.pdf (accessed on 13 March 2023).

[53] TESTEC. TT-HV 250. Available online: https://www.testec.de/en/assets/pdf/TT-HV/TT-HV 250_Datasheet_DE.pdf (accessed on 13 March 2023).

[54] A. Van den Bossche and D. Bozalakov, "Two channel high voltage differential probe for power electronics applications," 2013 15th European Conference on Power Electronics and Applications (EPE), Lille, France, 2013, pp. 1-6, doi: 10.1109/EPE.2013.6634710.

[55] Reisch, M. Elektronische Bauelemente: Funktion, Grundschaltungen, Modellierung mit SPICE, 2nd ed.; Springer: Berlin/Heidelberg, Germany, 2007; ISBN 3-540-34014-9.

[56] Keysight ADS, Advanced Design System.. Available online: http://edadownload.software.keysight.com/eedl/ads/2011_01/pdf/oaq kref.pdf. (accessed on 13 March 2023).

[57] CRS2512-FX-1001ELF RES SMD 1K OHM 1% 2W 2512. Available online: https://www.bourns.com/data/global/pdfs/CRS.pdf

[58] A. Vella, G. Galioto, G. Vitale, G. Lullo, and G. C. Giaconia, "GaN and SiC device characterization by a dedicated embedded measurement system," Electronics, vol. 12, no. 7, p. 1555, Mar. 2023.

[59] M. Gholizadeh, S. Sadeghi, A. Pak, J. Hansen, and D. Pommerenke, "A PCB based high resistance GHz bandwidth voltage pick up for detecting switching voltage," in 2023 International Symposium on Electromagnetic Compatibility—EMC Europe 2023, Sep. 4, pp. 1-6. IEEE.

[60] M. Grubmüller, B. Schweighofer, and H. Wegleiter, "Characterization of a resistive voltage divider design for wideband power measurements," in SENSORS, 2014 IEEE, Nov. 2, pp. 1332-1335.

[61] D. Garrido et al., "Simple and affordable method for fast transient measurements of

SiC devices," IEEE Trans. Power Electron., vol. 35, no. 3, pp. 2933-2942, 2019.

[62] Tectronix Probes and Probe Accessories. Available online: https://www.tek.com/en/products/oscilloscopes/oscilloscope-probes (accessed on 25 June 2024).

[63] Y. Wang et al., "High bandwidth differential voltage probe for accurate switching characterization of WBG devices," IEEE Trans. Power Electron., doi: 10.1109/TPEL.2024.3401011.

[64] M. Grubmüller, B. Schweighofer, and H. Wegleiter, "Development of a differential voltage probe for measurements in automotive electric drives," IEEE Trans. Ind. Electron., vol. 64, no. 3, pp. 2335-2343, Mar. 2017.

[65] M. Grubmüller, B. Schweighofer, and H. Wegleiter, "A digital isolated high voltage probe for measurements in power electronics," in 2018 IEEE 27th International Symposium on Industrial Electronics (ISIE), Cairns, QLD, Australia, 2018, pp. 791-796, doi: 10.1109/ISIE.2018.8433652.

[66] Y. Wang et al., "Transmission line Rogowski coil: Isolated current sensor with bandwidth exceeding 3 GHz for wide-bandgap device," IEEE Trans. Power Electron., Aug. 21, 2023.

[67] T. Li, D. J. Pommerenke, J. Zhang, and K. Hu, "A current probe for measuring the individual ball current in a ball–grid–array packaged device," IEEE Trans. Instrum. Meas., vol. 62, no. 12, pp. 3323-3329, Aug. 2013.

[68] V. Dubickas and H. Edin, "High-frequency model of the Rogowski coil with a small number of turns," IEEE Trans. Instrum. Meas., vol. 56, no. 6, pp. 2284-2288, Dec. 2007, doi: 10.1109/TIM.2007.907965.

[69] S. Fu et al., "Method of segmented turns arrangement of PCB Rogowski coil with anti-interference ability," IEEE Trans. Instrum. Meas., vol. 70, pp. 1-12, 2021.

[70] A. Mingotti, L. Peretto, and R. Tinarelli, "Effects of multiple influence quantities on Rogowski-coil-type current transformers," IEEE Trans. Instrum. Meas., vol. 69, no. 7, pp. 4827-4834, 2020.

[71] I. A. Metwally, "Design of different self-integrating and differentiating Rogowski coils for measuring large-magnitude fast impulse currents," IEEE Trans. Instrum. Meas., vol. 62, no. 8, pp. 2303-2313, 2013.

[72] E. Hemmati and S. M. Shahrtash, "Digital compensation of Rogowski coil's output voltage," IEEE Trans. Instrum. Meas., vol. 62, no. 1, pp. 71-82, 2013.

[73] I. A. Metwally, "Coaxial-cable wound Rogowski coils for measuring large-magnitude short-duration current pulses," IEEE Trans. Instrum. Meas., vol. 62, no. 1, pp. 119-128, 2013.

[74] M. Marracci et al., "Critical parameters for mutual inductance between Rogowski coil and primary conductor," IEEE Trans. Instrum. Meas., vol. 60, no. 2, pp. 625-632, 2011.

[75] I. A. Metwally, "Self-integrating Rogowski coil for high-impulse current measurement," IEEE Trans. Instrum. Meas., vol. 59, no. 2, pp. 353-360, 2010.

[76] G. Robles et al., "Inductive sensor for measuring high frequency partial discharges

within electrical insulation," IEEE Trans. Instrum. Meas., vol. 58, no. 11, pp. 3907-3913, 2009.

[77] "CWT MiniHF," Power Electronics Measurement, Nottingham, U.K., 2020. [Online]. Available: http://pemuk.com

[78] Y. Shi, Z. Xin, P. C. Loh, and F. Blaabjerg, "A review of traditional helical to recent miniaturized printed circuit board Rogowski coils for power-electronic applications," IEEE Trans. Power Electron., vol. 35, no. 11, pp. 12207-12222, Apr. 2020.

[79] K. Wang et al., "A high-bandwidth integrated current measurement for detecting switching current of fast GaN devices," IEEE Trans. Power Electron., vol. 33, no. 7, pp. 6199–6210, Jul. 2018.

[80] "Current Viewing Resistors," T&M Research, Albuquerque, NM, USA, 2020. [Online]. Available: http://www.tandmresearch.com/.

[81] W. Zhang, Z. Zhang, and F. Wang, "Review and bandwidth measurement of coaxial shunt resistors for wide-bandgap devices dynamic characterization," in Proc. IEEE Energy Convers. Congr. Expo., 2019, pp. 3259–3264.

[82] H. Rezaei et al., "1 Ω disk resistor full-wave modeling for JS-002 standard," in 2021 43rd Annual EOS/ESD Symposium (EOS/ESD), vol. 43, pp. 1-10. IEEE, 2021.

[83] Z. Qi et al., "A high-bandwidth and easy-to-integrate parasitics-based switching current measurement method for fast GaN devices," IEEE Trans. Power Electron., vol. 38, no. 1, pp. 447-459, 2022.

[84] M. Faifer et al., "A low-cost approach to the skin effect compensation in cylindrical shunts," IEEE Trans. Instrum. Meas., vol. 66, no. 9, pp. 2266-2273, Sep. 2017, doi: 10.1109/TIM.2017.2668498.

[85] M. Danilovic et al., "Evaluation of the switching characteristics of a gallium-nitride transistor," in Proc. IEEE Energy Convers. Congr. Expo.: Energy Convers. Innov. Clean Energy Future, 2011, pp. 2681–2688.

[86] J. A. Ferreira, W. A. Cronje, and W. A. Relihan, "Integration of high frequency current shunts in power electronic circuits," IEEE Annu. Power Electron. Specialists Conf., vol. 10, no. 1, pp. 1284–1290, 1992.

[87] J. H. Park, "Shunts and inductors for surge-current measurements," J. Res. Nat. Bureau Standards, vol. 39, no. 3, pp. 191–212, 1947.

[88] J. C. Hernandez et al., "Ultrafast switching superjunction MOSFETs for single phase PFC applications," in Proc. 29th Annu. Appl. Power Electron. Conf. Expo., 2014, pp. 143–149.

[89] W. Zhang et al., "High bandwidth low-inductance current shunt for wide-bandgap devices dynamic characterization," IEEE Trans. Power Electron., vol. 36, no. 4, pp. 4522–4531, Apr. 2021.

[90] S. Klever and R. W. De Doncker, "A high-bandwidth and low-inductive sensor for measuring the commutation current of WBG devices," in 2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe), Aalborg, Denmark, 2023, pp. 1-8, doi: 10.23919/EPE23ECCEEurope58414.2023.10264674.

[91] P. Ziegler et al., “Evaluation of a low-cost wide bandwidth current shunt for characterization of wide bandgap semiconductor devices,” in 2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe), Aalborg, Denmark, 2023, pp. 1-9, doi: 10.23919/EPE23ECCEEurope58414.2023.10264595.

[92] L. Shillaber et al., “Ultrafast current shunt (UFCS): A gigahertz bandwidth ultra-low-inductance current sensor,” IEEE Trans. Power Electron., vol. 37, no. 12, pp. 15493-15504, 2022.

[93] Y. Wang et al., “Impedance-matching shunt: Current sensor with ultrahigh bandwidth and extremely low parasitics for wide-bandgap device,” IEEE Trans. Power Electron., vol. 37, no. 10, pp. 11528-11533, May 23, 2022.

[94] Á. F. Hegedűs and T. Dabóczi, “A wideband current sensing method based on real-time resistance identification,” IEEE Trans. Instrum. Meas., vol. 73, pp. 1-14, 2024, Art no. 9500314, doi: 10.1109/TIM.2023.3338684.

[95] E. Grundkötter, P. Weßkamp, and J. Melbert, “Transient thermo-voltages on high-power shunt resistors,” IEEE Trans. Instrum. Meas., vol. 67, no. 2, pp. 415-424, Feb. 2018, doi: 10.1109/TIM.2017.2775418.

[96] T. C. Mallett, “Aging in commercial thick- and thin-film resistors: Survey and uncertainty analysis,” IEEE Trans. Instrum. Meas., vol. 68, no. 11, pp. 4190-4204, Nov. 2019, doi: 10.1109/TIM.2019.2938869.

[97] CRS2512-FX-1001ELF RES SMD 1K OHM 1% 2W 2512. Available online: https://www.bourns.com/data/global/pdfs/CRS.pdf.

[98] ERJ-2BQFR75X RES 0.75 OHM 1% 1/6W 0402. Available online: https://industrial.panasonic.com/cdbs/wwwdata/pdf/RDN0000/AOA0000C313.pdf.

[99] Muchaidze G, Koo J, Cai Q, Li T, Han L, Martwick A, Wang K, Min J, Drewniak JL, Pommerenke D. Susceptibility scanning as a failure analysis tool for system-level electrostatic discharge (ESD) problems. IEEE TEMC, 2008 May 20

[100] ANSI/ESD SP14.5-2015 ESD Association Standard Practice for Electrostatic Discharge Sensitivity Testing – Near Field Immunity Scanning – Component/Module /PCB Level

[101] Hosseinbeig A, Izadi OH, Shinde S, Pommerenke D, Shumiya H, Maeshima J, Araki K. A study on correlation between near-field EMI scan and ESD susceptibility of ICs. In2017 IEEE Int. Symp. EMCSI 2017 Aug 7 (pp. 169-174). IEEE.

[102] J.Xiao, D.Pommerenke, Jin Min, Wei Huang, Giorgi Muchaidze, “Local probe injection compared to direct ESD injection”, EMC Compo, Nov. 2009, Toulouse, France

[103] Li Z, Xiao J, Seol B, Lee J, Pommerenke D. Field injection probes for field coupled electrostatic discharge sensitivity database of ICs. In2010 IEEE Int. Symp. EMC, 2010 Jul 25 (pp. 329-333).

[104] Li Z, Xiao J, Seol B, Lee J, Pommerenke D. Measurement methodology for establishing an IC ESD sensitivity database. In2010 AP-Int. Symp. EMC 2010 Apr 12 (pp. 1051-1054).

[105] Wu X, Grassi F, Spadacini G, Pignari SA, Paoletti U, Hoda I. Investigation of Semi-Rigid Coaxial Test Probes as RF Injection Devices for Immunity Tests at PCB Level. IEEE Access. 2020 Aug 10;8:147919-29.

[106] Hosseinbeig A, Izadi OH, Solanki S, Lingayat TD, Subramanya BP, Vaidhyanathan AK, Zhou J, Pommerenke D. Methodology for analyzing ESD-induced soft failure using full-wave simulation and measurement. IEEE Transactions on Electromagnetic Compatibility. 2018 Feb 1;61(1):11-9.

[107] Yousaf J, Nah W, Al Majali ER, Saif H, Rmili H. Rapid Characterization of Efficient System Level ESD Protection Strategy Using Coupling Transfer Function. Microelectronics Journal. 2021 Feb 7:105004.

[108] Yousaf J, Lee H, Nah W. System Level ESD Analysis-A Comprehensive Review II on ESD Coupling Analysis Techniques. Journal of Electrical Engineering and Technology. 2018;13(5):2033-44.

[109] Jeon C, Lim H, Jin J, Kim J. A New Method of Component-level ESD Test to Assess System-level ESD Risk for ICs. In2019 Joint Int. Symp. EMC, EMC Sapporo/APEMC, 2019 Jun 3 (pp. 681-684). IEEE.