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Design of a modular I3C pad structure in a 110 nm TSMC process

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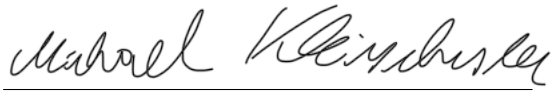

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Abstract

The I2C (Inter-Integrated Circuit) interface is a proven standard for embedded systems. The I2C interface is under pressure to reduce power consumption and chip area while increasing data transfer. For this reason, the research addresses the critical need for the I3C (Improved Inter Integrated Circuit) interface, solving the corresponding requirements. This work addresses a significant research gap by exploring the need for I3C, which is currently underrepresented in the existing literature. By using a modular concept, this study demonstrates their practical application in analog circuit design, facilitating rapid reuse and reducing time-to-market.

The study investigates the feasibility of a modular system for an I3C I/O (Input/Output), with the aim of determining an optimal granularity that provides a favorable cost-value ratio. Modular and non-modular blocks of the I3C I/O need to be identified to determine reasonable I3C I/O variants. This feasibility study includes the schematic implementation of different I3C I/O variants within the Cadence design environment, which must comply with the I3C and I2C standards. An area estimation of the modular and non-modular schematic blocks was conducted, to show possible area savings.

The results show that a 3.3 V modular option can achieve area savings, but the 1.2 V modular option does not provide similar benefits. The discussion highlights the economic benefits of this approach, emphasizing its potential to reduce chip area and facilitate design reuse. This modular strategy is especially valuable for creating numerous I3C I/O options due to its ease of reuse.

Kurzfassung

Die I2C Schnittstelle ist ein bewährter Standard für eingebettete Systeme. I2C steht unter dem Druck, den Stromverbrauch und die Chipfläche zu verringern und gleichzeitig die Datenübertragung zu erhöhen. Aus diesem Grund befasst sich die Masterarbeit mit dem kritischen Bedarf für I3C Anwendungen, um die damit verbundenen Anforderungen zu erfüllen. Diese Arbeit greift eine wichtige Forschungslücke auf, indem sie den Bedarf an I3C untersucht, der derzeit in der bestehenden Literatur unzureichend berücksichtigt wird. Durch den Einsatz eines Modularitätskonzepts demonstriert diese Masterarbeit deren praktische Anwendung im analogen Schaltungsdesign, was eine schnelle Wiederverwendung ermöglicht und die Markteinführung beschleunigt. Die Studie untersucht die Machbarkeit eines modularen Systems für I3C E/A (Eingang/Ausgang), mit dem Ziel, eine optimale Auflösung zu wählen, die ein günstiges Kosten-Nutzen-Verhältnis bietet. Es müssen modulare und nicht-modulare Blöcke von I3C E/As identifiziert werden, um sinnvolle I3C E/A Varianten zu bestimmen. Diese Machbarkeitsstudie beinhaltet die schematische Implementierung verschiedener I3C E/A Varianten innerhalb der Designumgebung von Cadence, die den I3C/I2C Standards entsprechen müssen. Eine Flächenabschätzung der modularen und nicht-modularen Blöcke wurde durchgeführt, um mögliche Flächeneinsparungen aufzuzeigen. Die Ergebnisse zeigen, dass eine modulare 3.3 V Variante zwar Flächeneinsparung erzielen kann, die modulare 1.2 V Variante jedoch keine ähnlichen Vorteile bietet. In der Diskussion werden die finanziellen Vorteile dieses Ansatzes hervorgehoben und das Potenzial zur Reduzierung von Chipfläche und der leichten Wiederverwendung von Designs betont. Diese modulare Strategie ist besonders wertvoll für die Erstellung zahlreicher I3C E/A Varianten, da sie zeitsparend wiederverwendet werden kann.

Introduction

Electronic systems need to share a lot of information among various components. Engineers have developed various standard protocols over the last decades that help systems communicate successfully [1]. Those standard protocols need a set of defined rules to send and receive data, via a physical medium. The protocol defines rules, regulations, synchronization between systems, syntax, and semantics. Communication protocols are classified into inter and intra-system protocols. Inter-system protocols are used to set up a data transfer between two devices such as a PC and a microprocessor kit. An inter-system protocol transmits data via an inter-bus system, such as Universal Asynchronous Receiver-Transmitter (UART), Universal Synchronous and Asynchronous Receiver-Transmitter (USART), or Universal Serial Bus (USB). Communication within a circuit board is done via an intra-system protocol, like I2C or SPI (Serial Peripheral Interface). In this thesis, only intra-system protocols are of interest. SPI is one of the most commonly used interfaces between multiple integrated circuits (ICs) on a printed circuit board (PCB) for short connections. SPI was designed by Motarloa in the 1980s, to connect integrated circuits within embedded systems [2]. SPI is a full duplex interface with 4 wires. Two wires are used to transfer data from the master to the slave (MOSI) and one data line is used to do it and vice versa (MISO). In addition, a clock line (CLK) for synchronization and a Chip select line (CS) is required [3]. When a few slaves are connected to a single master device, SPI is the appropriate solution. One limitation of SPI is the required CS line for each device that is added to the bus. This can lead to a high pin count and can lead to routing difficulties on a PCB. Nevertheless, SPI is excellent for high-frequency applications and low-level hardware design [4]. For this thesis, SPI is not of interest.

I2C was developed further and is therefore a more intriguing research topic. I2C was developed by Philips Semiconductors in the same decade as SPI [1]. The reason for the development of I2C was to connect a CPU (Central Processing Unit) to the peripheral chips in a TV-set easily. Connecting peripheral devices to a microcontroller unit is often realized by using the parallel address and the data bus of the microcontroller. Potentially a complex wiring scheme is needed to route the data and the address lines on the PCB. Saving area in mass production increases profitability and makes products more affordable for customers. In other words, using a parallel bus is an inexpensive solution for mass production.
The main aim of Philips Semiconductors was, to provide a simple bidirectional two-wire bus [5]. Bidirectional means that two systems can exchange information in both directions. The two-wire bus is established by a serial data line (SDA) and a serial clock line (SCL). Data is transmitted via the SDA line while synchronization is established with the SCL line [6]. Because of this simple implementation with 2 wires, I2C has been proven as

a standard for embedded systems [6]. Today I2C can be found in many systems, such as single-chip microcontrollers, general-purpose circuits like the LCD and LED drivers, real-time clocks for Analog to Digital (A/D) converters, temperature sensors, and many more. Those systems are getting smaller in size, which also forces the industry to develop smaller electronic components. Not only a reduction of the size is necessary, but at the same time the amount of data increases with the number of devices connected to the bus. In various fields, like automotive, IoT (Internet of Things), and smartphones, the interfaces are required to reduce power consumption and chip area while the data transfer increases tremendously [7]. At this point, the I2C interface is barely fulfilling the stated requirements.

The solution for the involved requirements was the development of the I3C Interface by the MIPI alliance, which was founded by ARM, Nokia, ST, and Texas Instruments [8]. I3C has been developed to provide a two-wire interface with low power consumption, high speed data transfer and low cost [9]. I3C was designed by the MIPI alliance group and was published in 2017 to the public[9]. "MIPI Alliance is a collaborative global organization serving industries that develop mobile and mobile-influenced devices" [8]. This organization has its force on designing and promoting hardware and software interfaces, which makes it easier to integrate parts that are integrated into devices, like in automotive, 5G (fifth-generation technology standard for broadband cellular networks), IoT, or mobile applications [8]. "MIPI Alliance crafts all of its specifications to meet the stringent operating conditions required in mobile devices: high-bandwidth performance, low power consumption, and low electromagnetic interference (EMI)" [8]. I3C is the next generation of I2C and implies backward compatibility to I2C, meaning that the data transfer between I2C and I3C devices is still possible. The bus architecture is the same as for I2C. I3C uses higher data rates, lower power levels and allows the user to implement flexible design implementations [7]. One of the most important features of I3C is the reduction of power consumption. I3C can reduce power consumption by a factor of 4 in the slowest data rate mode and can save even more power in higher data rate modes compared to I2C [10]. Reducing power consumption is a real need because the amount of sensors used in the automotive and consumer market is steadily increasing [11]. With the stated limitations of I2C, those needs could not be satisfied, thus demanding the I3C interface.
Applying a new communication interface is challenging since only a small amount of literature on the I3C topic is available. On the other hand, this challenge makes the topic appealing, especially when starting the implementation process from the beginning. In addition, I/O design does not impose the big challenge, but every product necessitates a reliable I/O to establish communication with other devices. However, the design of a reliable I/O structure is not effortless, since various requirements and conditions must be considered when designing the I/O. This specifically applies to the implementation of a failsafe structure, which must endure certain Electrostatic discharge (ESD) requirements. Furthermore, the actual literature status on MIPI-compliant I3C I/O will be evaluated. Although the demand for I3C-compatible devices is permanently increasing, there is a lack of literature on I3C I/Os. As previously mentioned the I3C standard was developed by the MIPI alliance, which revealed the public specification document of MIPI [9]. The I3C specification [9] serves as a guideline for the implementation. All further design considerations are based on the I3C Specification, examined in [9].

Since the research question concerns the feasibility of a modular design approach of an I3C I/O, further literature was conducted to answer the research question within the methods section. First and foremost, the basic functionality of I/Os is clarified in [12] and [13]. In the work of [12] and [13] the use of different types of I/Os is stated. In addition the location of Pads on an integrated circuit (IC) is shown. As previously mentioned, the I2C protocol is well-established in the industry, and the main components of an I2C I/O driver can be viewed in [14]. In combination with the official specification [9] and the main building blocks of an I2C I/O, deeper investigations into the design of a modular I3C I/O can be performed.

Heading from the general structure of I3C I/Os to the specific components of an I3C I/O, the input section of the I3C can be realized, by implementing a Schmitt trigger [15], [16], [17]. The Schmitt trigger is relevant for reading the data from the bus and distinguishing the two logic levels 0 and 1. An important building block of an I3C I/O is the output driver, which must be versatile, handling the I2C and the I3C protocol. In the book of Baker [15] the main principle of a Schmitt trigger is shown and the design steps with all the necessary design considerations are demonstrated. The I3C I/O must be qualified to read data from the I3C bus and has to be capable of transmitting data to other devices [18], [15], [19]. This can be accomplished with an output driver, forcing the bus to one of the logic levels, 0 and 1. In addition, the output driver must be compatible with the I2C specification. The main difference between I2C and I3C is the output driver. I2C uses an open-drain driver, whereas I3C uses a Push-Pull driver. At this point, the research question must be considered in detail, using the modular approach during the design, combining I2C- and I3C-specific components. To avoid any overlaps while switching from one logic state to the other, a dedicated logic block is used to control the output driver. Designing a non-overlapping logic block can be conducted with the previous work in [20]. Moreover, the output driver must be able to endure an electrostatic discharge (ESD) event. All the relevant ESD knowledge and implemented ESD protection of this thesis are contained in the book Electrostatic Discharge Protection [21].

A very important aspect of the ESD implementation is the failsafe requirement. Basic concepts of failsafe I/Os are presented in [22]. The work in [23] focuses on the ESD design of failsafe and voltage-tolerant IO circuits. Though some examples of failsafe I/Os are presented in [23], a new concept may be evaluated, accomplishing the requirements from the I3C specification [9]. With regard to the I2C specification, filtering glitches from the bus must be feasible. For this reason, a glitch filter block is required, using the concept discussed in [24] and [25].
The delay block is the last remaining block, which has to be considered within the literature research. Several delay variants were considered for the delay block [26], [27], [28].

With the literature research carried out, the research question can be addressed. What can a modularity principle for an I3C I/O look like? What is a reasonable granularity of such a modularity principle to give a good cost-value ratio? In this thesis, the feasibility of creating a modular I3C I/O in a 110 nm TSMC (Taiwan Semiconductor Manufacturing Company Limited) process is discussed. The scope of this thesis is the development of the I3C I/O, with the complete schematic and the corresponding simulation results. The

layout design and the test chip evaluations are outside the scope of this work. The outcome of this thesis can be part of a future test chip. The modular I3C approach could be a convenient solution, separating I2C- and I3C-related blocks for future implementations. Nowadays, I2C backward compatibility is inevitable, due to the fact I2C is widely used in industry. The backward compatibility will not be a strict requirement once the I3C replaces the I2C almost entirely. Accordingly, area and cost could be decreased by building new ICs. Referring to customer needs, a modular approach could be a convenient way to enhance full flexibility using the I2C, I3C module, or both modules together.
As the literature research showed, a few previous works conducted the I3C topic. Nevertheless, no literature could be found, that is dedicated to the research question. In particular, a failsafe concept at the output driver, implying ESD compliance will show new conclusions. The work in [11] showed a testchip in a 180 nm TSMC process. In comparison to [11], this thesis addresses a smaller process node, which involves lower voltage levels.

Acronyms

A/D Analog to Digital.

C_i Input Capacitance.

CDM Charged Device Model.

CLK Clock signal.

CMOS Complementary Metal Oxide Semiconductor.

Cpk Process Capability Index.

CPU Central Processing Unit.

CS Chip Select.

DfR Design for Reliability.

DI Digital Input.

DO Digital Output.

EMI Electromagnetic Interference.

ESD Electrostatic Discharge.

Fm Fast Mode.

Fm+ Fast Mode Plus.

FSC Failsafe Control.

GCNMOS Gate Coupled NMOS.

GGNMOS Gate Grounded NMOS.

GPIO General Purpose Input/Output.

HBM Human Body Model.

HDL High Description Language.

HDR-DDR High Data Rate Double Data Rate.

HDR-TSL High Data Rate Ternary Symbol Legacy.

HDR-TSP High Data Rate Ternary Symbol Pure.

I/O Input/Output.

I2C Inter Integrated Circuit.

I3C Improved Inter Integrated Circuit.

I_{i_FS} Input Current Failsafe.

I_i Input Current.

I_{OH} HIGH-level Output Current.

I_{OL} LOW-level Output Current.

IC Integrated Circuit.

IE Input Enable.

IEC International Electrotechnical Commission.

IoT Internet of Things.

LCD Liquid Crystal Display.

LDE Layout Dependent Effect.

LED Light Emitting Diode.

LSL Lower Specification Limit.

MC Monte Carlo.

MIM Metal Insulator Metal.

MISO Master In Slave Out.

MM Machine Model.

MOSI Master Out Slave In.

NMOS N-type Metal Oxide Semiconductor.

NPOR Low-Active Power On Reset.

OSI Open System Interconnection.

PCB Printed Circuit Board.

PDNs Pull Down Networks.

PLL Phase Locked Loop.

PMOS P-type Metal Oxide Semiconductor.

PVT Process Voltage Temperature.

SCL Serial Clock Line.

SCR Silicon Controlled Rectifier.

SDA Serial Data Line.

SDR Single Data Rate.

SOA Safe Operating Area.

SOAC Safe Operating Area Check.

SPI Serial Peripheral Interface.

$\mathbf{t}_{CF}$ SCL Clock Fall Time (MIPI I3C Specification)).

$\mathbf{t}_{CR}$ SCL Clock Rise Time (MIPI I3C Specification)).

$\mathbf{t}_{fCL}$ SCL Clock Fall Time (NXP I2C Specification).

$\mathbf{t}_{phl}$ Propagation Delay Time High to Low.

$\mathbf{t}_{plh}$ Propagation Delay Time Low to High.

$\mathbf{t}_{rCL}$ SCL Clock Rise Time (NXP I2C Specification).

$\mathbf{t}_{sCO}$ Clock in to Data Out for Slave (MIPI I3C Specification).

$\mathbf{t}_{VD}$ Data Valid Time (NXP I2C Specification).

tm Typical mean.

TSMC Taiwan Semiconductor Manufacturing Company Limited.

UART Universal Asynchronous Receiver-Transmitter.

USART Universal Synchronous and Asynchronous Receiver-Transmitter.

USB Universal Serial Bus.

USL Upper Specification Limit.

$\mathbf{V}_{OH}$ Output High Level.

$\mathbf{V}_{OL}$ Output Low Level.

VLSI Very Large Scale Integration.

wo Worst One.

wp Worst Power.

WPE Well Proximity Effect.

ws Worst Speed.

wz Worst Zero.

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1 Research and Economic Question

How complex must the modularity principle for an I3C I/O be for it to make economic sense? Since this thesis was developed in cooperation with ams-OSRAM AG, the research question can be seen more as an economic question. The economic question is related to the chip area and the development costs. Is it possible with such a modular approach to save chip area? For this reason, it must be clarified which measures must be taken to develop such a modular I3C I/O. Since the time to market in industry is quite tight, the development time is limited. Is it possible to decrease the development time with this modularity principle?

Answering these questions requires several steps. First and foremost, a definition of all I2C and I3C relevant functions must be clarified. For this reason, a permutation matrix with a potential combination of I3C I/O options was established. A reduced number of I/O options results from the permutation matrix. The reduced I/O options are implemented in Chapter 5. Based on the circuits shown from the literature research the individual blocks are designed. The design process was carried out first with some hand calculations and later proven within the Cadence design environment. Different simulation and test benches are developed to guarantee the full functionality of the I3C I/O variants. These simulations include transient, DC, SOAC (Safe Operating Area Check), Dynamic Floating Node DC Leakage Path Check, as well as an MC (Monte Carlo) analysis. The I3C I/O must be robust against process, voltage, and temperature (PVT) variations. A corner setup was elaborated to confirm full functionality across all process, temperature, and supply corners. All simulation results must be evaluated and compared with the specification limits, which are stated in the I3C and I2C specification documents [9] and [5]. Finally, floorplanning and a size comparison between I/O options can be conducted. Based on the results of the size comparison a conclusion is made if the modular approach makes economic sense.

2 I/O Cells in a nutshell

I/Os are responsible for communicating data between the chip and the external world [12]. The external world is a PCB where the chip is placed. "Good I/O subsystem has the following properties:

1. Drives large capacitances typical of off-chip signals
2. Operates at voltage levels compatible with other chips
3. Provides adequate bandwidth
4. Limits slew rates to control high-frequency noise
5. Protects chip against damage from electrostatic discharge (ESD)
6. Protects against over-voltage damage
7. Has a small number of pins (low cost)" [12][p. 590 - 591]

In order to design I/O structures, the analog expertise as well as the knowledge of process-specific ESD structures are needed [12]. "Process and library vendors normally supply well-characterized pad libraries tailored to a given manufacturing process" [12][p. 591]. To get an overview of basic options in I/O subsystems most of the important pads are presented [12]. Such an I/O library contains *VDD* and *GND* pads, bidirectional pads, digital input (DI), and digital output (DO) pads. Bidirectional pads are General Purpose Input/Output (GPIO) or I3C I/Os because those pads contain an input receiver and an output driver. In addition, corner cells are used to contain the connection and stress relief structures in all metal layers in the corner of the chip and filler I/O cells are used to contain the geometrical information of the power rings in all metal layers. An overview of the different pads, which are explained in the following chapters, is depicted in Figure 1. The I/O area is used as a placeholder for various pads, depending on the requirements of the IC.

2.0.1 VDD and GND Pads

A VDD and GND pad is used to connect the chip to the external power supply. "Power and ground pads are simply squares of metal connected to the package and the on-chip power grid" [12][p. 591]. VDD and GND pads usually contain some of the ESD clamp circuits. If the chip needs a high current, enough VDD and GND pads must be placed to support the necessary current.

2.0.2 Digital Output (DO) Pads

Digital output (DO) pads are used to drive resistive and capacitive loads. Their drive capability must be sufficient to reach the required rise and fall times for a certain capacitive load [12]. "If the pad drives resistive loads, it must also deliver enough current to meet the required DC transfer characteristics" [12][p. 591]. "Output pads generally contain additional buffering to reduce the load seen by the on-chip circuitry driving the pad"[12][p. 591].

2.0.3 Digital Input (DI) Pads

Digital Input (DI) Pads are used to convert a distorted signal into a clean valid signal with correct logic levels [12]. A valid signal with correct logic levels is necessary to have correct functionality in the core circuitry [12]. The input path also includes an ESD protection circuitry. If the core voltage level differs from the input signal the input buffer performs a voltage conversion. Digital input pads may contain a Schmitt trigger circuit. A Schmitt trigger can filter out glitches from a noisy input signal.

2.0.4 Bidirectional Pads

Bidirectional pads contain a digital input and an output path. General Purpose Input Output pads (GPIO) and I3C I/Os belong to the category of bidirectional pads. A GPIO pad may also include an analog path, for transmitting analog signals to the core circuitry.

2.0.5 Analog Pads

"Analog inputs and outputs connect to simple metal pads and then directly to the on-chip analog circuitry without any digital buffer or driver" [12][p. 593]. An analog input and output pad must include primary and optionally a secondary ESD protection [12]. In Chapter 2.1, ESD concepts are discussed in more detail.

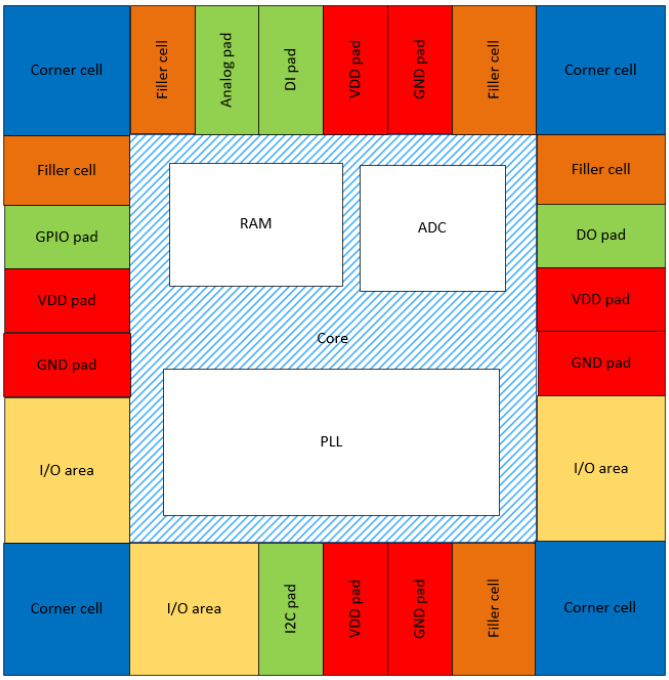

Figure 1: Illustration of different pad types.

2.0.6 Core-limited vs Pad-limited design

Based on the application and the complexity of the chip, a pad-limited or a core-limited design is chosen. If the core determines the die area it is named a core-limited design. If the area occupied by I/Os determines the die area it is called a pad-limited design, depicted in Figure 2. I/Os in a pad-limited design are geometrically narrow, to place a large number of I/Os.

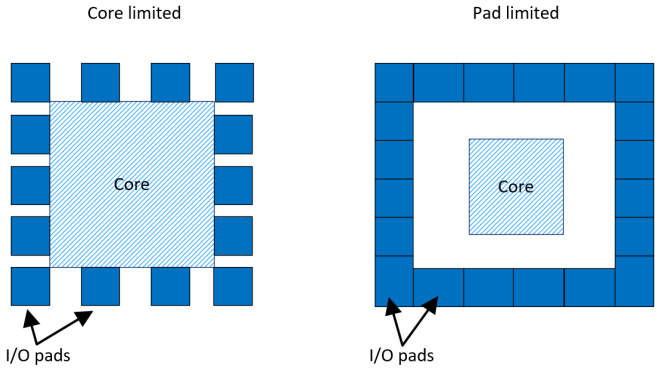

Figure 2: Core limited vs pad limited design.

2.1 ESD concept

This chapter gives an overview of the implemented ESD concept. For the sake of clarity, this chapter will focus on the general ESD concept and not on the detailed functionality. For more information, see [21].

2.1.1 ESD introduction

ESD is an important issue when dealing with risks to the functionality of ICs and other electronic components [21]. "It is an event in which infinite amount of charge is transferred from one object (i.e., human body) to another (i.e., microchip)" [21]. In a relatively short period of time, a high current can pass through the item, caused by the ESD event [21]. If the energy created by an ESD event in the IC is not rapidly dissipated, it may lead to failure or destruction of the internal circuitry [21]. Damage can happen as follows: Gate oxide breakdown, a junction failure, or a damaged interconnect. Those damages can have an impact on the transistor behavior, reliability, and overall circuit behavior. The stated damages are shown in Figure 3.

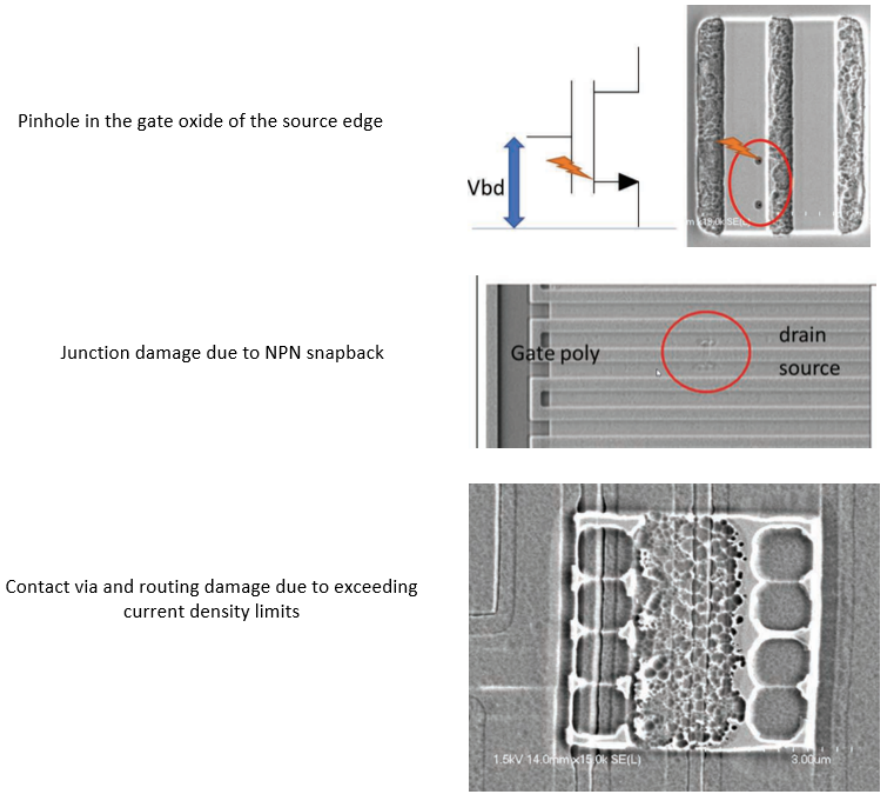

Figure 3: Damages caused through an ESD event [29][p. 60].

ESD events happen every day and in different situations of life. Charge can be generated when two objects collide or glide past each other [21]. This is known as the triboelectric effect [21]. In general, a classification of four standards or models can be made:

1. "Human Body Model (HBM): Describes an event when a charged person touches an IC
2. Machine Model (MM): A charged metal object which is in contact with an IC
3. Charged Device Model (CDM): Describes an event when a charged device is in contact with a grounded object
4. International Electrotechnical Commission (IEC): Describes an event when a charged cable or wire is in contact with an electronic component" [21][p. 2-3]

ICs must be protected against the mentioned ESD events [21]. For this reason, an ESD protection circuit must be implemented [21]. For this thesis, the HBM model is of interest. The protective devices are designed to withstand a 4 kV HBM voltage. When the system is in normal operation the ESD device must be turned off and in case of an ESD event the ESD protection device must be quickly switched on [21]. The high current during an ESD event must be conducted by the ESD device [21]. This high ESD current must be discharged quickly to ground [21]. An important feature of the ESD device is that it must not be damaged by the ESD event [21]. In addition, the ESD device must clamp the voltage to a certain voltage level and the ESD device must be switched off again after the ESD event has ended [21]. In Figure 4 the operation window of an ESD protection device is described. To prevent the ESD protection device from operating outside the normal operation window, a safety margin is implemented. In addition, the ESD protection trigger voltage must have enough margin to the oxide breakdown window, to prevent any gate oxide damage.

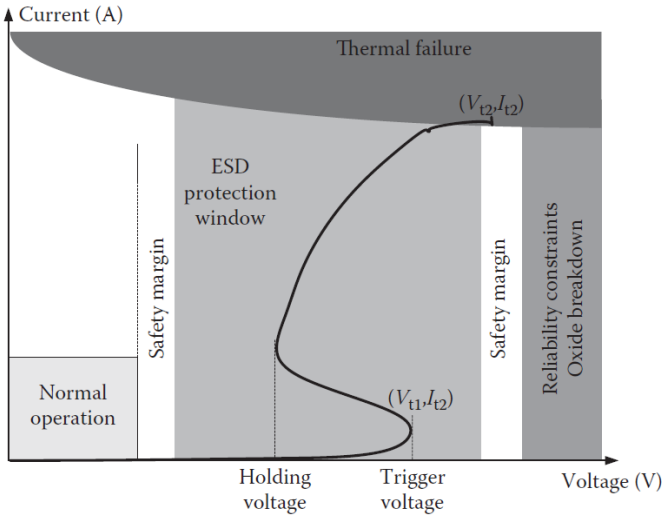

Figure 4: "Illustration of IC operating area, ESD design window, I–V curve of ESD protection device, and IC reliability constraint" [21][p. 4].

The concept of ESD protection must fulfill several requirements that must be considered. An ESD protection concept has to include the following points [21]:

1. In normal operation the ESD device must be turned off
2. In case of an ESD event, the ESD device must be switched from off to on-state. The switch-on of the ESD device must happen fast
3. The voltage level during ESD needs to be kept low enough to prevent the core circuitry from failing
4. The ESD device and the core circuit must not be damaged during an ESD event
5. After an ESD event the ESD device must be turned off again
6. The ESD protection device should be of small size, must draw low leakage current, and have high robustness

2.1.2 Snapback vs non-snapback devcies

In this chapter two types of ESD protection are discussed: Snapback and non-snapback devices [21]. In Figure 5 the I/V curves of the snapback and the non-snapback device are depicted. A snapback device has an operating window, determined by a lower and an upper bound. The lower bound is defined by the normal operating voltage (VDD) [21]. The highest voltage that the internal core circuitry may withstand without suffering damage defines the upper bound. [21]. The snapback device has a trigger voltage point V_{t1}, where the device is turned on, as presented in Figure 5. If the trigger voltage point is reached, the device is turned on and operates in the snapback region. As it is presented in Figure 5 (b) the voltage is reduced by the snapback and the power dissipation of the snapback ESD device is reduced as well [21]. The holding point is now reached, labeled with V_h. The curve represents the on-resistance from the holding point V_h upwards. If the voltage reaches the failure point V_{t2}, the ESD protection device is damaged. The group of snapback-type devices includes a Silicon-Controlled Rectifier (SCR), a Gate Grounded NMOS (GGNMOS), or a Gate Coupled NMOS (GCNMOS). The different devices will be explained in Chapter 2.1.3. A non-snapback device, like a forward-biased diode, is shown in Figure 5 (a). The trigger voltage point and the holding voltage point are the same. The non-snapback device must not reach the failure current and failure voltage to avoid damage to the ESD protection device.

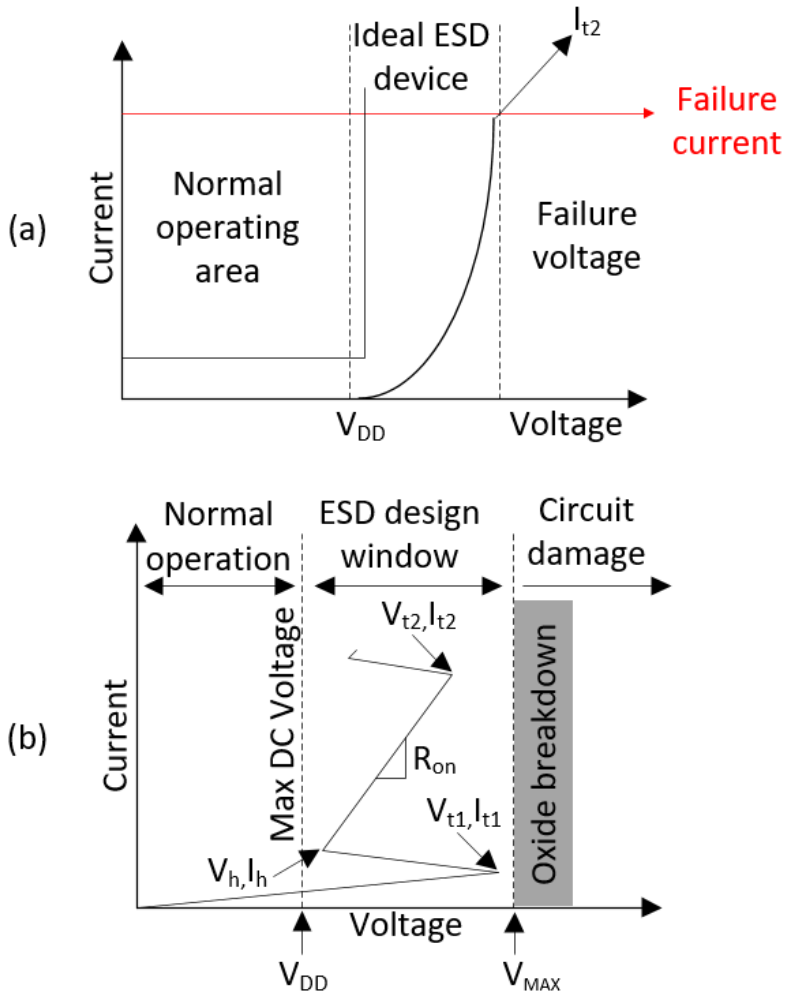

Figure 5: Difference of the I-V curve of (a) non-snapback and (b) snapback ESD device [21].

2.1.3 Protection Design Methodology

The main ESD protection concept includes a primary element, an isolation resistor and a secondary element, which is shown in Figure 7.

The ESD protection scheme should include a primary ESD protection, which is designed to dissipate the majority of the ESD current and a secondary ESD protection, which is used to prevent any gate-oxide damage on the transistors in the $DATA\_IN\_PATH$ [21]. In general, the primary protection triggers at a higher voltage than the secondary protection [21]. Between primary and secondary protection an isolation resistor is placed. This isolation resistor limits the current flowing to the secondary protection [21].

Various devices can be used to implement primary and secondary protection. The thesis focuses on the ESD protection components used in the I3C I/O. The primary protection is implemented by placing a diode. In addition to the diode, the output stage consists of an ESD PMOS and an NMOS transistor. A PMOS and an NMOS transistor with drain extension are used to operate at higher drain-source voltages [30]. The secondary protection is accomplished by a gate-grounded NMOS (GGNMOS). A GGNMOS goes into parasitic npn bipolar conduction in case of an ESD event [21]. The GGMOS triggers at V_{t1}, goes into snapback and carries the ESD current unit the failure point (V_{t2}, I_{t2}) is reached [21]. The I-V characteristic curve of a gate-grounded NMOS device is depicted in Figure 6. In addition to ESD protection for the I3C I/O, a power clamp is shown in Figure 7. To protect the power supply from an ESD event a supply clamp is implemented, using a snapback device.

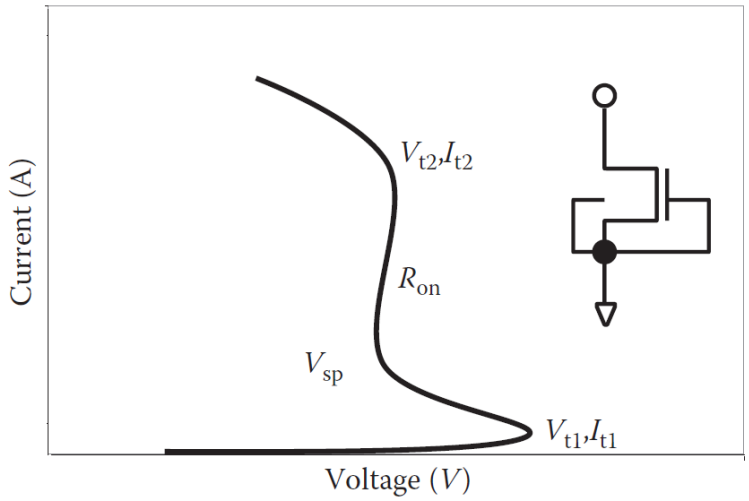

Figure 6: I-V curve of a gate-grounded NMOS transistor, used as a secondary ESD protection [21][p. 15].

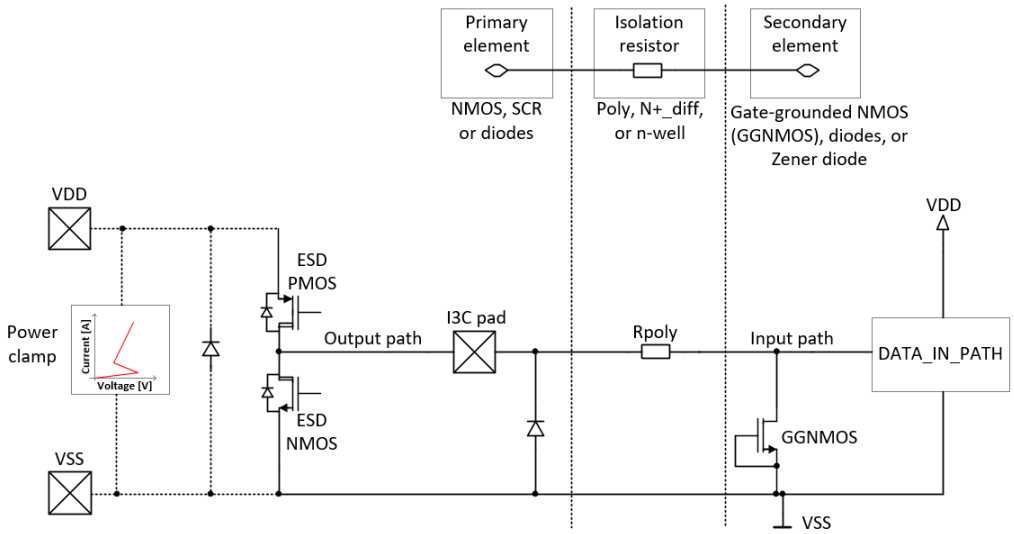

Figure 7: ESD protection concept.

An ESD network must provide a current path for a positive and negative discharge from the I3C I/O. The used approach is based on a V_{SS}-based ESD protection. A V_{SS}-based ESD protection shunts the current over the negative supply rail (V_{SS}). Since the I3C specification requires a failsafe functionality, no primary ESD protection against V_{DD} is allowed. Further details about the failsafe concept will be explained in Chapter 4.2.2.2.

The current paths for a positive and negative discharge from I/O to V_{DD} and I/O to V_{SS} are presented in Figure 8. Examining the current path I/O to V_{SS} for a positive discharge, the current will flow over the ESD NMOS device with drain extension to V_{SS}. The current path of a negative discharge I/O to V_{SS} just passes through the primary forward-biased ESD diode. The supply clamp is not involved. For a positive discharge from the I/O to V_{DD} the current flows via the ESD NMOS over the parallel diode of the power clamp to the V_{DD} pad. This approach follows the failsafe I/O concept rules since no current can flow over the back-to-back connected PMOS transistors. For a negative discharge from the I/O to V_{DD} the current path flows over the supply clamp and the diode to the PAD node.

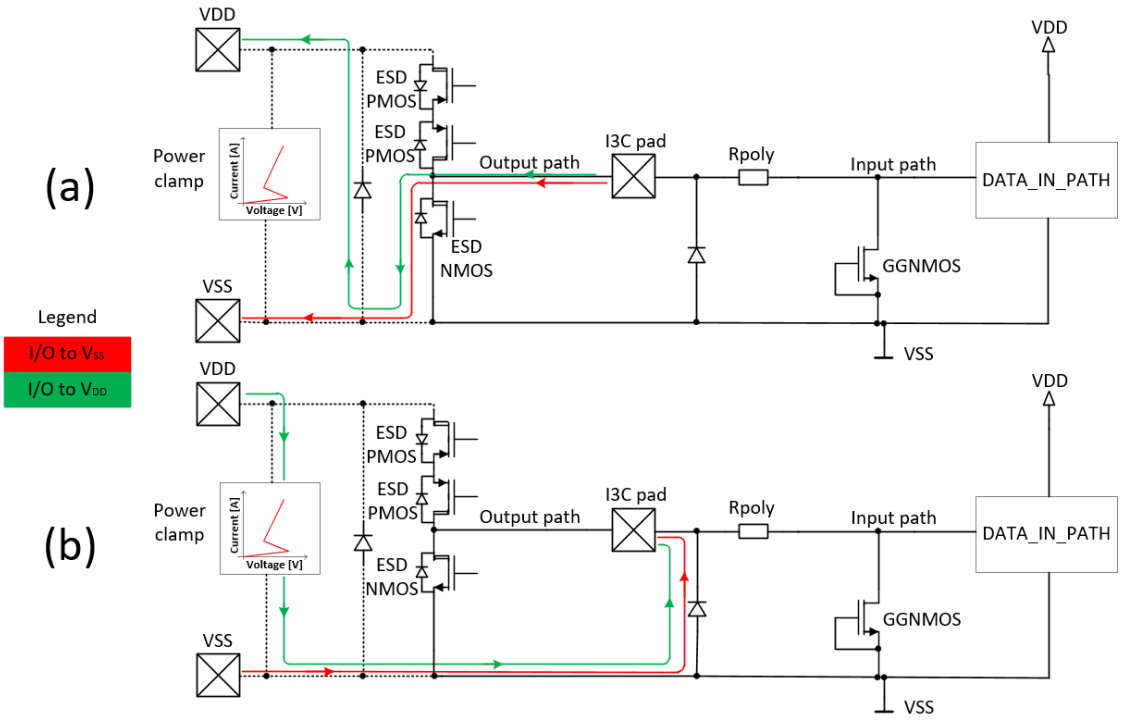

Figure 8: Current path for (a) positive and (b) negative discharge from the I3C I/O to V_{SS}.

2.2 Supply domain

The supply concept for this thesis can be divided into two parts. If the V_{BUS} equals 1.2 V, a supply concept, shown in Figure 9 can be used. The bus concept is split up into a supply domain to handle ESD events (*vddo*) and a peripheral supply domain (*vddr*). Those two domains have a star-point connection directly at the *VDD_1V2* pad. In the same manner, the *GND* concept is implemented. The output driver must be connected to the *vddo*/*gndo* supply since an ESD event can occur. In case of an ESD event, the *vddo*/*gndo* domain must be able to handle the high current. The second option is used when having a V_{BUS} = 3.3 V, depicted in Figure 10. In this case, the *vddo* supply is 3.3 V. The peripheral voltage *vddr3V3* is connected via a star point connection to the *VDD_3V3* pad. For the core voltage *vddr1V2*, a separate supply pad *VDD_1V2* is needed. The input Schmitt trigger accomplishes the transition between the *vddr3V3* and the *vddr1V2* domain. Since the core voltage is always at 1.2 V, all core elements like the Glitch filter or the Delay cell can be used for the 3.3 V and the 1.2 V option.

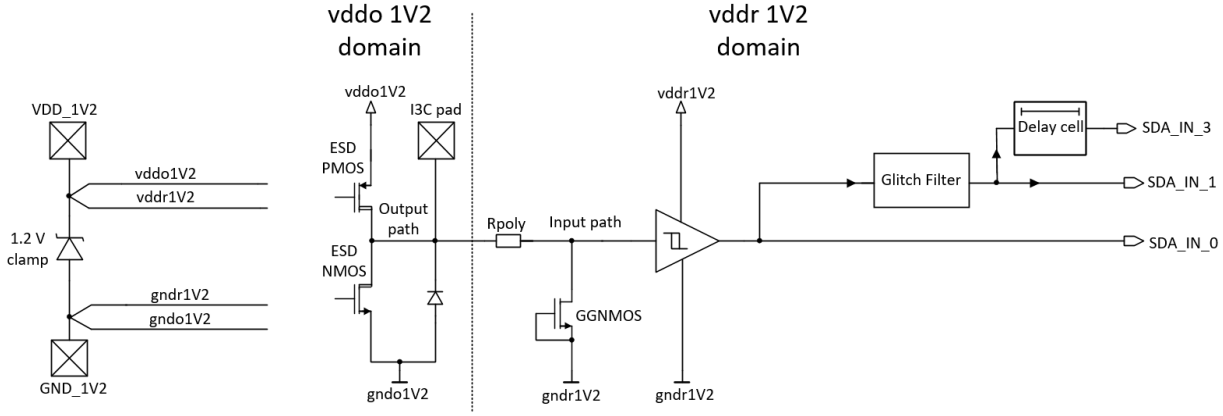

Figure 9: Supply concept for 1.2 V I/O options.

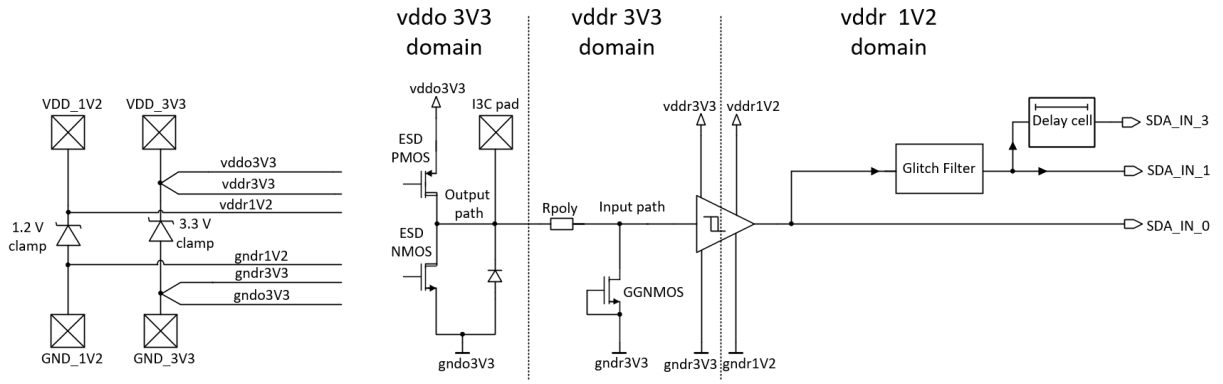

Figure 10: Supply concept for 3.3 V I/O options.

3 I2C/I3C Interface

The thesis will put its focus on the lowest level of abstraction, which is defined by the OSI model (Open System Interconnection). The OSI model was defined by the International Standards Organization and defines seven types of layers with functions, establishing communication over a network between computer systems [31]. The lowest level of this model is called the physical layer and defines the connection via electrical cables or wireless technology. On the physical layer, raw data is transmitted, which consists of 0s and 1s [31]. The second layer is called the data link layer. On the data link layer, the data formatting and data flow between nodes is defined. The data link layer also includes error detection and correction. Certain parts of the I2C protocol belong to different OSI layers. The data transfer of the I3C I/O structure happens on the physical layer because it deals with electrical characteristics. Particular features of the I2C interface operate on the data link layer, like the handshake process of I2C. Further details about the I2C protocol can be taken from the I2C specification [5]. An abstraction of the OSI seven-layer model is shown in Figure 11.
Several years ago, the I2C protocol was developed to address consumer electronics needs by offering a cheap way to connect a processor to several devices [9]. For this reason, I2C has been widely used in many industries [9]. In mobile applications, the I2C tradition continued, although the requirements for I2C were changing [9]. The I3C interface was created to address problems with sensor integration [9]. In addition to that, I3C provides a fast, low-cost cost, and low-power two-wire digital interface, which I2C, SPI, and UART could not serve [9]. The sensor classes addressed by I3C range from Time-of-Flight sensors, and ambient light sensors to heart rate sensors [9]. A general overview of the I3C bus structure is depicted in Figure 12. The bus includes a main I3C master device, I2C slave devices, a secondary I3C master device, and I3C slave devices. I3C is a two-wire bidirectional serial interface (SDA and SCL line) with a maximum operating frequency of 12.5 MHz using the Push-Pull configuration. Compared to I2C the speed improvements with I3C are more than ten times higher. Furthermore, I3C was developed to reduce power consumption by a factor of four or higher which is presented in Figure 13. The different I3C modes which are shown in Figure 13 are stated in the I3C specification as the following [9]:

- Single Data rate mode (SDR): A new enhanced version of the I2C protocol, operating in Push-Pull (I3C) or Open Drain (I2C) configuration, Data rate in I3C Push-Pull SDR of 11.11 Mbps
- I3C High data rate double data rate mode (HDR-DDR): Data and Commands change SDA on both SCL edges (rise and fall time), which effectively doubles the data rate to 22.22 Mbps
- High Data Rate Ternary Modes (HDR-TSP and HDR-TSL): Uses ternary signaling on the two wires. Ternary signaling uses three possible transitions: Only SCL changes, Only SDA changes or SCL and SDA change
  The data maximum data rate of I3C is 33.37 Mbps in HDR-TSP mode

Legacy I2C devices are still supported by the I3C interface and can be operated on the same bus with limitations [9]. If an I2C device is used on an I3C bus, the operating frequency is limited to the maximum frequency of the I2C device [9]. Since the master

thesis deals with the implementation of a modular I/O structure, the I3C/I2C protocol will not be explained in this thesis. Detailed information can be found in the official I2C specifications of NXP [5] and in the I3C specification from MIPI [9].

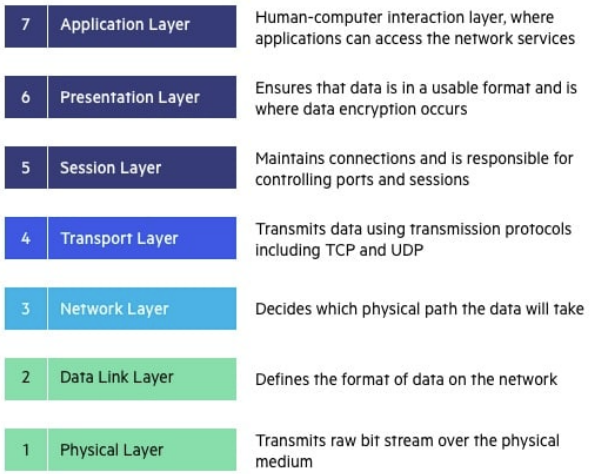

Figure 11: Abstraction of the seven OSI layer model [32].

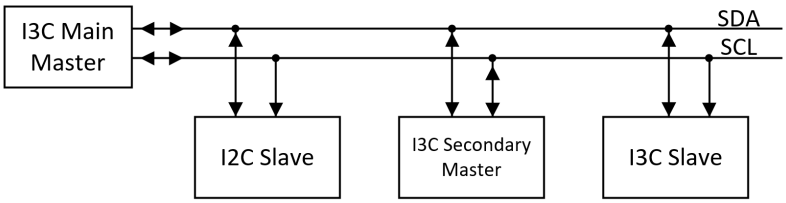

Figure 12: Abstraction of the I3C bus.

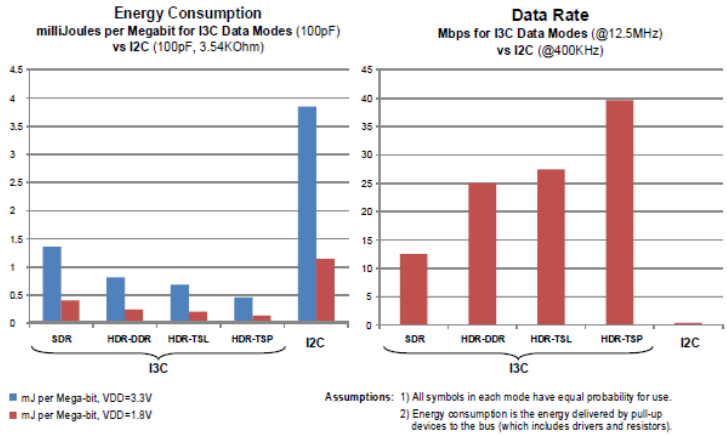

Figure 13: Energy Consumption and Raw Data Rate: I3C vs I2C [10].

Heading to the technical implementations, one of the major changes from I2C to I3C is the output driver. I2C uses an open drain NMOS transistor which requires an external Pull-up resistor to the bus supply voltage. The I2C NMOS transistor must be able to pull down the I2C bus to the required low-level voltage (V_{OL}), which is stated in the I2C specification [5]. An example of the I2C bus with Pull-up resistors and an open drain output driver is depicted in Figure 14. In addition to the Pull-up resistors, the bus has a capacitance, consisting of wires, connections, and the input capacitance of each slave device. The maximum load capacitance is stated in the I2C specification [5] and is required to calculate the maximum Pull-up resistance. The maximum Pull-up resistance can be calculated from the RC time constant. For this consideration, the bus voltage is related to the input thresholds of $V_{IH} = 0.7 \cdot V_{BUS}$ and $V_{IL} = 0.3 \cdot V_{BUS}$ [5]. To fulfill the rise time specification, the following formula must be applied from the I2C specification [5]:

$$
\begin{aligned}
V(t1) = 0.3 \cdot V_{BUS} &= V_{BUS}\left(1 - e^{\frac{-t1}{RC}}\right); t1 = 0.357 \cdot RC, \\
V(t2) = 0.7 \cdot V_{BUS} &= V_{BUS}\left(1 - e^{\frac{-t2}{RC}}\right); t2 = 1.204 \cdot RC, \\
T = t2 - t1 &= 0.8473 \cdot RC, \\
R_{p(max)} &= \frac{tr}{0.8473 \cdot C_{BUS}}.
\end{aligned}
\tag{1}
$$

I3C uses a Push-Pull output driver which is presented in Figure 15. The Push-Pull driver enables the bus to pull the network without additional Pull-up resistors to V_{BUS} via the PMOS transistor and can pull down the I3C bus to V_{SS} via the NMOS transistor. The two operating modes can be viewed in Figure 15.

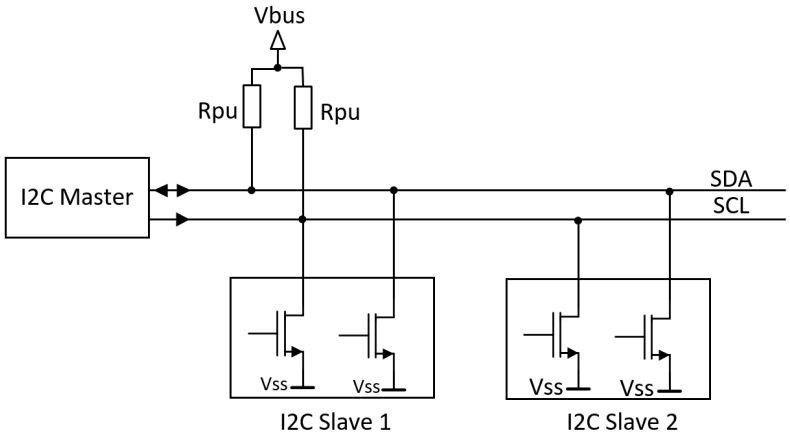

Figure 14: I2C bus with open drain outputs and Pull-up resistors [10].

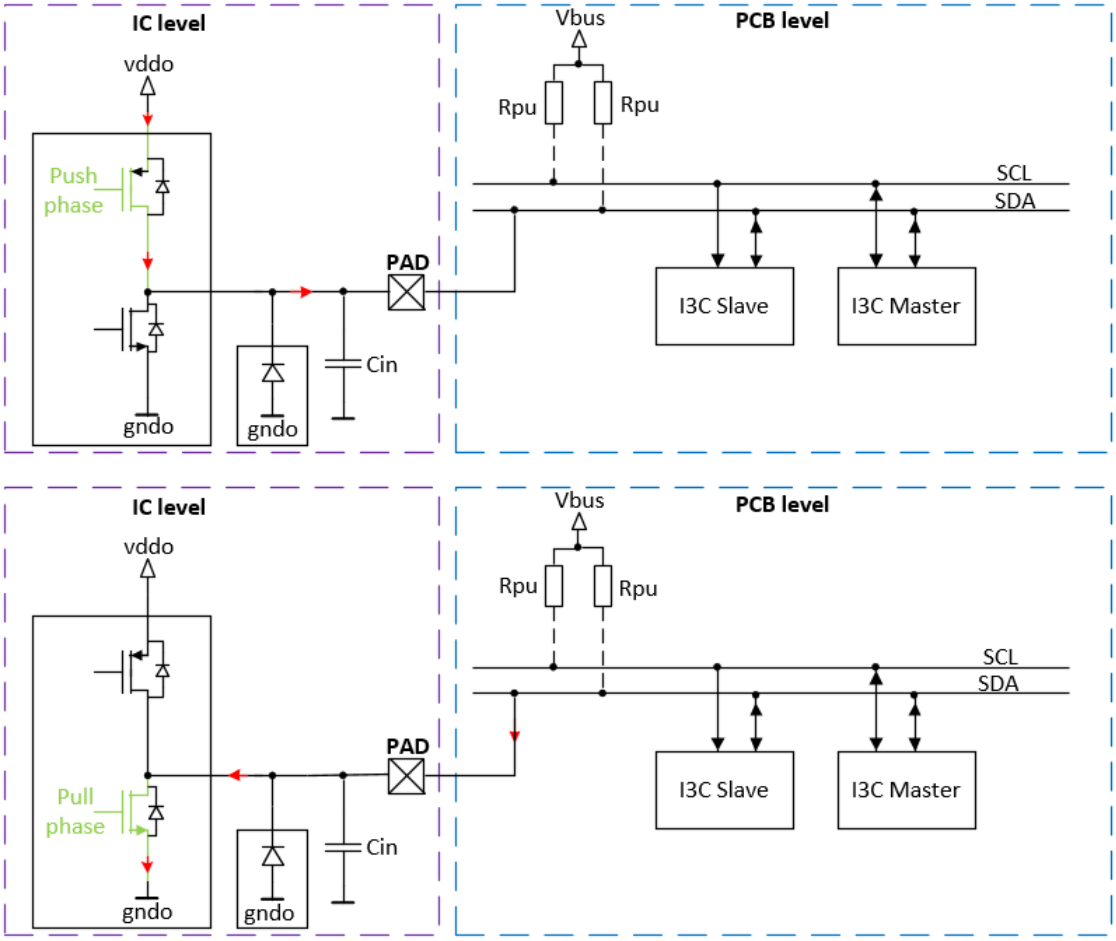

Figure 15: I3C output driver in (a) Push mode and (b) Pull mode.

3.1 Timing parameters

In this chapter, the most important timing parameters are explained. The first parameter is the propagation delay for a rising (t_{plh}) and a falling edge (t_{phl}). The propagation delay is determined between $0.5 \cdot Vin$ and $0.5 \cdot Vout$, which is depicted in Figure 16. In addition to this, an input signal from $V_{IL} = 0.3 \cdot V_{BUS}$ to $V_{IH} = 0.7 \cdot V_{BUS}$ can occur on the bus. The timing diagram for such an input signal is shown in Figure 17.

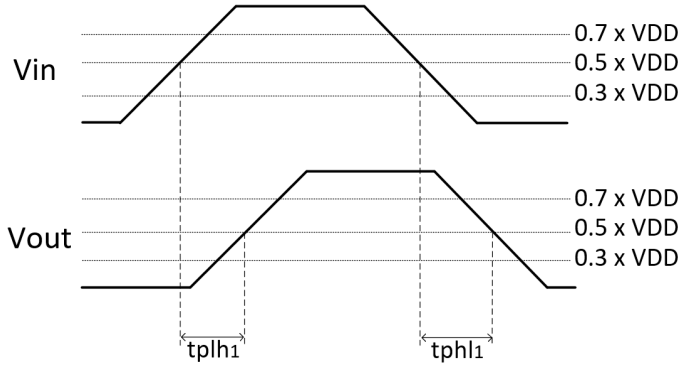

Figure 16: Visualization of the propagation delay for an input signal (Vin) from VSS to *VDD*.

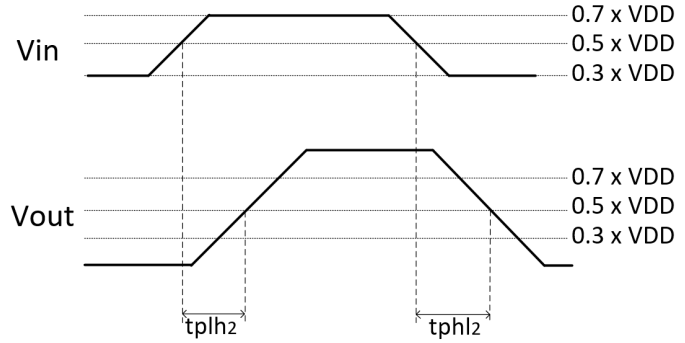

Figure 17: Visualization of the propagation delay for an input signal (Vin) from $0.3 \cdot VDD$ to $0.7 \cdot VDD$.

Another important timing parameter for this thesis is the roundtrip delay t_{sco}, officially named *Clock in to Data Out for Slave*. The roundtrip-delay path leads from the *SCL* pad over the input path of the I3C I/O, to the digital core, and finally over the I3C I/O output path to the *SDA* pad, which is shown in Figure 18. The t_{sCO} delay is illustrated in Figure 19. t_{sco_high} is defined by 30 % of the falling edge of *SCL* to 0 % of the rising edge of *SDA*. t_{sco_low} is defined by 30 % of the falling edge of *SCL* to 100 % of the falling edge of *SDA*. Similarly, the I2C specification has a round trip delay parameter, known as the data valid time t_{VD}. The definition of t_{vd} is depicted in Figure 20.

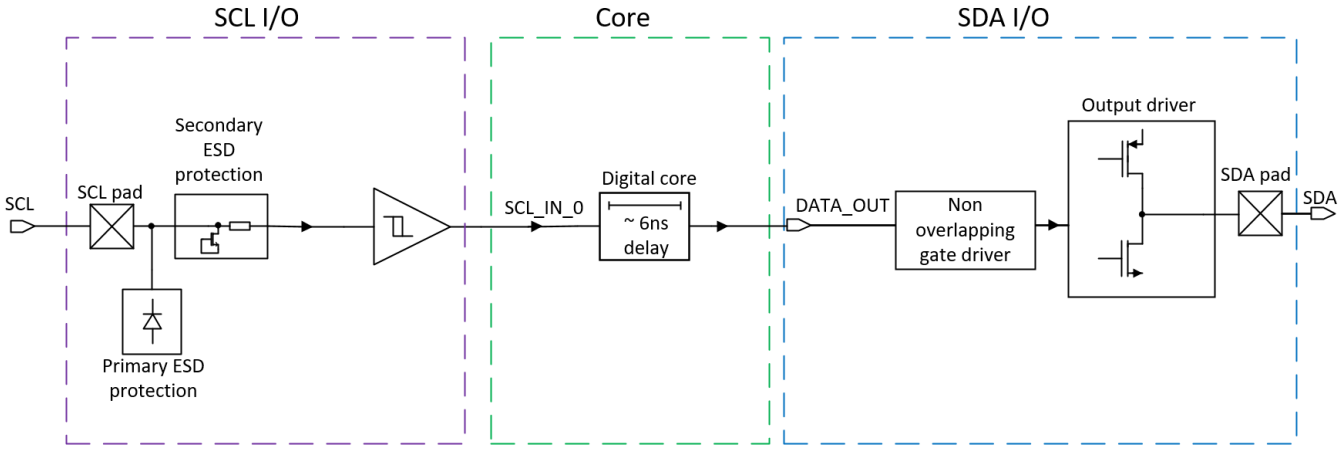

Figure 18: Data path of the I3C roundtrip delay.

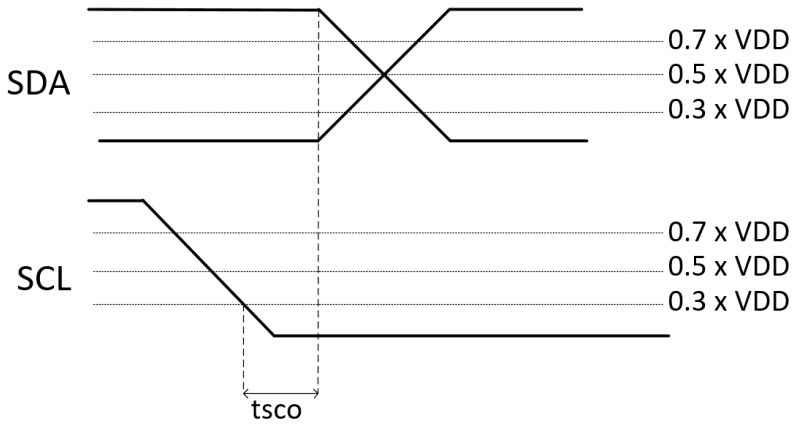

Figure 19: Timing diagram of the I3C roundtrip delay.

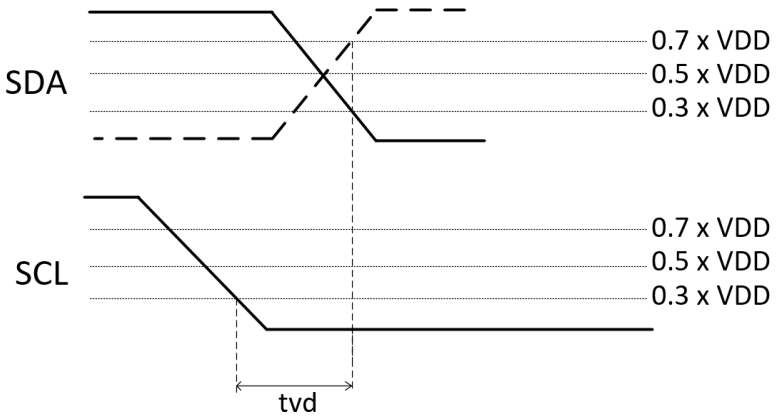

Figure 20: Timing diagram of the I2C data valid time.

4 I2C/I3C I/O Cell topology

4.1 Block diagram

In order to get a better understanding of the I/O structure, a block diagram is shown in Figure 21. This block serves only as a rough overview and contains no specific details of the individual blocks. All blocks will be described in the Chapters 4.2.1 and 4.2.2. The block diagram is mainly divided into 2 parts: a *DATA_IN_PATH* and a *DATA_OUT_PATH*. The input signal comes from the SDA/SCL line to the PAD node. After that, the signal is fed into the ESD protection block. The input data is processed by a modular *IN* block. The output of the modular *IN* block is directly connected to *SDA_IN_0* pin. The output of the *IN* block is connected to a Glitch filter block. The output of the glitch filter block is called *SDA_IN_1*. *SDA_IN_1* is tied to the input of a delay block. The output of the delay block is labeled with *SDA_IN_3*. Via the three input signals *SDA_IN_0*, *SDA_IN_1* and *SDA_IN_3* data from the I3C/I2C bus can be received.
Transmitting data can be accomplished via the *DATA_OUT_PATH*. Dedicated output data is sent to a non-overlapping gate driver. The output of the non-overlapping gate driver is connected to a modular *OUT* block. After the modular output block *OUT* an ESD diode is placed.

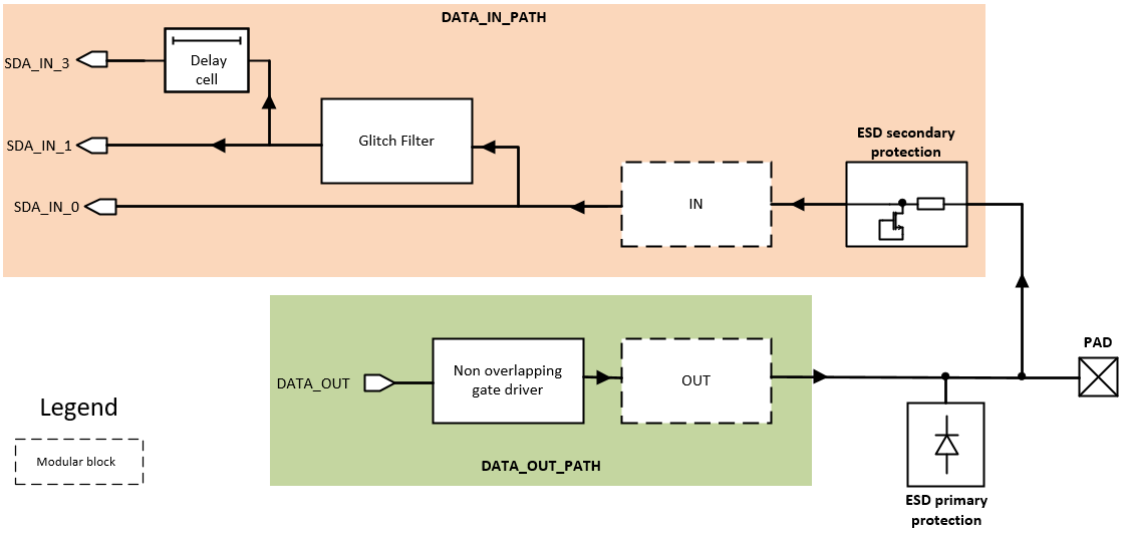

Figure 21: Block diagram of a modular I3C I/O.

4.2 Idea of the Modularity Principle

Modular systems have the big advantage of being flexible, quickly integrated, and independent of other modules in a bigger system. Modular systems are not only useful in our everyday lives, they can also be a big advantage in IC design. A modular approach can shorten the time to market or increase the flexibility to meet customer requirements. The modular blocks, shown in Figure 21, were designed in the following manner. First, a detailed analysis of the MIPI specification [9] and the I2C specification [5]. After this analysis, the block diagram was created, which is presented in Figure 21. At this point, a representation of combining these blocks must be developed. For this reason, a permutation matrix is introduced in Table 1. The permutation matrix is the starting point of generating the different I3C I/O combinations. The column names and the row names of this matrix are identical. A possible combination can be read from top to bottom or from left to right. If a parameter is valid for a certain combination, the field is marked with an X, otherwise the field is blank. The listed parameters in the permutation matrix are explained more precisely in Chapters 4.2.1 and 4.2.2. A short explanation of the parameter names used in the permutation matrix are given in the following list:

- V_{BUS}: The I3C bus voltage
- Pure I2C: I2C I/O without I3C functionality
- Pure I3C: I3C I/O without I2C backward compatibility
- I2C Delay: Include Glitch filter and Delay block
- Fm+ (Fast Mode Plus): Support of I2C Fm+ mode and Fm mode
- Fm (Fast Mode): Support of I2C of Fm mode only
- V_{BUS} available separate V_{DDIO} pin: Ensures inherent failsafe functionality
- Failsafe circuit required: An additional circuitry is necessary to ensure failsafe functionality in case V_{DDIO} is not available
- V_{DDR}: Peripheral supply domain

The number of combinations would be enormous. Therefore a reduction of the combinations is necessary. The relevant combinations are listed in Table 2 concerning functionality, die area, and cost. The presented combinations in table 2 can be implemented with the modular blocks, presented in Figure 22 and the non-modular blocks, shown in Figure 21. In total, three modular IN blocks and four modular OUT blocks can be viewed in Figure 22. The modular IN block is exchanged by an input Schmitt trigger, with different supply voltages (VDD) and bus voltages (V_{BUS}). The content of the black box OUT can include an I3C failsafe output driver, an I3C non-failsafe output driver, or an I3C inherent failsafe output driver. The Fm+ block can extend the other three OUT blocks, to make the I3C I/O compatible with the I2C Fm+ mode. In the Chapters 4.2.1 and 4.2.2 the content of the modular and non-modular blocks will be described in more detail.

	$V_{BUS} = 1.2$ V	$V_{BUS} = 1.8$ V	$V_{BUS} = 3.3$ V	Pure I2C	Pure I3C	I2C Delay	Fm+	Fm	V_{BUS} available via V_{DDIO} Pin	Failsafe circuit required	$V_{DDR} = 1.2$ V	$V_{DDR} = 1.8$ V	$V_{DDR} = 3.3$ V
$V_{BUS} = 1.2$ V	X			X	X	X	X	X	X	X	X	X	X
$V_{BUS} = 1.8$ V		X		X	X	X	X	X	X	X	X	X	X
$V_{BUS} = 3.3$ V			X	X	X	X	X	X	X	X	X	X	X
Pure I2C	X	X	X	X	X	X	X	X	X	X	X	X	X
Pure I3C	X	X	X	X	X	X	X	X	X	X	X	X	X
I2C Delay	X	X	X	X	X	X	X	X	X	X	X	X	X
Fm+	X	X	X	X	X	X	X	X	X	X	X	X	X
Fm	X	X	X	X	X	X	X	X	X	X	X	X	X
V_{BUS} available via V_{DDIO} Pin	X	X	X	X	X	X	X	X	X	X	X	X	X
Failsafe circuit required	X	X	X	X	X	X	X	X	X	X	X	X	X
$V_{DDR} = 1.2$ V	X	X	X	X	X	X	X	X	X	X	X	X	X
$V_{DDR} = 1.8$ V	X	X	X	X	X	X	X	X	X	X	X	X	X
$V_{DDR} = 3.3$ V	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 1: Permutation matrix with modular (green) and non-modular (yellow) combinations.

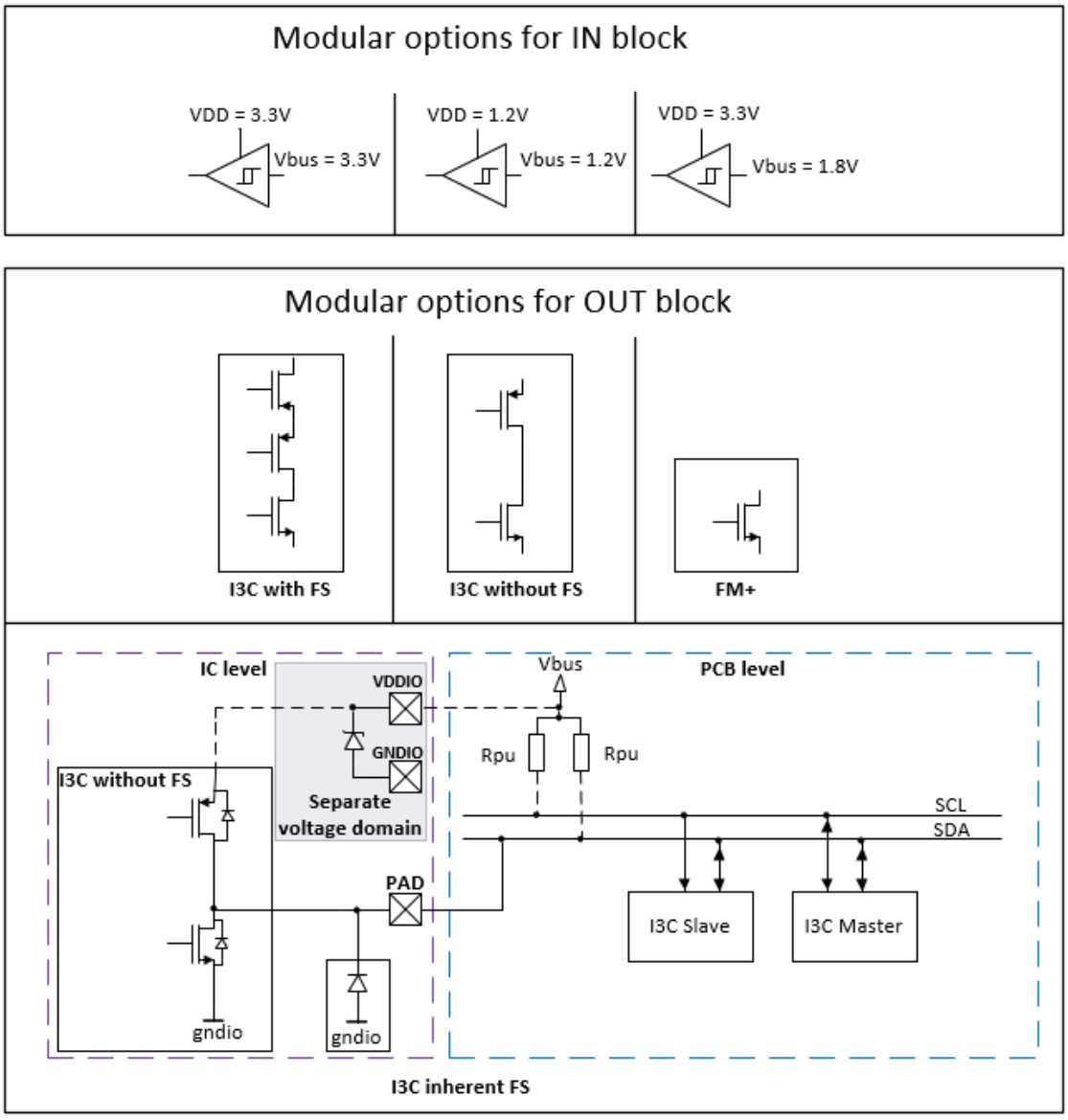

Figure 22: Overview of the modular blocks.

Fm	*VDD*	I3C_Fm_3V3	I3C I/O which is I2C Fm compatible operating at V_{BUS} = *VDD* = 3.3 V
		I3C_Fm_1V2	I3C I/O which is I2C Fm compatible operating at V_{BUS} = *VDD* = 1.2 V
	V_{BUS}	I3C_Fm_3V3_V_B3V3	I3C I/O which is I2C Fm compatible. V_{BUS} is available via a separate *VDDIO* Pin, *VDD* = 3.3 V and V_{BUS} = 3.3 V
		I3C_Fm_1V2_V_B1V2	I3C I/O which is I2C Fm compatible. V_{BUS} is available via a separate *VDDIO* Pin, *VDD* = 1.2 V and V_{BUS} = 1.2 V
		I3C_Fm_3V3_V_B1V8	I3C I/O which is I2C Fm compatible. V_{BUS} is available via a separate *VDDIO* Pin, *VDD* = 3.3 V and V_{BUS} = 1.8 V
Fm+	*VDD*	I3C_Fm+_3V3	I3C I/O which is I2C Fm+ compatible operating at V_{BUS} = *VDD* = 3.3 V
		I3C_Fm+_1V2	I3C I/O which is I2C Fm+ compatible operating at V_{BUS} = *VDD* = 1.2 V
	V_{BUS}	I3C_Fm+_3V3_V_B3V3	I3C I/O which is I2C Fm+ compatible. V_{BUS} is available via a separate *VDDIO* Pin, *VDD* = 3.3 V and V_{BUS} = 3.3 V
		I3C_Fm+_1V2_V_B1V2	I3C I/O which is I2C Fm+ compatible.V_{BUS} is available via a separate *VDDIO* Pin, *VDD* = 1.2 V and V_{BUS} = 1.2 V
		I3C_Fm_3V3_V_B1V8	I3C I/O which is I2C Fm+ compatible. V_{BUS} is available via a separate *VDDIO* Pin, *VDD* = 3.3 V and V_{BUS} = 1.8 V

Table 2: List of the reduced number of I/O options.

4.2.1 Input Structure

After the secondary ESD protection, the input structure is used for reading the input data from the I3C bus. This chapter will provide the required theoretical knowledge for all associated blocks.

4.2.1.1 Schmitt trigger

The Schmitt trigger is the first modular block that will be discussed. This chapter goes into more detail about why Schmitt triggers are needed, how a Schmitt trigger operates, and which aspects must be considered before starting the design of the Schmitt trigger.

4.2.1.2 Introduction to Comparators

First and foremost, this chapter will examine the input path of an I3C I/O. The first section describes the analog-to-digital conversion of the input signal, coming from the outside world. Such an analog-to-digital conversion can be accomplished with a comparator [18]. A comparator uses a reference analog voltage and compares it with the analog input signal [18]. This analog-to-digital conversion is relevant, providing a valid digital logic level to the core circuitry [12]. The comparator is depicted in Figure 23 and has a positive input v_p and a negative input v_n and a dedicated output v_O. If the voltage difference between v_p and v_n is positive, the output voltage v_O is raised to the output high voltage V_{OH} [18]. If the voltage difference between v_p and v_n is negative, v_O will be set to the output low voltage V_{OL}, as it is shown in Figure 24. The voltage level where the output switches from V_{OL} to V_{OH} and vice versa, is defined by a single threshold voltage.

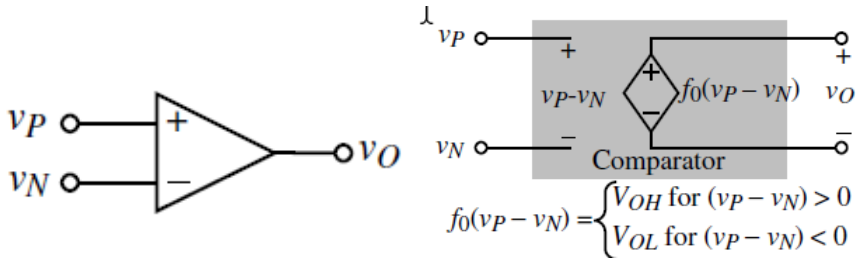

Figure 23: Comparator symbol (left) and the comparator model (right) [18].

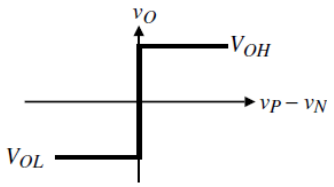

Figure 24: Ideal transfer curve of a comparator [18].

4.2.1.3 Challenges with Comparators

As presented in Chapter 4.2.1.2, the transition between the analog and digital world is accomplished via comparators. Since comparators possess a single threshold, they have certain limitations. Analog input signals are not entirely noiseless. If a noisy input signal is applied to the input of a comparator, the output voltage will bounce between the two rails V_{OL} and V_{OH}, shown in Figure 25 (left). This instability can cause failures in the internal core circuitry. Due to this limitation, an improved approach must be considered. This improvement can be achieved with a Schmitt trigger circuit.

Schmitt triggers are used to generate clean pulses from noisy input signals [15]. The main difference between Schmitt triggers and comparators is the transfer curve. Unlike the standard comparator, the Schmitt trigger has two different threshold voltages for rising and falling transition, which is depicted in Figure 26. If the input voltage reaches V_{TH_LH}, the output voltage is raised to V_{OH}. When the input voltages drop again under V_{TH_HL}, the output voltage drops to V_{OL}. The hysteresis is defined as the difference between V_{TH_LH} and V_{TH_HL}, which is an important parameter in the I3C specification from MIPI [9].

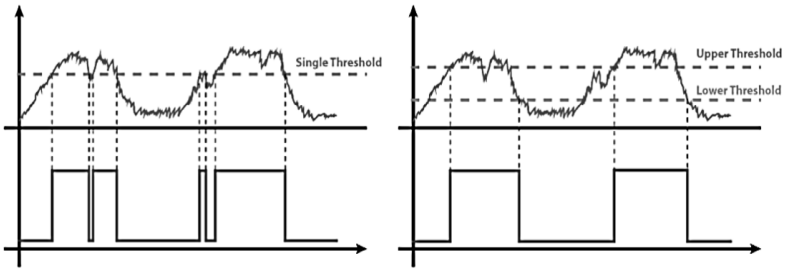

Figure 25: Comparison of an output signal without hysteresis (left) and with hysteresis (right) [33].

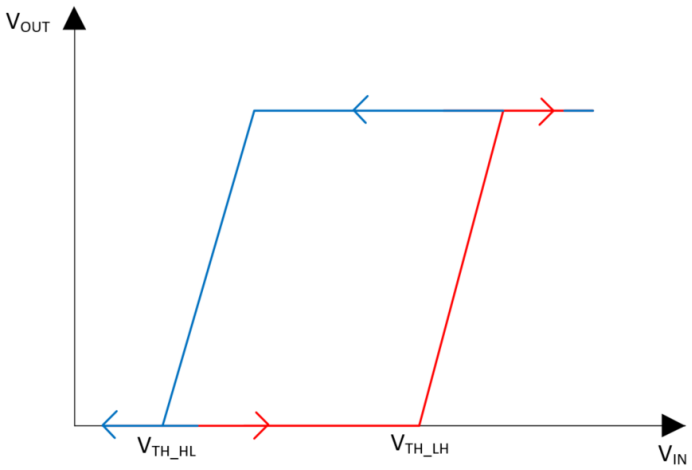

Figure 26: Transfer curve of a Schmitt trigger.

4.2.1.4 Schmitt trigger circuits

In this chapter, the Schmitt trigger circuit will be analyzed. The applied Schmitt trigger concept was first mentioned by M. Filanovsky and H. Bakes [16]. The traditional design of M. Filanovsky and H. Bakes uses a regenerative resistive feedback amplifier [16]. The proposed design is widely spread in the industry. Additionally, the threshold voltages can be adapted precisely and demonstrate good temperature behavior. In contrast to the applied implementation of [16], a variant with CMOS (Complementary Metal Oxide Semiconductor) inverters and positive feedback is presented in [17]. Furthermore, a widely used design is explained in [17], where two inverters are used with two feedback transistors. The design flow for the Schmitt trigger with regenerative resistive feedback is based on the book of R. Baker [15].

4.2.1.5 Regenerative resistive feedback amplifier

Subsequently, the circuit of [16] will be examined in this chapter. The circuit depicted in Figure 27 can be divided into two separate parts. V_{OH} is limited by the upper rail (VDD), whereas V_{OL} is limited by the lower rail (VSS) [15]. Assuming the input voltage v_{in} starts at 0 V and the state of the node *outn* is currently VDD. M3 is turned on and will keep the voltage node v_N at VDD - V_{THN} [15]. If a voltage ramp is applied to the input node, M1 will start turning on [15]. The V_{TH_LH} for the Schmitt trigger is defined by:

$$V_{IN} = V_{TH\_LH} = V_{THN2} + V_N, \tag{2}$$

at which point the transistor M2 starts to turn on [15]. M2 starts turning on and at the same time, M3 will start turning off. If M2 is fully turned on and the output node is pulled to VSS, M3 is completely turned off [15]. Since a non-inverting function is required, an inverter is conducted behind *out*. In the same manner, the threshold voltage V_{TH_HL} is defined by the upper part of the circuit, shown in Figure 27. The threshold voltage is very well defined by the positive feedback [15].

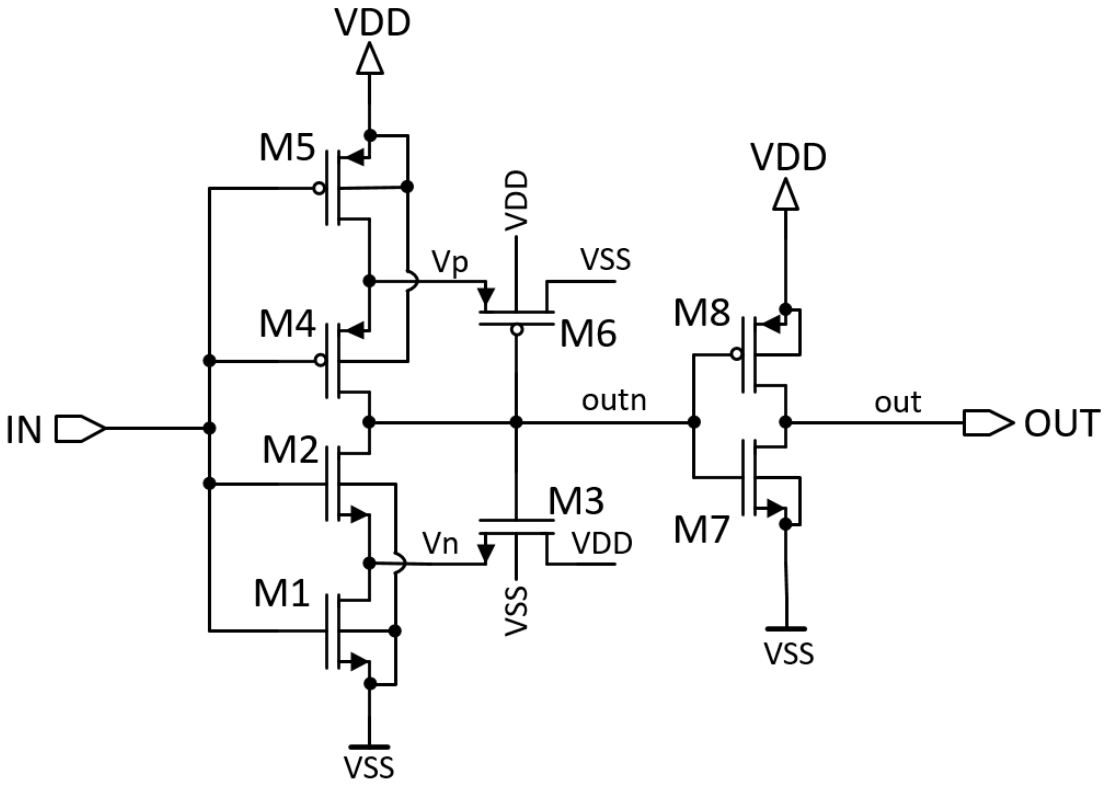

Figure 27: Schematic of the Schmitt trigger circuit.

Regarding the transistor sizing, (2) must be considered. If the DC operating point of (2) is reached, the current flowing through the transistor M1 and M3 is the same [15]. Equating the currents, the following is obtained: [15]

$$\frac{\beta_1}{2}(V_{TH\_LH} - V_{THN1})^2 = \frac{\beta_3}{2}(VDD - V_N - V_{THN3})^2. \tag{3}$$

Since the sources of M2 and M3 are tied together, the threshold voltage V_{THN2} equals V_{THN3} [15]. For this reason, the body effect for M2 and M3 can be neglected [15]. The combination of (2) and (3) lead to:

$$\begin{aligned}
\frac{\beta_1}{\beta_3} &= \left[\frac{VDD - V_N - V_{THN3}}{V_{TH_LH} - V_{THN1}}\right]^2, \\
\frac{\beta_1}{\beta_3} &= \left[\frac{VDD - V_N - V_{TH_LH} + V_{THN2} - V_{THN3}}{V_{TH_LH} - V_{THN1}}\right]^2, \\
\frac{\beta_1}{\beta_3} &= \left[\frac{VDD - V_N - V_{TH_LH}}{V_{TH_LH} - V_{THN1}}\right]^2.
\end{aligned} \tag{4}$$

In the same manner, the equations for the threshold voltage V_{TH_HL} can be derived [15]. The transistor ratios for V_{TH_HL} can be expressed as the following:

$$\frac{\beta_5}{\beta_6} = \left[\frac{V_{TH\_HL}}{VDD - V_{TH\_HL} - V_{THP5}}\right]^2. \tag{5}$$

As M2 and M4 act like a normal switch, the R_{ON} resistance must be as small as possible. This small R_{ON} can be achieved by increasing the ratio $\frac{W}{L}$ of transistors M2 and M4. The formula of R_{ON} is derived in (6).

$$I_{DS} = \beta\left[(V_{GS} - V_{th})V_{DS} - \frac{{V_{DS}}^2}{2}\right] \quad ; \quad 0 < V_{DS} < V_{GS} - V_{th} \quad \text{linear region,}$$
$$R_{on} = \frac{\mathrm{d}V_{DS}}{\mathrm{d}I_{DS}} = \frac{1}{\frac{W}{L} \cdot (V_{GS} - V_{th} - V_{DS}).} \tag{6}$$

Switching Characteristics
The propagation delay of the Schmitt trigger is an important specification parameter. The propagation delay is mainly dependent on the resistance of M1, M2, M4, and M5 [15]. The resistance of those transistors can be adjusted by the channel length, as shown in (6). The propagation delay time, neglecting the propagation delay of the inverter, can be expressed with (7). The load capacitance consists of the gate capacitances of M3, M6, M7, and M8. The propagation delay for the rising/falling edge can be expressed as the following:

$$\begin{aligned} t_{PHL} &= (R_{n1} + R_{n2}) \cdot C_{load}, \\ t_{PLH} &= (R_{p4} + R_{p5}) \cdot C_{load}, \\ C_{load} &= C_{G3} + C_{G6} + C_{G7} + C_{G8}. \end{aligned} \tag{7}$$

Layout Dependent Effect (LDE)
As introduced, this thesis will only be a feasibility study and will not include any layout activities. Nevertheless, layout-dependent effects have to be taken into consideration, when this work is brought to silicon. As this is a plan for future work, to use the proposed design on a testchip, these layout considerations are necessary. In submicron CMOS processes, layout-dependent effects (LDE) alter the device performance [34]. "The well-proximity effect (WPE) is a major cause of LDE" [34, p. 3822]. "During the high energy ion implantation of the wells, parts of the ions laterally scatter from the edge of the photoresist into the well and embed in the silicon surface" [34, p. 3822]. This scattering from the edge is presented in the Figure 28. The high ion concentration leads to a gradient near the well edge [34]. The MOSFET geometrics are influenced [34]. An important CMOS parameter is the threshold voltage. Usually, the doping concentration across the transistor is constant [34]. In the region close to the well edge the doping concentration is higher,

which is presented in Figure 28. Assuming the acceptor concentration N_A in the doped region is constant across the transistor [34]. Since the doping concentration near the well edge is higher, V_{TH} is influenced [34]. In Figure 29 the layout of an NMOS transistor with the well edge distance d1 is shown. ΔV_{TH} increases when the well edge distance d_1 decreases, due to WPE [34]. The second investigation is the impact of the width of the transistor, depicted in Figure 29. The impact on V_{TH} of the higher doping concentration is less significant for wider transistors [34]. Dummy transistors are displayed, to introduce an additional distance to the well edge. As an example, dummy transistors are placed around matching structures, like a current mirror [35]. Dummy transistors help to ensure that the current mirror has the same geometry when etched in silicon [35].

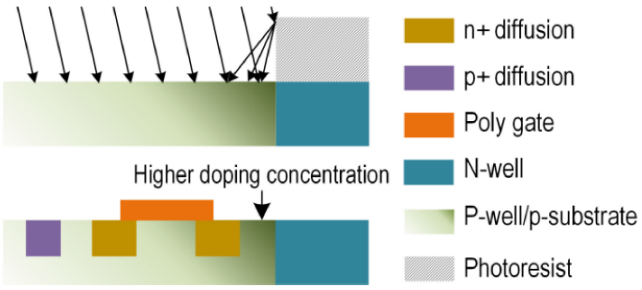

Figure 28: "Illustration of WPE on NMOS. The color gradient of the P-well highlights the ion concentration profile. The region close to the well edge has a higher doping concentration" [34][p. 3823].

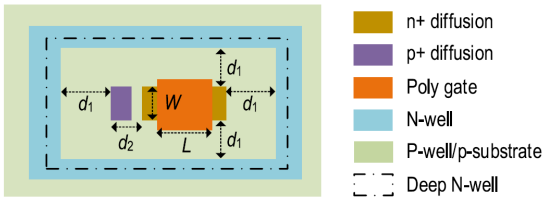

Figure 29: "Layout of the NMOS in deep N-well" [34][p. 3823].

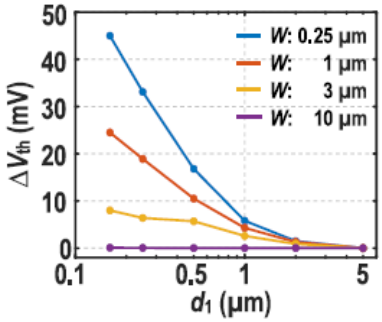

Figure 30: "The NMOS's ΔV_{TH} (referenced to d1 = 5 µm in each case) versus d1 with various W (L = 3 µm) at room temperature in the selected 65 nm CMOS process" [34][p. 3823].

4.2.1.6 Glitch Filter

The need for glitch-free devices is increasing all the time, especially when considering IoT or cloud computing [25]. Devices communicate using specific protocols [25]. If an error in signal integrity occurs, an error can have an impact on all these devices [24]. Related to this thesis, a flaw in signal integrity can cause a misinterpretation of data. To guarantee this signal integrity, glitch-free devices are demanded. "A glitch is any unneeded signal transition in the system, which can occur because of switch bounce, slow switching signals, or noise." [25][p. 259]. Glitches can cause problems if a logic block is affected or the glitch is stored by a latch [25]. In addition, glitches have an impact on the power consumption [25]. The reason for this is the additional charging/discharging of gate capacitances [25]. A way to handle glitches is to remove them before they affect the system [25]. This is the reason, why a glitch filter is introduced. A way to perform glitch filtering is accomplished by using an RC filter in combination with a simple CMOS inverter [25]. "Glitch filtering is the process of eliminating undesirable pulses of narrow width from an input signal while allowing the passage of pulses of larger width"[25][p. 259]. The input signal is delayed by the glitch filter circuit. This additional delay should be as small as possible and the same for the rising and falling edge of an input signal [24]. If the propagation delay of rising and falling edges is different, the duty cycle is distorted [24]. The very simple glitch filter approach with two inverters and an RC circuit is presented in the left schematic of Figure 31. The input signal IN is applied to an inverter, which is connected to the RC network formed by the resistor R_0 and a MOS capacitor C_{M1} [24]. The RC circuit has a given time constant $\tau = R_0 \cdot C_{M1}$. The RC circuit is attached to a second inverter, which has a certain threshold voltage. When an input glitch with a pulse width less than a certain threshold is applied, the MOS capacitor is not charged sufficiently [24]. The voltage at node *rcn* is smaller than the threshold voltage of the output inverter [24]. The high-frequency glitch has been filtered [24].

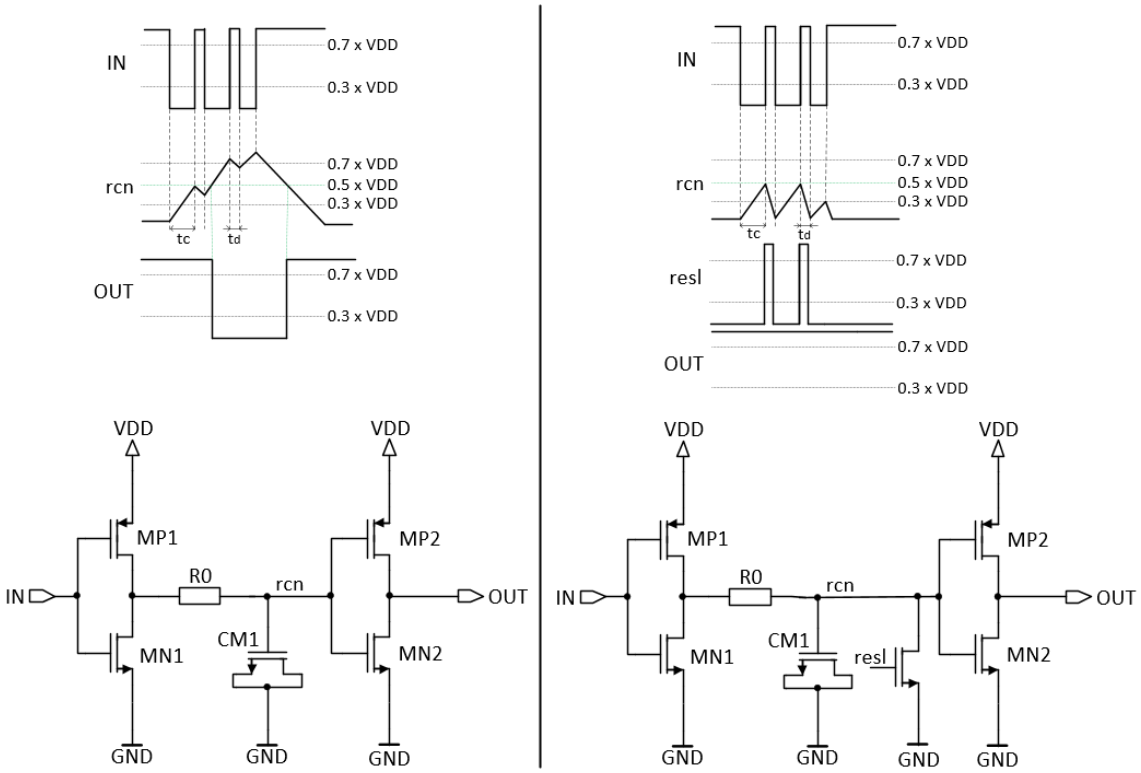

Figure 31: Multiple glitches applied to a basic glitch filter circuit without reset mechanism (left) and with reset mechanism (right).

4.2.1.6.1 Proposed glitch filter circuit

Subsequently, the used circuitry in this thesis is slightly different. Hence, the left circuit shown in Figure 31 has some limitations. The issue of this circuit is, that multiple glitches close together can not be filtered with this basic circuit. If multiple glitches occur in a row, the internal node *rcn* can not be discharged to *GND*, which is shown in Figure 31 (left). The charge time is labeled with *tc* and the discharge time is labeled with *td*. In Figure 31 (left) *td* is too short for the voltage node *rcn* to discharge to *GND*. The node *rcn* will be consecutively increased by the multiple glitches. The output inverter, formed by the transistors MN2 and MP2, will reach the threshold voltage and the glitch will not be filtered. A reset mechanism is required to get rid of this issue. This is presented in the Figure 31 (right). A reset mechanism is implemented, to discharge the *rcn* node via an NMOS transistor. For every applied low glitch *rcn* is discharged to *GND*. In the same manner, a reset mechanism must be implemented for input high glitches. Another issue with this circuit is the threshold voltage of the inverter, which has a large temperature variation. For this reason, a different circuit was chosen in this thesis. A concept of the proposed glitch filter circuit is shown in Figure 32. A Schmitt trigger replaces the output inverter to minimize the impact of temperature on the threshold voltages. In addition, a reset mechanism for a high/low input glitch is implemented. The *resl* and *resh* switches, which are charging and discharging the *rcn* respectively, provide the explained reset mechanism. The output will be finally stored in a Flip flop.

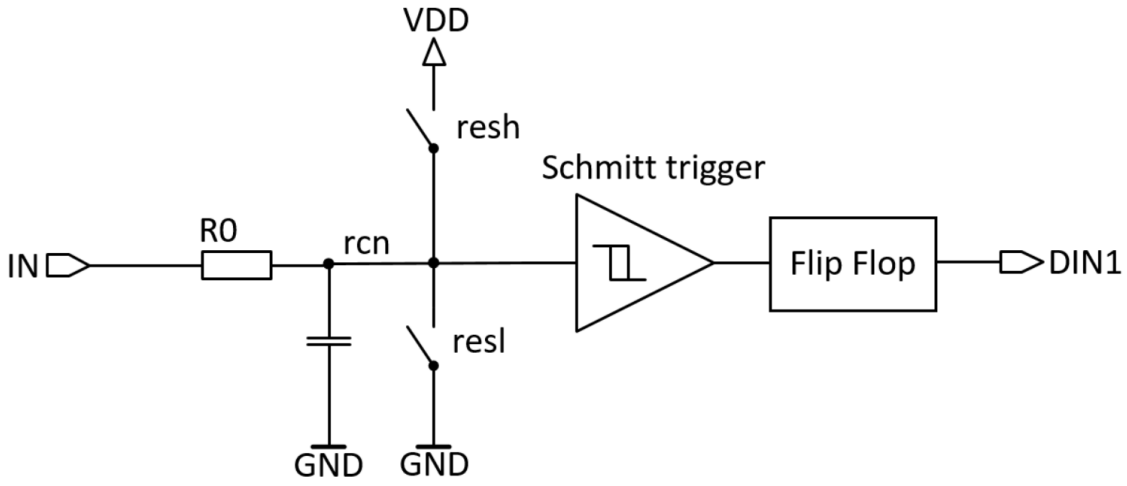

Figure 32: Concept of the proposed glitch filter circuit.

4.2.1.7 Delay blocks

Delay elements are required in various VLSI (Very Large Scale Integration) applications, including asynchronous system, a self-timed dynamic logic, a phase-locked loop (PLL), and a switch capacitor circuit [26]. The delay range varies with the application requirements [26]. The delay is typically in the order of ps and ns for high-frequency applications and in the order of µs and ms for low-frequency applications [26]. A delay element can be implemented using analog and digital methods [26], [27]. A variety of digital and analog delay elements are presented in previous works of [27] and [28]. In this thesis, the delay element is needed to detect a START and STOP condition by an I2C slave controller. In previous works various delay elements are compared [27], [28]. For this thesis, some of those delay elements are implemented. The chosen delay circuits include an inverter chain with an RC delay, a cascaded glitch filter delay, and a CMOS thyristor delay. Finally, the results of each delay will be discussed and one delay element will be chosen based on these results.

4.2.1.7.1 Cascaded Inverters

A simple method of implementing a delay circuit is using a pair of cascaded inverters [28]. The delay element is formed by six cascaded inverters. Each inverter adds a delay to the input signal [28]. The propagation delay of an inverter depends on the charge and discharge load capacitance [28]. An approximation can be done by using an average value of the saturation current of PMOS and NMOS transistors [28]:

$$I_{av} = \frac{k_{p/n}}{2}(V_{GS} - |V_{T_{p/n}}|)^2 = \frac{k_{p/n}}{2}(V_{DD} - |V_{T_{p/n}}|)^2 \approx \frac{k_{p/n}}{2}{V_{DD}}^2. \tag{8}$$

Since $V_{DD} \gg |V_{Tp}, V_{Tn}|$[28], in respect to (8), following propagation delay can be derived [28]:

$$t_{prop} = \frac{1}{2}(t_{pLH} + t_{pHL}) = \frac{C_L}{2 \cdot V_{DD}} \left(\frac{1}{k_p} + \frac{1}{k_n} \right). \tag{9}$$

The total propagation delay is made up of all single delays, including the rise/fall time of each inverter [28].

4.2.1.7.2 Cascaded Glitch Filter Delay

The second concept consists of two cascaded glitch filter blocks. Since the introduced glitch filter circuit from Chapter 4.2.1.6.1 is adding a delay to the input signal, a cascade circuit of two glitch filters can be implemented as a delay. The basic concept of the cascaded glitch filter delay is presented in Figure 33.

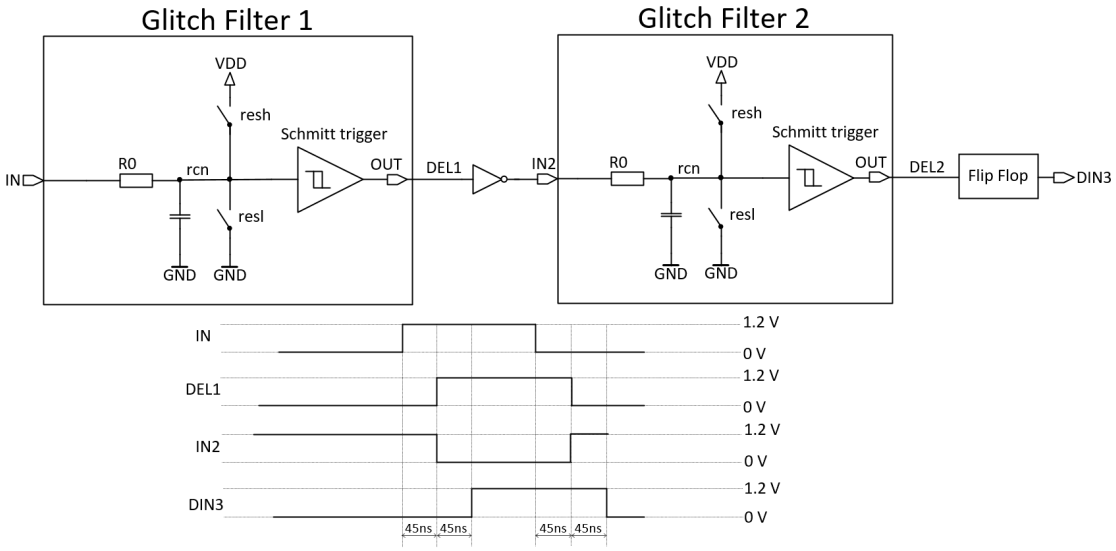

Figure 33: Concept of the cascaded glitch filter delay.

4.2.1.7.3 CMOS Thyristor Delay

The CMOS thyristor delay works with two thyristor structures $SCR1$ and $SCR2$, depicted in Figure 35. The internal structure of the two thyristors will be shown in Chapter 5.2.3.2. In addition, the circuit consists of two Pull Down Networks (PDNs) which determine the discharge current of the two capacitors $C1$ and $C2$. A timing diagram for this concept of the thyristor-based delay element is presented in Figure 35. If a rising edge at the time t_1 at the Input IN occurs, the capacitor $C1$ will be discharged with the switch $S3$ and the PDN. If the node $\overline{Vout}$ is under a certain threshold, $SCR2$ will not be switched on and $C2$ is charged to VDD over $S2$, at time t_2. Similarly, a falling edge at the input node can be explained. The output logic generates the output signal $DIN3$ for a rising/falling input edge.

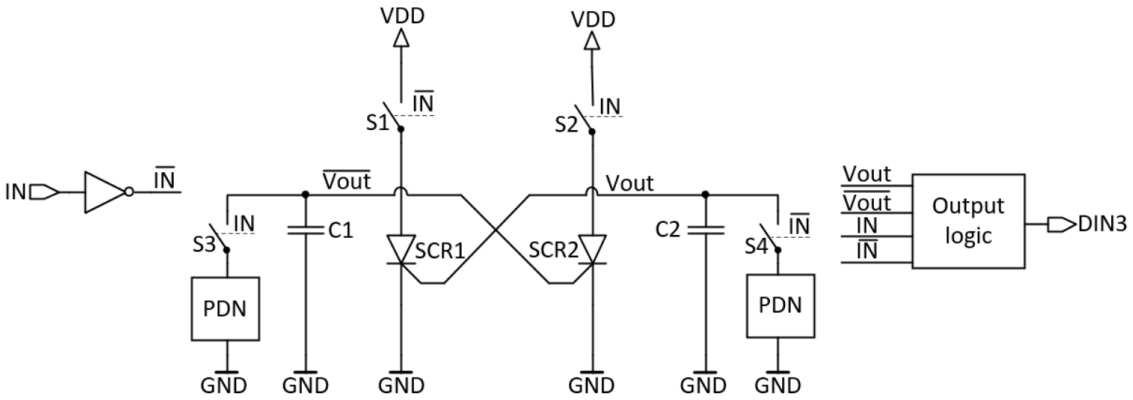

Figure 34: Concept of the thyristor-based delay element.

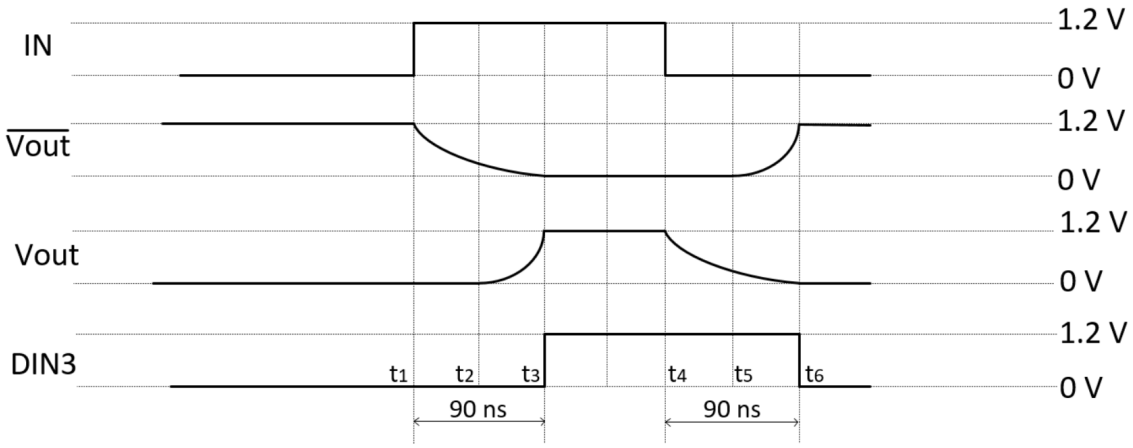

Figure 35: Timing diagram of the of the thyristor-based delay element.

4.2.2 Output structure

In this chapter, all relevant knowledge for the blocks of the output structure is provided. This includes the non-overlapping gate driver and the modular output block.

4.2.2.1 Non-Overlapping Gate Driver

A non-overlapping gate driver is the first non-modular block in the output path. This block is necessary, to avoid switching overlaps of PMOS and NMOS transistor of the Push-Pull driver. If data transits from 0 to 1, the NMOS transistor M0 must be switched off and the PMOS transistor M2 must be turned on. If transistors M0 and M2 are turned on and off at the same time a cross current from *vddo* over M2 and M0 to *gndo* is flowing. This will lead to an increase in power consumption. In Figure 36 a schematic of the Push-Pull output driver is depicted. Using a design with a delayed P_GATE and N_GATE signal shows no cross current $Icross$. If P_GATE and N_GATE are not delayed, a cross current will flow, as it is shown in the right timing diagram of Figure 36.

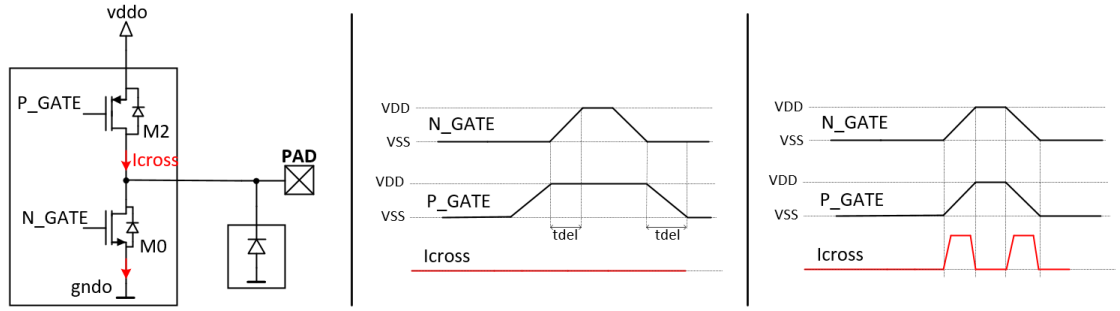

Figure 36: Cross current visualization of a non-overlapping gate driver (middle) and without a non-overlapping gate driver (right).

4.2.2.2 Failsafe Output Stage

The I3C specification indicates that an I3C device does not increase the leakage current when the device is unpowered [9]. This can happen when the whole device is in a power-down state, but the I3C bus is still powered [9]. The input leakage must not exceed 10 µA for $V_{BUS} \geq 1.8$ V and 5 µA for $V_{BUS} \leq 1.8$ V. The main issue with the failsafe implementation is the PMOS driver. In Figure 37 only one PMOS transistor is used for the I3C push driver. If the device is unpowered the supply voltage is 0 V. However, the bus voltage is still at 1.2 V in the example of Figure 37. As a result, the PAD node is also at 1.2 V. The green-colored body diode of the PMOS transistor is now forward-biased. An additional leakage current I_{LEAK} is backpowering the IC and might cause effects that corrupt the I3C communication. This additional leakage current will exceed the maximum leakage current of 5 µA/ 10 µA. The failsafe requirement with this implementation is not met. As a result of this problem, two solutions are presented to fulfill the failsafe requirement. The first solution is the usage of back-to-back connected PMOS transistors. The second solution is an inherent failsafe concept.

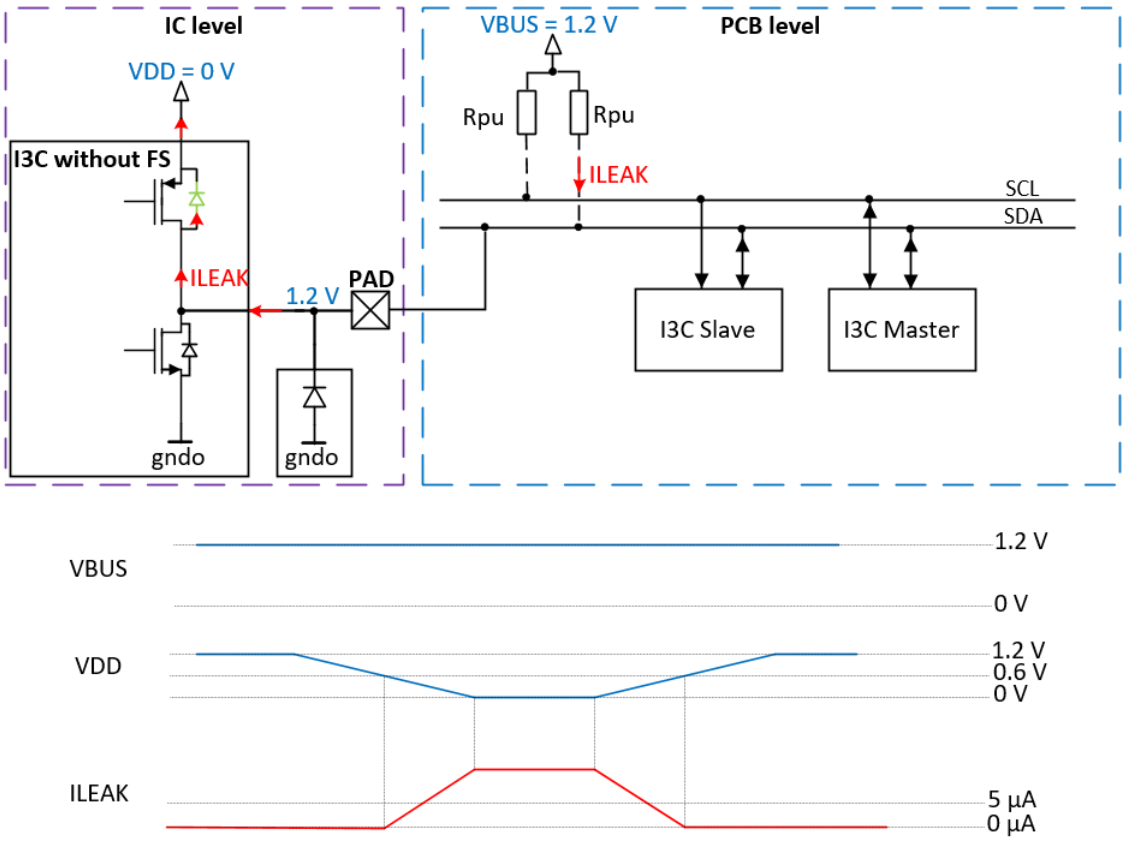

Figure 37: Failsafe problem with the usage of a single PMOS transistor.

4.2.2.2.1 Back-to-Back connected PMOS transistors

The first solution to be discussed is the one with the two back-to-back connected PMOS transistors. The transistor is connected in a command source configuration, shown in Figure 38. This results in two anti-serial body diodes. If the IC is unpowered, the colored green body diode is forward-biased, but the second body diode (marked as red) is still reverse-biased. No leakage current can flow, which fulfills the failsafe requirement from the MIPI specification [9].

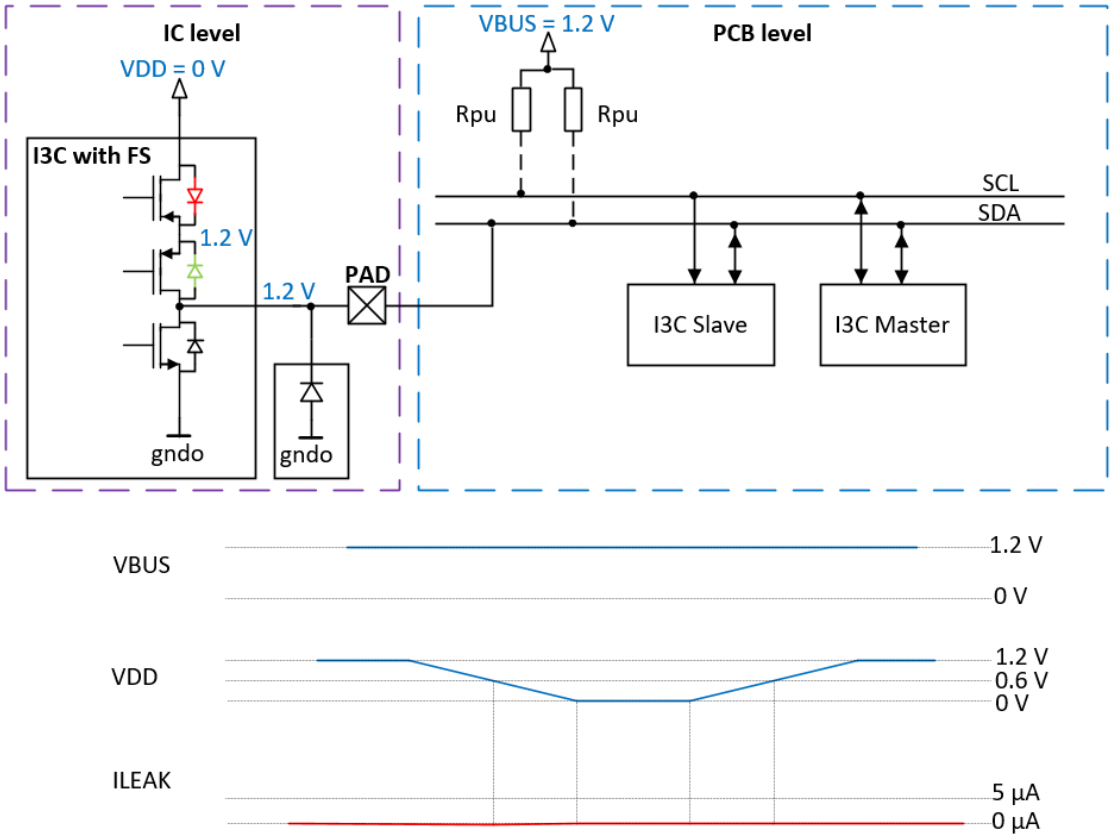

Figure 38: Back-to-back connected PMOS transistors to fulfill failsafe requirement.

4.2.2.2.2 Inherent failsafe concept

The second solution is an output driver which is inherent failsafe, shown in Figure 39. The idea of an inherent failsafe output stage needs to be supported by both, the chip topology as well as the PCB system topology. In the inherent failsafe output concept, the output stage is not supplied from the main chip supply domain, but rather from the I3C V_{BUS} supply directly. This requires the IC to provide separate pins for the V_{BUS} domain from the I3C PCB system to be connected. Separate V_{DDIO} and G_{NDIO} are necessary. In this concept, when the IC is not supplied, V_{BUS} is still available for the output stage, preventing the parasitic bulk-source diode of the PMOS transistor from getting forward-biased.

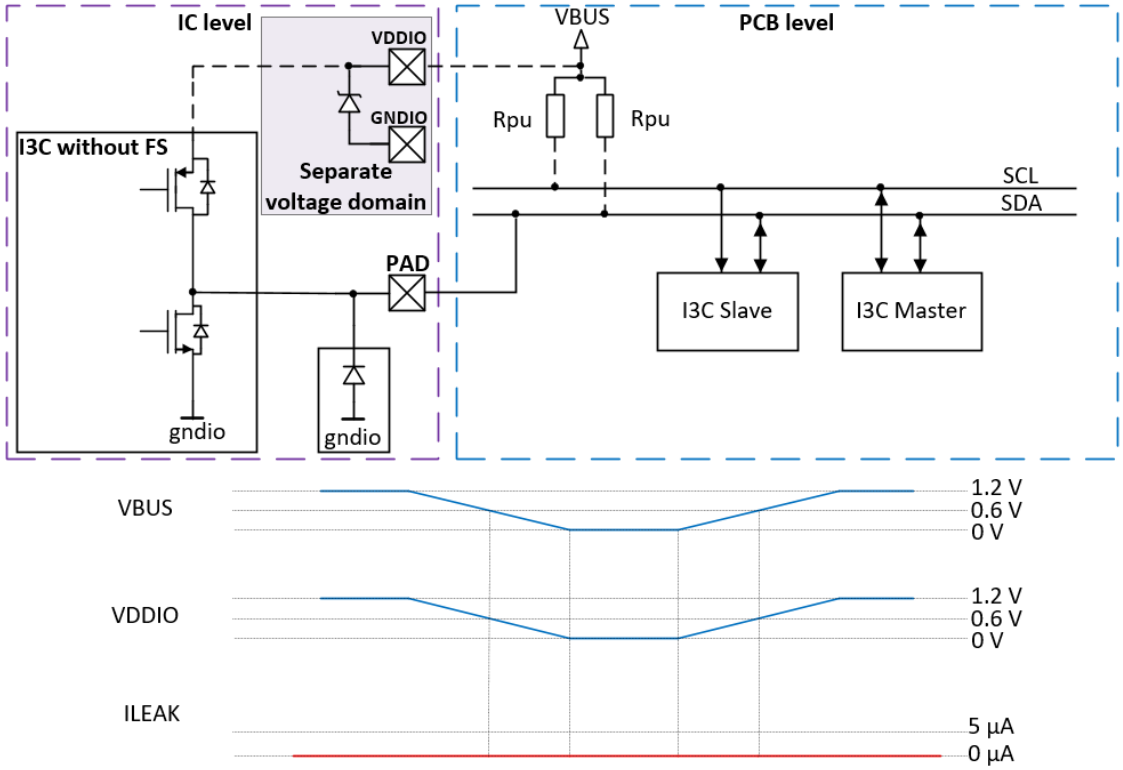

Figure 39: Inherent failsafe solution.

5 I2C/I3C cell implementation

This chapter implements the proposed I/O options from Table 2 in the Cadence Design environment. The implemented I/O options are verified with the proposed simulation strategy from Chapter 5.1.

5.1 Simulation strategy

To ensure the correct implementation of the various I/O options a simulation strategy is needed. The simulation strategy contains DC, transient simulations, a consideration of process variation, a floating node induced leakage path check, and a SOAC.

5.1.1 Safe Operating Area Check

Device reliability plays an important role within circuit design [36]. The lifetime standards of modern circuits for automotive and industrial applications can lead up to 10.000 hours [36]."Therefore to ensure such a lifetime for high voltage and temperature applications the design development is using conservative techniques for design for reliability (DfR) like safe operating areas. Within this operating area is determined by certain voltage and current/power conditions" [36], which is depicted in Figure 41. Safe Operating Area (SOA) checks the maximum parameters such as *vgs_max* or *vds_max* which are predefined. If the maximum parameters are exceeded, a warning will be presented. One possibility to perform SOA checking is the following: "Model encapsulation of every device by an SOA checker which is connected in parallel to the respective device" [36].In Figure 40 an example of model encapsulation of an NMOS transistor is depicted. The properties of transistor Mx can be measured by a high description language (HDL) [36].

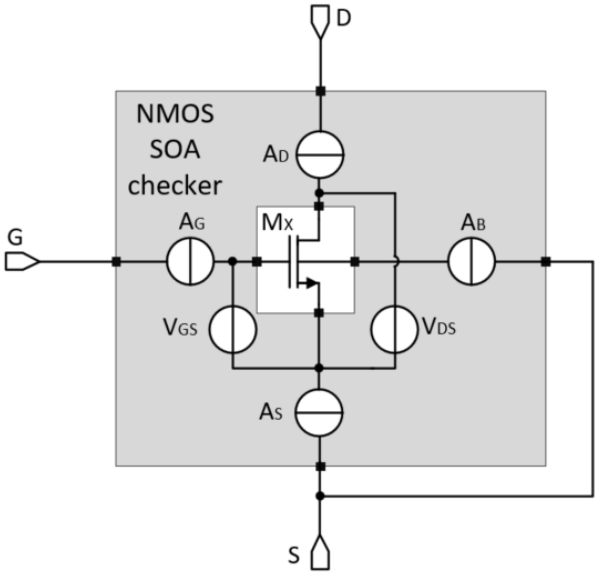

Figure 40: SOA rule check by model encapsulation of the device models [36].

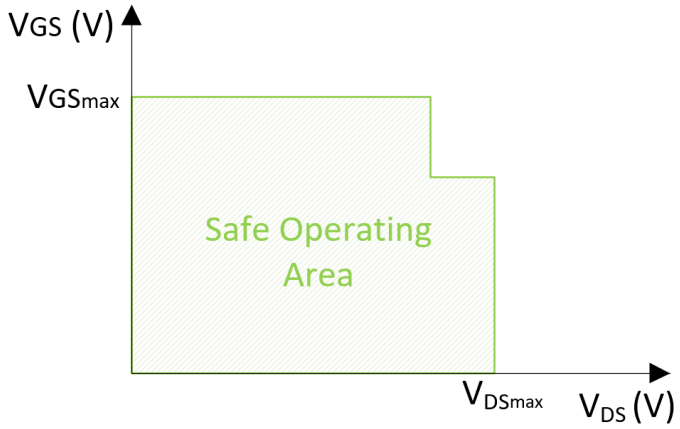

Figure 41: SOA diagram for 10.000 hours lifetime.

5.1.2 Floating Node Induced Leakage Path Check

A floating node induced leakage path check uses a two-step approach for this check. First, a floating node is checked similarly to a dynamic high impedance check. A dynamic high impedance check detects any floating node during a given specific time window of a transient simulation. In Figure 42 an example of a floating node is shown. A dynamic high impedance check indicates only floating nodes and does not give any information about the leakage paths caused by the floating nodes. In addition, the floating node will only be identified if the stimuli trigger the floating node scenario. After the dynamic high impedance check, the floating voltage sweep from 0 V to *VDD* is performed. The floating node induced leakage path check identifies any leakage path related to the floating gate MOSFET. The steps taken by the floating node induced leakage path check are visualized in Figure 43.

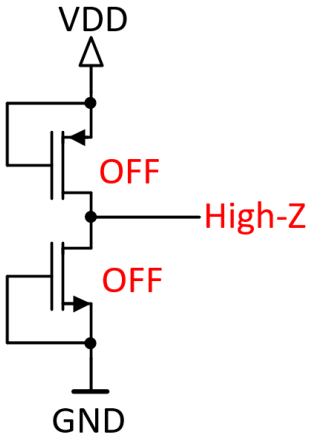

Figure 42: Example of a floating node.

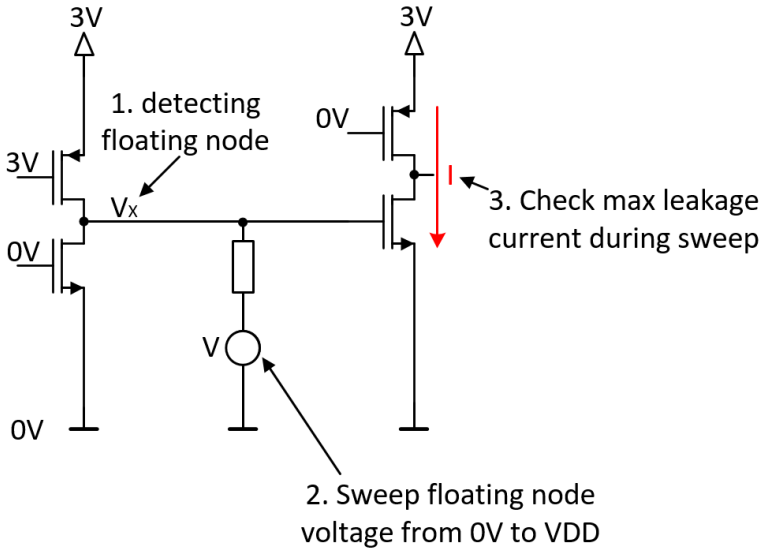

Figure 43: Steps taken by the floating node induced leakage path check.

5.1.3 Dealing with Process Variation

The implemented design must be robust against temperature, supply variation, process variation, and mismatch. Process parameters such as the gate oxide thickness t_{ox}, can vary over a whole wafer, as shown in Figure 44. Local variations caused by trapped charges in the gate oxide, or random dimensional variations can lead to parameter mismatch. Two principles can be applied to simulate process variation: a corner analysis and a Monte Carlo analysis.

5.1.3.1 Corner analysis

Every controlled process parameter on silicon must lie between a minimum (MIN) and a maximum (MAX). If a simulation of the design with the MIN and MAX values of each parameter is performed, the assumption can be made, that the silicon will meet the specifications as well. Since there are a lot of parameters, this will lead to an enormous simulation effort. To avoid this problem, the MIN/MAX values of the most extreme cases are covered with the minimum number of model files. The different model files are presented in Table 3. The different model files for a MOS transistor with designated explanations are shown in Table 3. Furthermore, an explanation for the resistor and capacitor corners is briefly explained in Table 4. The design must meet the specifications in all process corners, shown in Figure 45.

Furthermore, corners are also constructed for several other device groups. For this thesis, resistors, capacitors, and MOS transistors are of interest. An example of a corner set for a nominal supply voltage of 1.2 V is given in Table 5. The corner set does not include the typical operating conditions (25 °C, 1.2 V, tm), since they are already covered by the nominal corner.

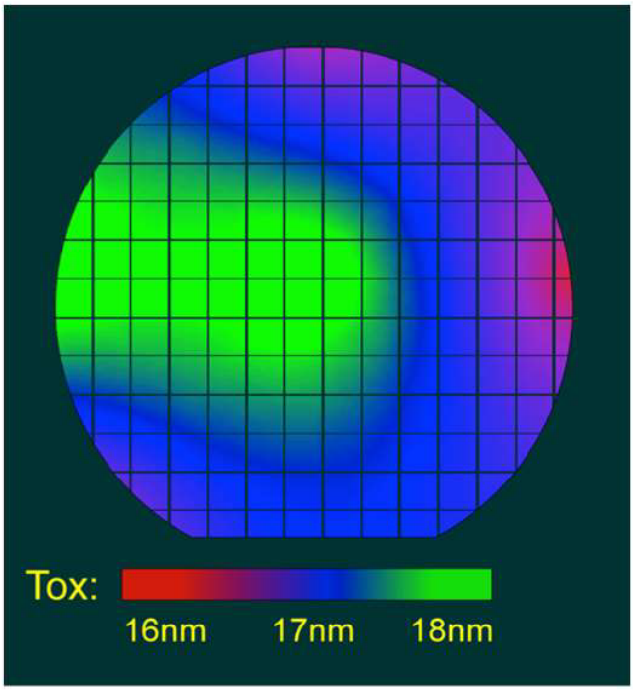

Figure 44: Gate oxide variation over a wafer [37].

tm	Typical mean		
ws	Worst Speed	Slow = high V_{th} and low I_{DS}	Slow PMOS and slow NMOS
wp	Worst Power	Fast = low V_{th} and high I_{DS}	Fast PMOS and fast NMOS
wz	Worst Zero		Slow NMOS, fast PMOS
wo	Worst One		Fast NMOS, slow PMOS

Table 3: Explanation of the different model files used in the corner analysis.

Process corner	Resistor	Capacitor
wp	MIN resistance, MAX current	MIN capacitance, MIN current
ws	MAX resistance, MIN current	MAX capacitance, MAX current.

Table 4: Explanation of the resistor and capacitor corners.

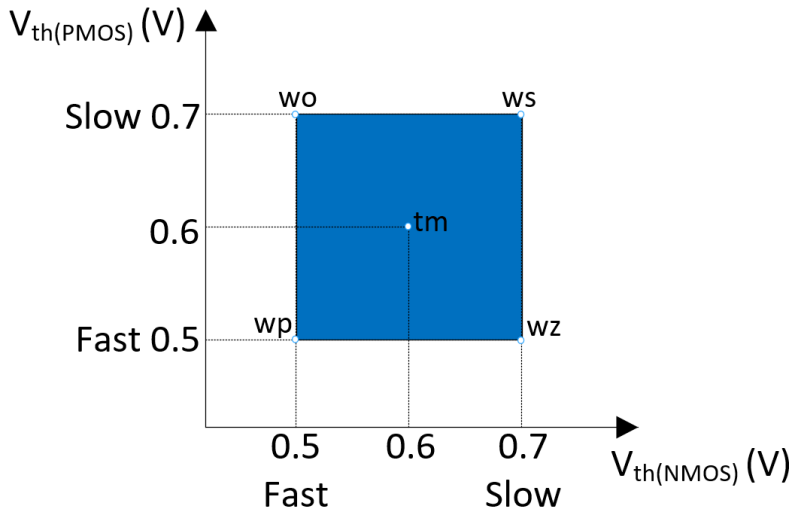

Figure 45: Corner analysis based on the threshold voltage of MOS transistors [37].

Parameters	
Temperature [°C]	-40 150
VDD [V]	1.08 1.32
MOS process corner	cmoswo cmoswp cmosws cmoswz
Capacitor process corner	capwp capws
Resistor process corner	reswp resws

Table 5: Example of a corner set for a 1.2 V supply domain.

5.1.3.2 Monte Carlo Analysis

Since a corner simulation does not give any direct yield estimation, the Monte Carlo (MC) analysis is introduced. A Monte Carlo analysis uses a statistical way to analyze a circuit. An MC analysis considers the variation across one wafer whereas a Corner analysis considers the process variation across several lots. Every parameter has a statistical distribution. For each run, every parameter is calculated randomly according to the process-given distributions. This leads to a different variation for each device. An MC analysis takes process variation and mismatch into account. A differential input stage is a good example to show the impact of the mismatch. For a differential input stage, the threshold voltage of every device is different, as shown in Figure 49. This will lead to an offset voltage for the differential input stage. The mismatch simulation is based on a Gaussian distribution, which leads to a circle around the typical corner, as depicted in Figure 46. Figure 47 shows the mismatch simulation applied on each process corner and typical corner. This illustrates a theoretical worst-case scenario, which does not correspond to reality. In real fabrication the wo and wz corners are unlikely to reach since process parameters are mutually correlated. If the gate oxide thickness of a PMOS transistor is small, the NMOS transistor has also a thinner gate oxide. This correlation is taken into account when simulating process and mismatch combined, as it is depicted in Figure 48. Figure 48 shows the more probable scenario to reality. All MC simulations in this thesis are done with process and mismatch.

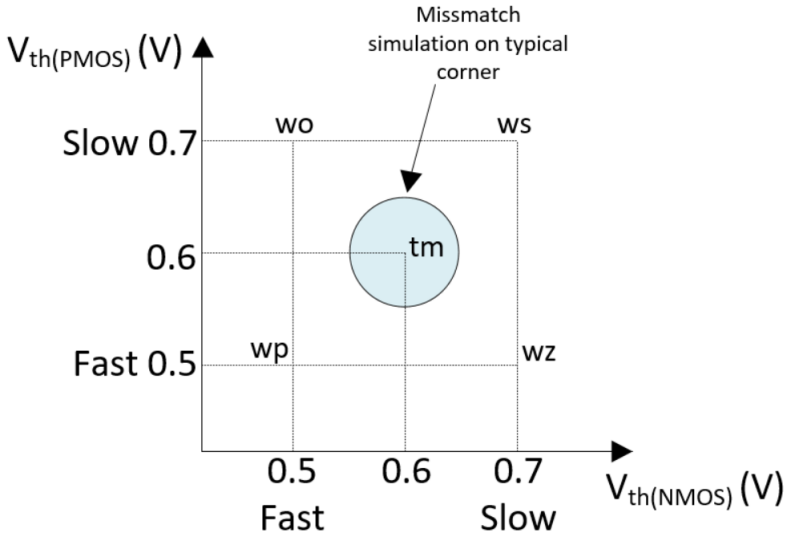

Figure 46: Mismatch simulation on a typical corner.

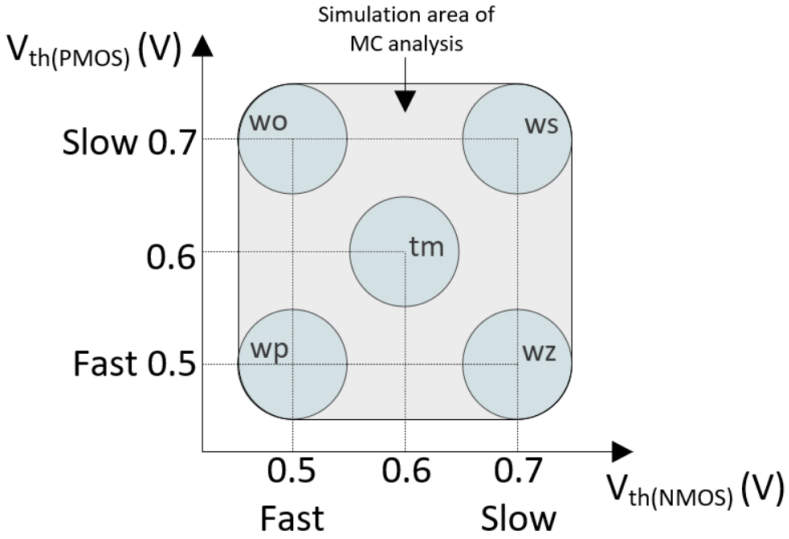

Figure 47: Simulation area of a mismatch simulation on every process and typical corner.

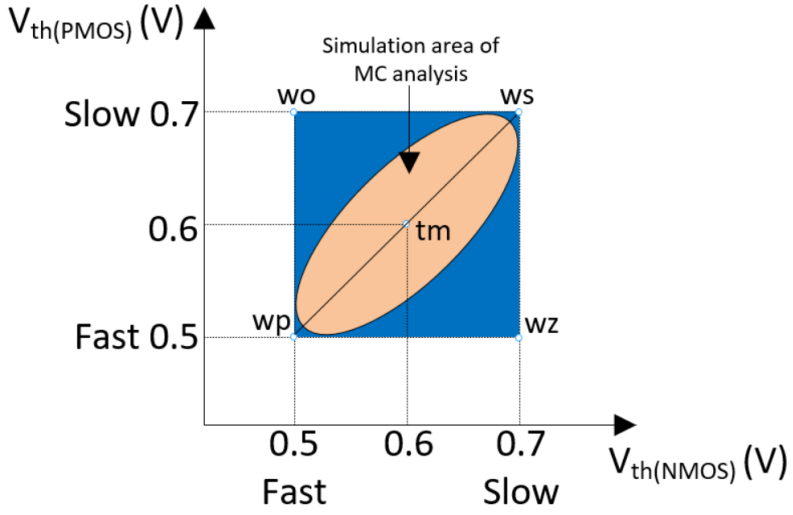

Figure 48: Simulation area for a process and mismatch simulation.

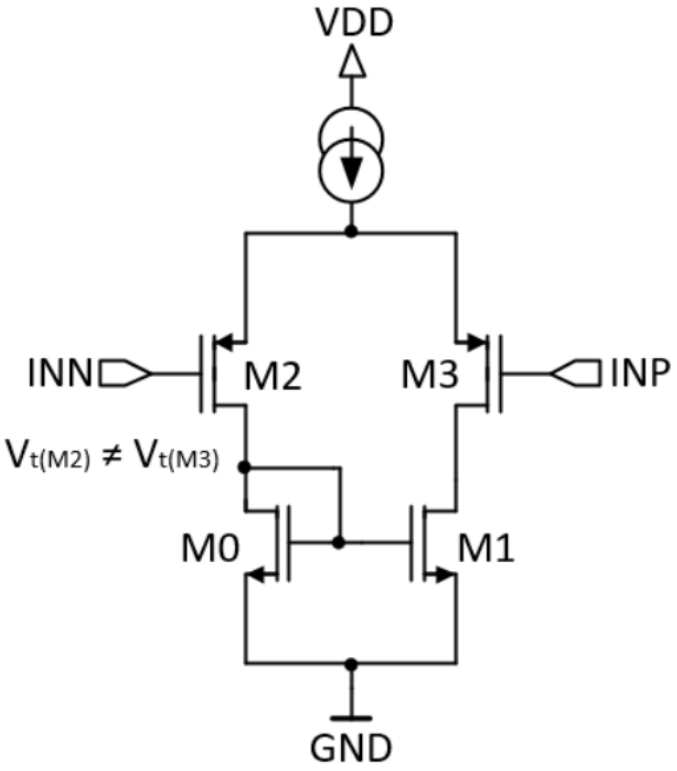

Figure 49: Mismatch illustration of a differential input stage.

As a result of the Monte Carlo analysis, a histogram of the Schmitt trigger hysteresis is obtained, as shown in 50. The histogram in Figure 50, shows the mean value, the standard deviation, and the values for the threshold voltage for $\pm$ 3σ. Another important parameter is the Process Capability Index (Cpk) value. The Cpk value takes the location of the distribution within the spec limits into account. The Cpk value shows how many standard deviations the specification limits are from the mean value of the process. The formula of the Cpk is shown in the (10). The higher the Cpk value, the better the yield. In general, a Cpk of 1.33 or higher is desired. A Cpk value of 1.33 leads to a yield of 99.99 %, and a Cpk of 0.67 leads to a yield of 95.45 %. The two Gaussian distributions for the two Cpk values are presented in Figure 51.

$$Cpk = min\left(\frac{USL - \mu}{3\sigma}; \frac{\mu - LSL}{3\sigma}\right)$$

USL .. Upper Spec Limit

LSL .. Lower Spec Limit

(10)

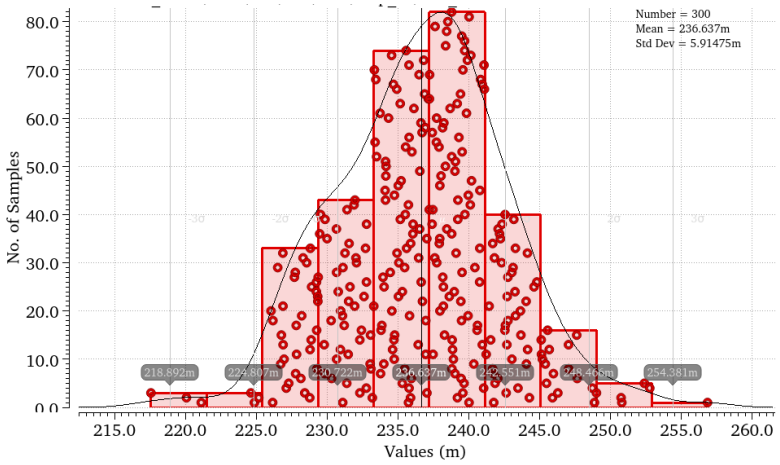

Figure 50: Histogram of the input Schmitt trigger hysteresis.

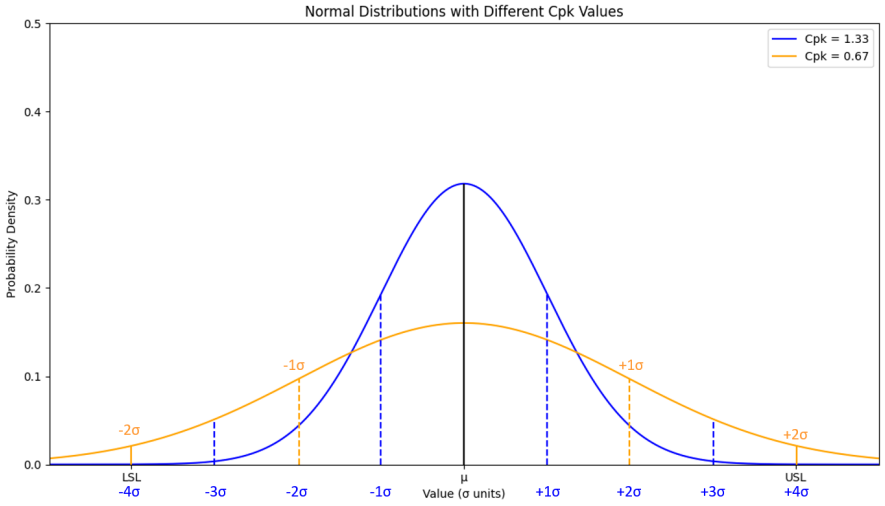

Figure 51: Distribution for different Cpk values.

5.2 Data In Path

5.2.1 Schmitt trigger implementation

This chapter presents the implementation of the modular Schmitt trigger, presented in Chapter 4.2.1.5. The modularity concept contains three different Schmitt trigger options, which are the following:

1. $V_{BUS} = VDD = 1.2$ V,
2. $V_{BUS} = 1.8$ V, $VDD = 3.3$ V,
3. $V_{BUS} = VDD = 3.3$ V.

5.2.1.1 Option $V_{BUS} = VDD = 1.2$ V

As already clarified in Table 2, one possible option includes $VDD = V_{BUS} = 1.2$ V. The schematic for this variant is shown in Figure 52. Since the highest nominal voltage that appears is 1.2 V, 1.2 V transistors are chosen. The threshold voltage was approximated with $V_{TH} \approx 500$ mV, which is necessary to solve (11) and (12). In addition, applying (4) and (5) , the MIPI specification must be considered. MIPI introduced the maximum low-level input voltage $V_{IL} = 0.3 \cdot VDD$ and a minimum high-level input voltage $V_{IH} = 0.7 \cdot VDD$ [9]. Other important specification parameters are the two threshold voltages V_{TH_LH} and V_{TH_HL} and the hysteresis V_{HYST}. The hysteresis can be calculated as $V_{HYST} = V_{TH\_LH} - V_{TH\_HL}$. Since temperature and process variations affect the hysteresis of the Schmitt trigger significantly, an additional margin must be implemented. This margin is accomplished by setting the threshold values to $V_{TH\_LH} = VDD \cdot 0.6$ and $V_{TH\_HL} = VDD \cdot 0.4$. An Input Enable signal (IE) is used, to disable the Schmitt trigger when not operating. If $IE = 0$, M9 is turned on and pulls the potential of *outn* to *VDD*. Since the node *outn* is attached to an inverter, the output is pulled to VSS. M12 sets the node v_P to VDD. This is necessary to avoid that v_P is floating.
The PMOS transistor ratios can be calculated as the following:

$$\begin{aligned} \frac{\beta_5}{\beta_6} &= \left[\frac{V_{TH\_HL}}{VDD - V_{TH\_HL} - V_{THP}}\right]^2 = \left[\frac{VDD \cdot 0.4}{VDD - VDD \cdot 0.4 - 500\text{ mV}}\right]^2, \\ \frac{\beta_5}{\beta_6} &= \left[\frac{480\text{ mV}}{1.2\text{ V - }480\text{ mV - }500\text{ mV}}\right]^2 = 4.76. \end{aligned} \tag{11}$$

The NMOS transistor ratios can be calculated as the following:

$$\begin{aligned} \frac{\beta_1}{\beta_3} &= \left[\frac{VDD - V_{TH\_LH}}{V_{TH\_LH} - V_{THN}}\right]^2 = \left[\frac{VDD \cdot 0.6}{VDD - VDD \cdot 0.6 - 500\text{ mV}}\right]^2, \\ \frac{\beta_1}{\beta_3} &= \left[\frac{1.2\text{ V - }720\text{ mV}}{720\text{ mV - }500\text{ mV}}\right]^2 = 4.76. \end{aligned} \tag{12}$$

The calculated ratios of (11) and (12) must be used for the transistor dimensioning.

$$\frac{\beta_5}{\beta_6} = 4.76 \stackrel{!}{=} \frac{W5 \cdot L6}{W6 \cdot L5}$$
$$\mathrm{W_5} = 21\ \mu\mathrm{m},\ \mathrm{W_6} = 7\ \mu\mathrm{m},\ \mathrm{L_5} = \mathrm{L_6} = 180\ \mathrm{nm} \tag{13}$$

$$\frac{\beta_1}{\beta_3} = 4.76 \stackrel{!}{=} \frac{W1 \cdot L3}{W3 \cdot L1}$$
$$\mathrm{W_1} = 9\ \mu\mathrm{m},\ \mathrm{W_3} = 1\ \mu\mathrm{m},\ \mathrm{L_1} = \mathrm{L_3} = 180\ \mathrm{nm} \tag{14}$$

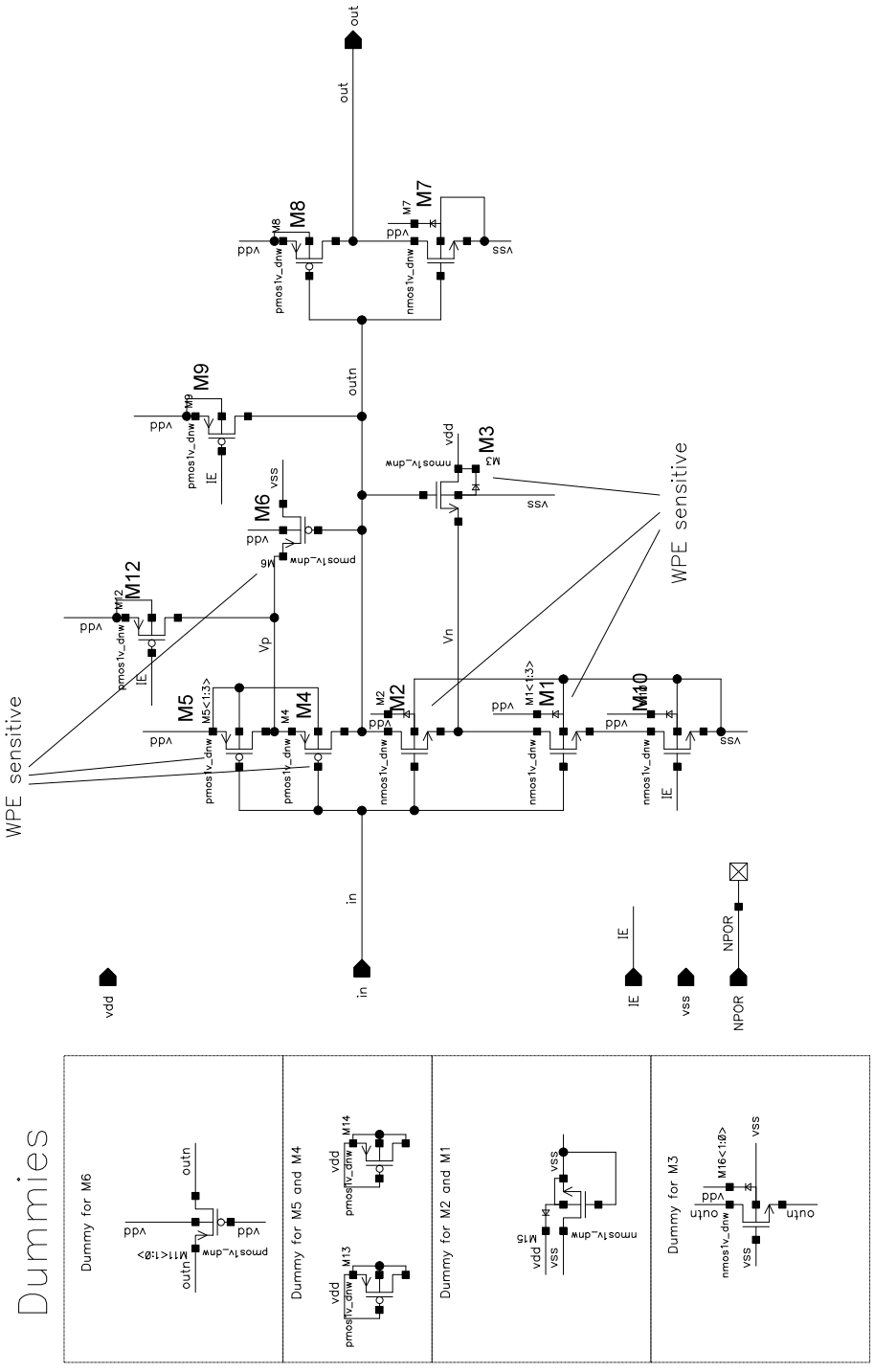

Figure 52: Schmitt trigger design for $V_{BUS} = VDD = 1.2$ V.

5.2.1.2 Option V_{BUS} = 1.8 V, VDD = 3.3 V

In the same manner the Schmitt trigger design for the V_{BUS} = 1.8 V and VDD = 3.3 V option can be accomplished. The design requires 3.3 V transistors since the highest nominal voltage is 3.3 V. The schematic for this option is depicted in Figure 53.

Calculating PMOS transistor ratios:

$$\frac{\beta_5}{\beta_6} = \left[\frac{V_{TH\_HL}}{VDD - V_{TH\_HL} - V_{THP}}\right]^2 = \left[\frac{720 \text{ mV}}{3.3 \text{ V - } 720 \text{ mV - } 500 \text{ mV}}\right]^2 = 0.12.$$

Calculating NMOS transistor ratios:

$$\frac{\beta_1}{\beta_3} = \left[\frac{VDD - V_{TH\_LH}}{V_{TH\_LH} - V_{THN}}\right]^2 = \left[\frac{3.3V - 1.08V}{1.08V - 500mV}\right]^2 = 14.65.$$

Transistor dimensions:

$$\text{W}_1 = 20 \text{ µm, W}_3 = 700 \text{ nm, L}_1 = 500 \text{ nm, L}_3 = 1.5 \text{ µm,}$$
$$\text{W}_5 = 700 \text{ nm, W}_6 = 3.5 \text{ µm, L}_5 = \text{L}_6 = 500 \text{ nm.} \tag{15}$$

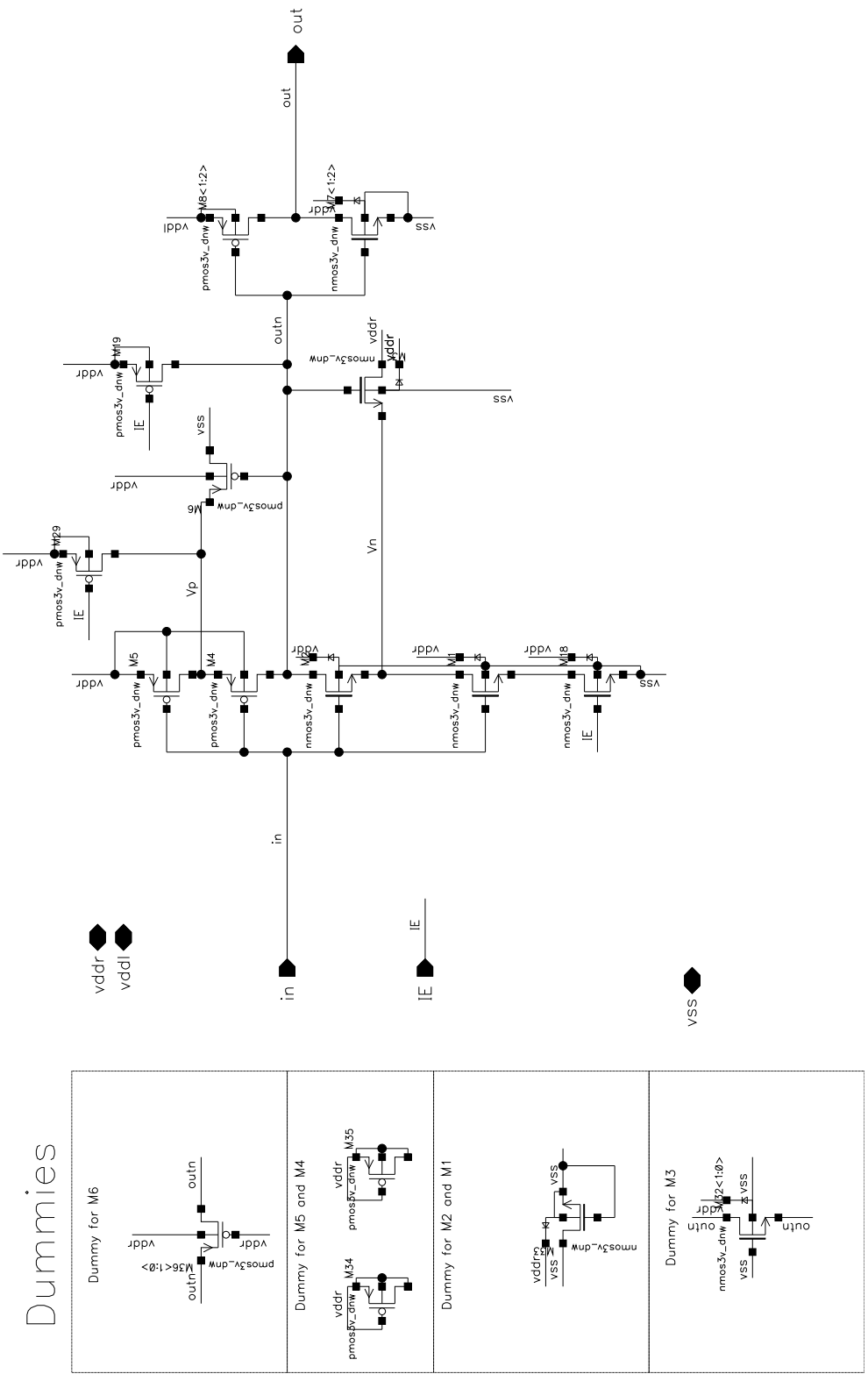

Figure 53: Schmitt trigger design for V_{BUS} = 3.3 V VDD = 1.8 V.

5.2.1.3 Option $V_{BUS} = VDD = 3.3$ V

Finally, the last option is presented in this chapter. As the other two options were explained in detail, this option will not be further analyzed. The design of this option can be accomplished in the same manner. The circuit for this option is depicted in Figure 54. The transistor sizes for this option are calculated the following:

$$W_1 = 4\ \mu m,\ W_3 = 3\ \mu m,\ L_1 = 400\ nm,\ L_3 = 400\ nm,$$

$$W_5 = 6\ \mu m,\ W_6 = 3\ \mu m,\ L_5 = L_6 = 500\ nm.$$

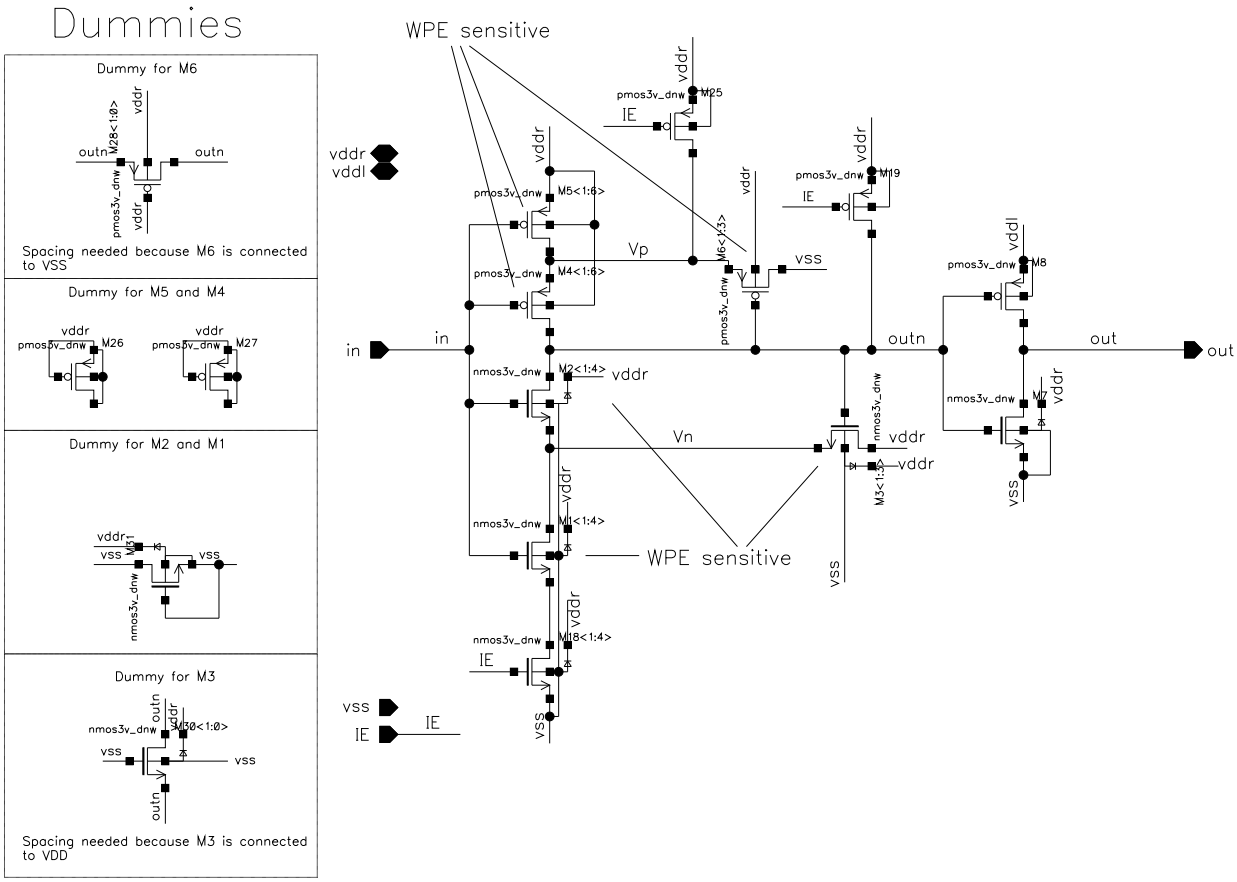

Figure 54: Schmitt trigger design for $V_{BUS} = VDD = 3.3$ V.

5.2.1.4 Simulation results

This chapter shows the hysteresis and the timing parameters for all modular Schmitt trigger blocks. First, the DC parameters of the Schmitt trigger are discussed. The DC parameters contain the threshold voltage and the calculated hysteresis. A slow transient ramp is used to show a DC sweep equivalent behavior. The applied input signal and the corresponding output are visible in Figure 55. The absolute threshold levels V_{TH_LH} and V_{TH_LH} are shown with markers M3 and M4, respectively. Since the MIPI specification uses relative threshold levels, the following calculations are performed:

$$\begin{aligned} V_{TH\_LH\_rel} &= \frac{V_{TH\_LH}}{V_{BUS}} \cdot 100, \\ V_{TH\_HL\_rel} &= \frac{V_{TH\_HL}}{V_{BUS}} \cdot 100, \\ V_{HYST\_rel} &= \frac{V_{HYST}}{V_{BUS}} \cdot 100. \end{aligned} \tag{16}$$

In Table 6 the corner simulation results for the typical mean (tm), Minimum (Min), and Maximum (Max) are listed. In addition, the results of the Monte Carlo simulation are exhibited in Table 6, using the mean value (Mean) the standard deviation (Std. Dev.), and the Cpk value. First, the simulation results for the relative threshold voltages and the relative hysteresis are stated in Table 6. All results are within the specification limits and marked with PASS and fulfill the required Cpk $\geq$ 1.33.
Second, the timing parameters of the Schmitt trigger are discussed. As already introduced, the input path is part of the round trip delay t_{sco}. The propagation delay of the Schmitt trigger must be kept to a minimum. Since the propagation delay of the input path is no specification parameter, it is labeled as INFO in Table 6. The two propagation delays $TPLH\_1$ and $TPLH\_2$, which were introduced in Chapter 3.1, are plotted in Figure 56 and 57.

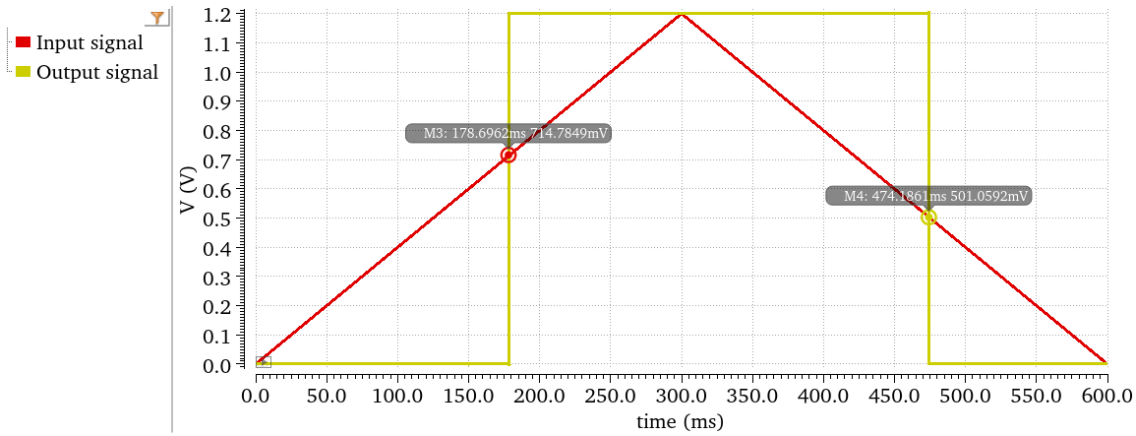

Figure 55: Schmitt trigger threshold measurement via applying a slow transient ramp.

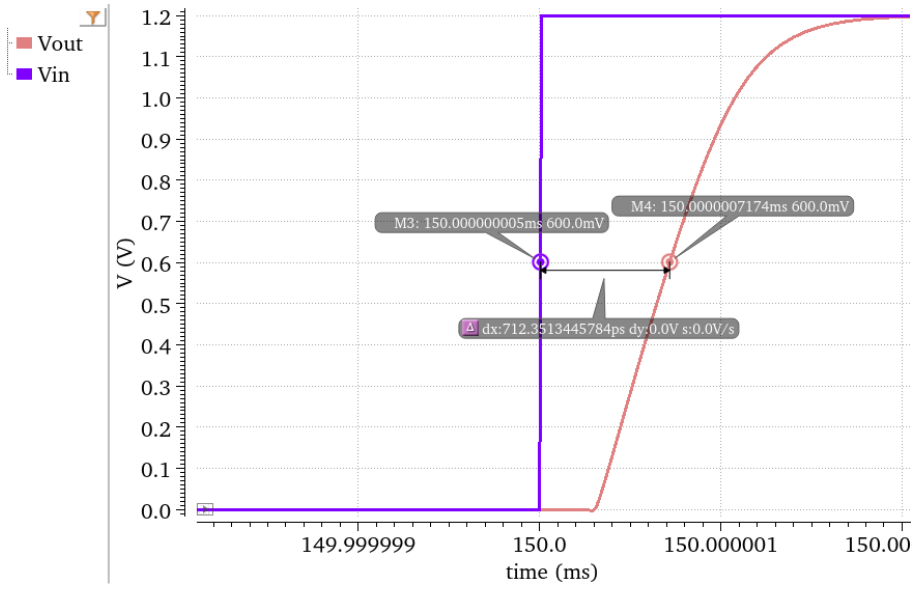

Figure 56: Schmitt trigger propagation delay TPLH_1.

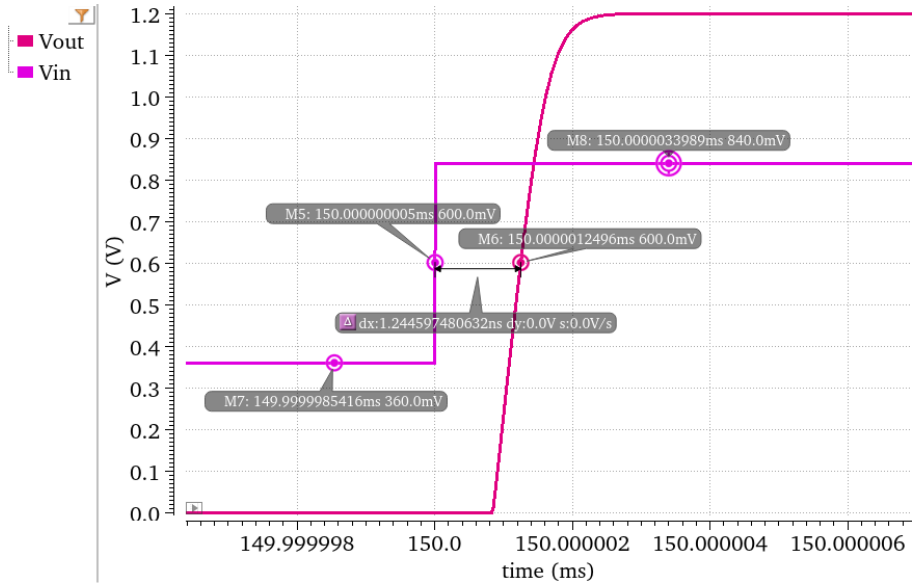

Figure 57: Schmitt trigger propagation delay TPLH_2.

Test names	Spec.	PASS/FAIL	$V_{BUS} = VDD = 1.2$ V						$V_{BUS} = 1.8$ V and $VDD = 3.3$ V						$V_{BUS} = VDD = 3.3$ V					
			tm	Min	Max	Mean	Std. Dev.	Cpk	tm	Min	Max	Mean	Std. Dev.	Cpk	tm	Min	Max	Mean	Std. Dev.	Cpk
$V_{TH\_LH\_rel}$	< 70 %	PASS	59.56 %	53.45 %	65.92 %	61.17 %	893.9 m%	3.29	58.01 %	44.98 %	68.69 %	62.27 %	1.51 %	1.71	59.99 %	56.22 %	64.21 %	65.2 %	531.8 m%	3.01
$V_{TH\_HL\_rel}$	> 30 %	PASS	41.94 %	37.39 %	48.05 %	41.13 %	769.6 m%	4.82	42.7 %	33.37 %	49.85 %	37.29 %	823 m%	2.95	38.45 %	33.95 %	42.71 %	35.17 %	550.4 m%	3.13
V_{HYST_rel}	> 10 %	PASS	17.62 %	11.01 %	23.51 %	13.04 %	450 m%	2.25	15.31 %	11.43 %	21.24 %	13.5 %	593.9 m%	1.97	21.54 %	19.36 %	23.6 %	19.05 %	264.1 m%	11.4
TPLH_1	INFO		712.4 ps	392.7 ps	1.67 ns	959.2 ps	48.46 ps	20.9	1.66 ns	890.5 ps	3.25 ns	2.13 ns	166.3 ps	3.75	1.62 ns	886.9 ps	3.3 ns	2.14 ns	176.7 ps	3.5
TPHL_1	INFO		968.6 ps	600.3 ps	2.25 ns	1.31 ns	103.2 ps	8.7	2.25 ns	1.41 ns	4.35 ns	3.32 ns	102.2 ps	2.2	1.0 ns	778.8 ps	1.55 ns	1.43 ns	33.73 ps	25.4
TPLH_2	INFO		1.25 ns	538.6 ps	7.15 ns	1.28 ns	140.9 ps	6.45	2.28 ns	1.12 ns	5.72 ns	2.91 ns	248.9 ps	1.46	1.73 ns	939.6 ps	3.39 ns	2.31 ns	162.8 ps	3.46
TPHL_2	INFO		960.4 ps	603.1 ps	2.23 ns	1.30 ns	101.2 ps	8.9	1.87 ns	1.25 ns	3.50 ns	2.83 ns	248.9 ps	4.29	987.3 ps	770 ps	1.5 ns	1.40 ns	35.47 ps	24.5

Table 6: Corner and Monte Carlo simulation results for all Schmitt trigger options.

5.2.2 Glitch filter design

As the basic functionality of the glitch filter circuit was clarified in Chapter 4.2.1.6.1, the implemented schematic method will be introduced in this chapter. The circuit shown in Figure 60 is the combination of an RC network and a Schmitt trigger. Furthermore, the node *rcn* is reset via the transistors M1 and M0. The PMOS transistor M0 is pulling the node *rcn* to *VDD*. M0 is controlled by $resh = \overline{INV \cdot OUT\_d50n}$. The same mechanism applies if a low input glitch appears, resetting *rcn* via M1. A timing diagram of this reset mechanism is shown in Figure 58. The glitch filter in Figure 60 must suppress glitches up to 50 ns, which is stated in the specification of MIPI [9]. To deal with the temperature and process variation of the glitch filter the nominal filter time is set to 80 ns. If an input high glitch with less than 50 ns appears at the input, *rcn* will be discharged towards *GND*. As the time constant τ of the RC network is greater than the pulse width of the glitch, the threshold voltage of the Schmitt trigger will not be reached. The output node OUT_N of the Schmitt trigger remains unchanged. The input high glitch is filtered.

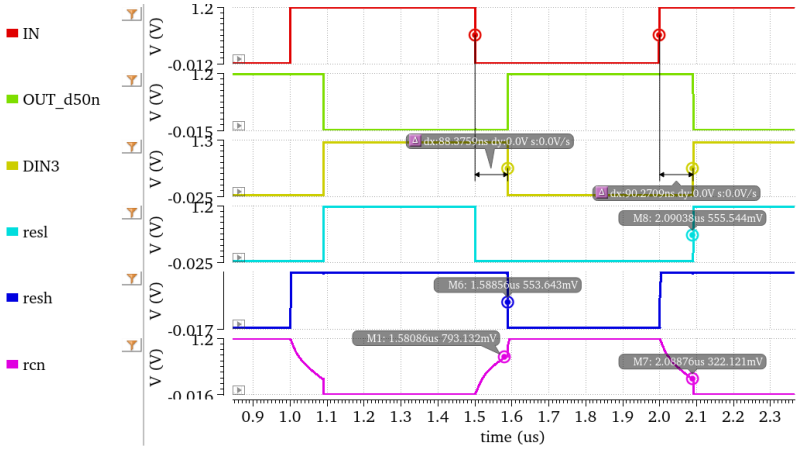

Figure 58: Timing diagram of the proposed glitch filter circuit.

The capacitance needed for the time constant τ is implemented via a MOS capacitor. In this case, the gate capacitance of the two transistors is used. Unfortunately, the gate capacitance depends on the gate-source voltage (V_{GS}) [25]. This dependency is the reason for a mismatch. "When gate-source voltage is applied, greater than the threshold voltage of the transistor, then the channel is already formed, and the capacitance is higher compared to the previous case. As gate-source voltage is increased, the capacity value also changes" [25]. To get rid of this problem, an additional MOS capacitance is added. The two transistors M12 and M13 are used as capacitors. M12 and M13 must be of different types [25]. The dependency of the gate capacitance over V_{GS} is presented in Figure 59. Figure 59 shows the gate capacitance of a PMOS and an NMOS transistor (red curve), the capacitance for a PMOS transistor (green curve) and the capacitance for an NMOS transistor (yellow curve) used as a MOS capacitor. Another advantage of an MOS capacitor is area saving compared to a usual capacitor, due to the higher sheet capacitance of a MOS capacitor compared to a metal capacitor. The two MOS capacitors of transistors M12 and M13 are connected in parallel.

The total capacitance C_{tot} is the sum of the two capacitors [25]:

$$C_{tot} = CP_{M12} + CN_{M13}. \tag{17}$$

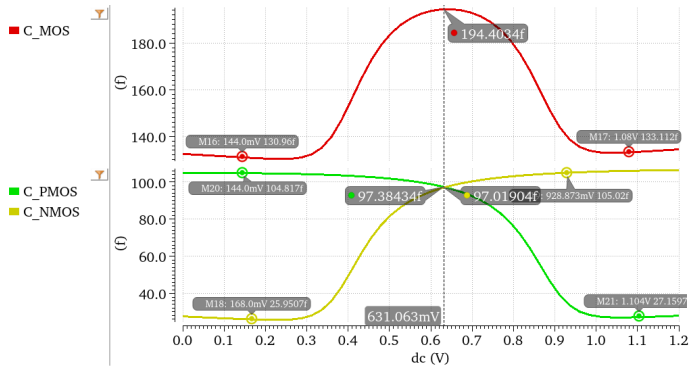

Figure 59: C-V Curve PMOS and NMOS transistor used as a MOS capacitor.

The most important consideration is the time constant τ. The threshold voltage of the Schmitt trigger is directly correlated to the time constant τ. The threshold voltage V_{TH_LH} will be set to around 600 mV. The exact calculation for the threshold voltages will not be conducted for this Schmitt trigger, as the calculation steps are already presented in Chapter 5.2.1.1.

With the definition of V_{TH_LH} , the following calculation can be conducted:

$$V_{TH\_LH} = 0.6 \cdot VDD = VDD \cdot \left(1 - e^{\frac{-t_0}{R \cdot C}}\right),$$

$$t_0 = RC \cdot \ln(0.6) = RC \cdot 0.51,$$

$$t_0 \geq 80 \text{ ns} \longrightarrow 0.51 \cdot RC \geq 80 \text{ ns},$$

$$RC \geq 157 \text{ ns}.$$

The resistance was chosen with 100 kΩ. This results in a needed capacitance of

$$C = \frac{157 \text{ ns}}{100 \text{ k}\Omega} = 1.57 \text{ pF}. \tag{18}$$

As the chosen resistance value is high, a poly resistance to achieve 100 kΩ is needed. A MOS capacitance of 1.57 pF is required to reach a time constant $\tau = 80$ ns. To get a MOS capacitance of 1.57 pF the parameters W and L of the MOS capacitors (M12 and M13) are swept.

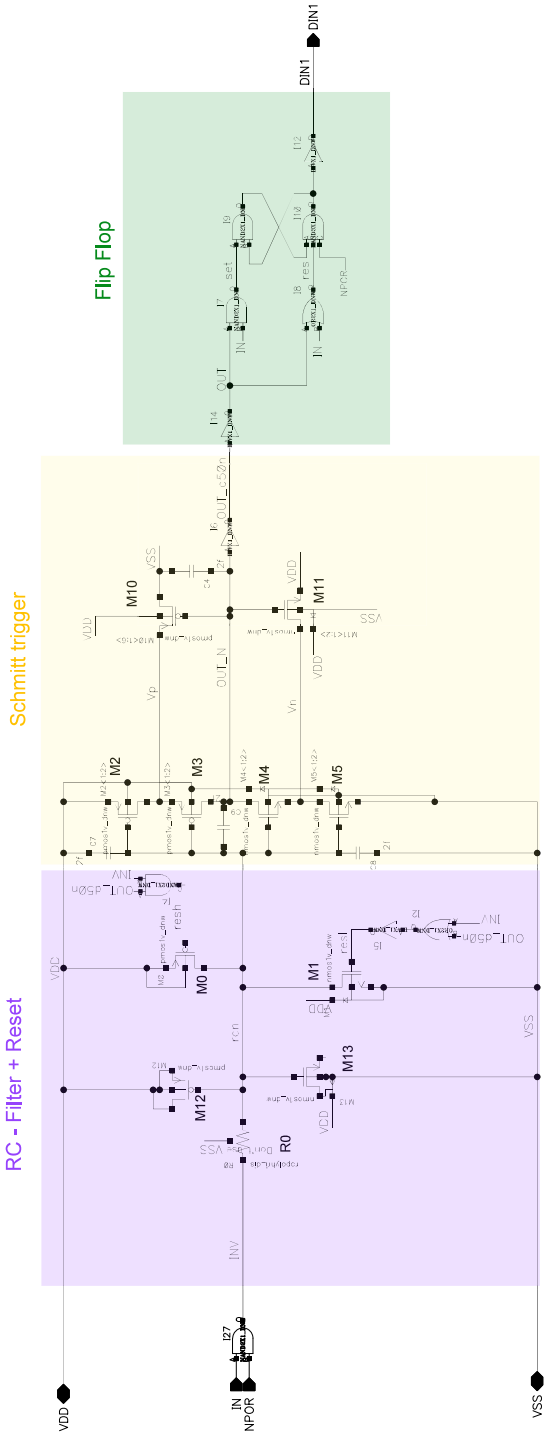

Figure 60: Proposed glitch filter design.

5.2.2.1 Simulation Plan

Moreover, a proper testbench must be set up to validate the correct functionality. The first parameter of high importance is the propagation delay of the glitch filter for a rising/falling edge. As previously mentioned, the duty cycle distortion of the glitch filter must be as negligible as possible. Second, the glitch filter must suppress glitches up to 50 ns over temperature, supply variation, and process corners. This is tested, by applying input glitches with different pulse widths, which can be viewed in Figure 61. In total, five input glitches with different pulse widths are applied. The input signals are represented by *vin_glitch_test* and are labeled with 1-5. The output signal of the glitch filter is represented by *vout_glitch_test*.
Furthermore, a reliability test with ten consecutive 50 ns high-level glitches and ten consecutive low-level glitches was performed. In Figure 62 three different periods can be viewed. Period 1 includes ten consecutive high glitches with a pulse width of 50 ns. Period 2 is a 200 ns pulse, which toggles the output to logic HIGH. Period 3 includes ten consecutive low glitches with a pulse width of 50 ns. All high glitches and low glitches are filtered by the glitch filter circuit. If a glitch had not been suppressed, the signal *tsp_error* would have changed its value. In this case, the *tsp_error* signal shows 0 V for the whole test sequence. This indicates that all glitches are filtered successfully. In combination with this test sequence, an I3C signal with a frequency of 12.5 MHz was applied. This is the highest frequency at which I3C operates and must be suppressed by every I2C device.

The simulation results are presented in Tables 7 and 8. The propagation delay variation over Corner and Monte Carlo analysis is shown in Table 7. Table 8 presents the simulation results for the glitches with different pulse widths, the 12.5 MHz test, and the reliability test. In total, 65 glitches over Corner and 1500 glitches over Monte Carlo were applied. Table 7 indicates that input signals with a maximum pulse width of 60 ns are suppressed. The number of unfiltered glitches of the 12.5 MHz signal is presented in row I3C_TST_12.5MHz_INPUT of Table 8. All glitches for a 12.5 MHz signal are filtered. The last row of Table 8 shows the simulation result for the reliability test. All glitches for this reliability test are successfully filtered.

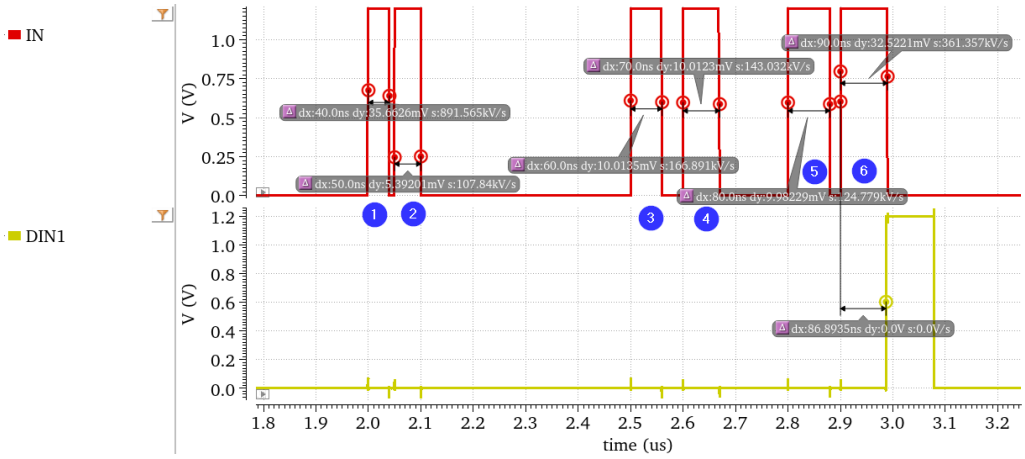

Figure 61: Verification of glitch filter capability of different input signals.

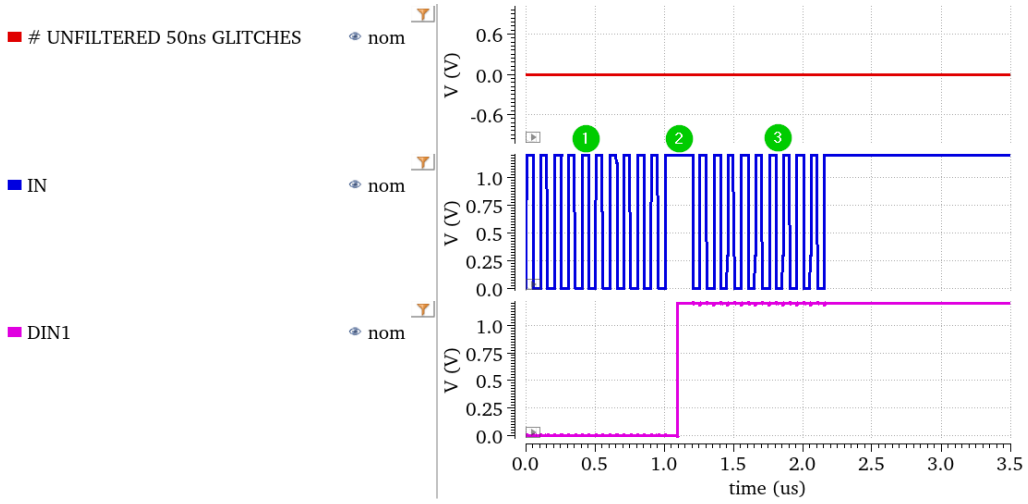

Figure 62: Reliability test with several consecutive 50 ns input glitches.

Test names	Spec	PASS/FAIL	tm	Min	Max	Mean	Std. Dev.	Cpk
TPLH_1MHz	> 50 ns	PASS	87 ns	66.58 ns	113.7 ns	80.61 ns	3.96 ns	2.57
TPHL_1MHz	> 50 ns	PASS	88.38 ns	66.12 ns	120.7 ns	80.47 ns	3.76 ns	2.7

Table 7: Propagation delay results of proposed glitch filter circuit.

5.2.3 Delay design

This chapter shows the different delay implementations and the simulation results for each delay option. The different delay options are compared and the most suitable delay option is chosen for all I3C I/O options. The selection of the best delay design is based on chip area, current consumption, and delay variation over Corner and Monte Carlo simulations.

			Corner results		Monte Carlo results	
Test names	Spec [Number of Glitches]	PASS/FAIL	Applied Glitches	Unfiltered Glitches	Applied Glitches	Unfiltered Glitches
GLITCH_TST_40ns_INPUT	0	PASS	65	0	1500	0
GLITCH_TST_50ns_INPUT	0	PASS	65	0	1500	0
GLITCH_TST_60ns_INPUT	INFO		65	0	1500	0
GLITCH_TST_70ns_INPUT	INFO		65	6	1500	1
GLITCH_TST_80ns_INPUT	INFO		65	28	1500	294
GLITCH_TST_90ns_INPUT	INFO		65	35	1500	1117
I3C_TST_12.5MHz_INPUT	0	PASS	65	0	1500	0
TSP_ERROR	0	PASS	65	0	1500	0

Table 8: Corner and Monte Carlo results of unfiltered glitches for various test cases.

5.2.3.1 Cascaded inverter stage

The theoretical knowledge of the cascaded inverter stage was presented in Chapter 4.2.1.7.1. The propagation delay of a cascaded inverter stage can be increased by decreasing k_p and k_n, which can be achieved by adjusting the transistor dimension (W/L) [28]. Increasing the length of the PMOS transistor will raise the resistance, which increases the propagation delay of each inverter stage. A higher resistance will increase the time constant τ, which leads to a longer propagation delay of the cascaded inverter circuit. The load capacitance is another option for tuning the propagation delay. The load capacitance is depicted in Figure 64 as MOS capacitors. As already introduced in Chapter 4.2.1.6, NMOS and PMOS transistors are used, to reduce the dependence of capacitance on V_{GS}. In Figure 63 the delay of all inverter stages and the total delay at the output are presented.

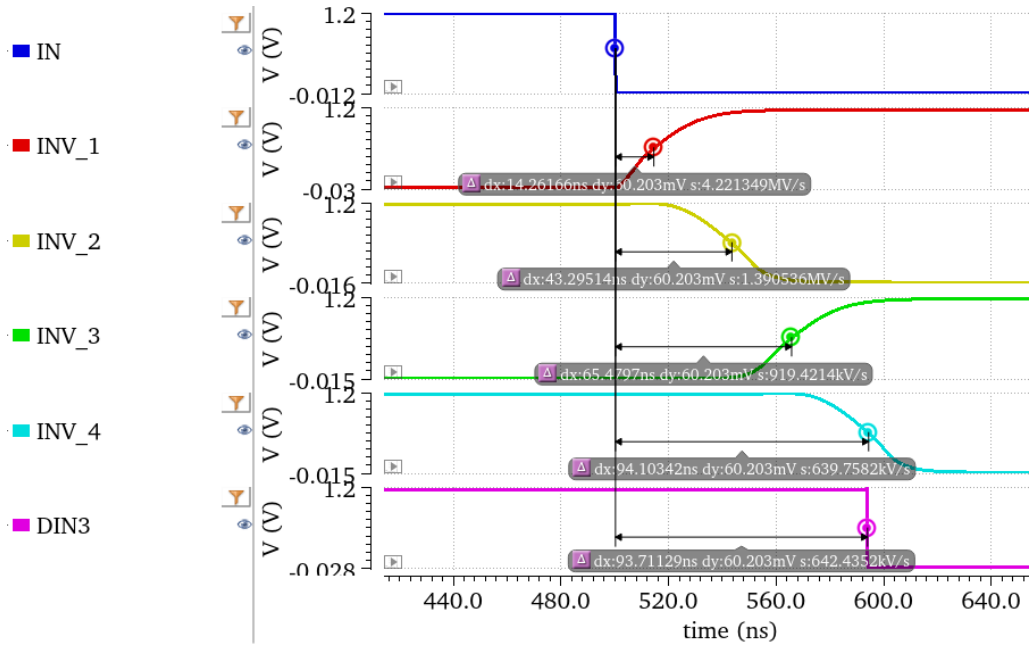

Figure 63: Delay of each inverter stage of the cascaded inverter delay.

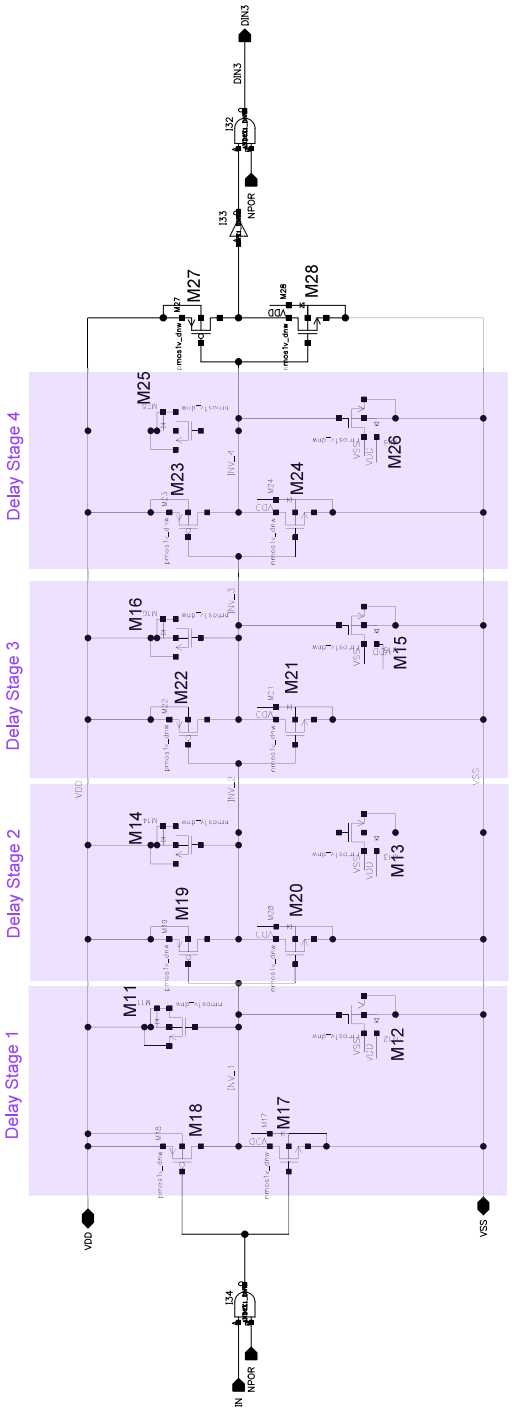

Figure 64: Schematic of the cascaded inverter delay.

5.2.3.2 Thyristor-based Delay

The second delay element is a thyristor-based concept, which was proposed in [38] and shown in Figure 66. Transistors R1 to R5 are responsible for the propagation delay of the rising edge between the input signal *IN* and the output *VOUT* [28]. In the same manner, transistors F1 to F5 participate in delaying the falling edge on the input signal *IN* [28]. The implemented thyristor delay is based on the work of [28] and [26]. The inverter formed by M1 and M2 inverts the input signal *IN* into *INN*. A rising edge on the input node *IN* turns on R1 and discharges $VOUT\_N$ via the Pull-down transistors MP1 and MP2 [28]. When the voltage $VOUT\_N$ decreases to $V_{DD} - |V_{Tp}|$, R3 turns on [28]. R4 is turned on by the inverted input signal *INN*, which charges up *VOUT* over R3 to V_{DD} [28]. Once *VOUT* reaches the threshold voltage of R2, R2 turns on and discharges the MOS capacitors MC3 and MC4 via the transistor R5 [28]. The transistors R2, R3, and R4 form a positive feedback loop [28]. This positive feedback loop results in a fast rising/falling edge to V_{DD}/V_{SS} for $VOUT/VOUT\_N$ [28]. The transistors R5 and F5 are used to reduce the impact of the subthreshold current since the design has a high temperature and process sensitivity [26]. Transistor R5 ensures that the subthreshold current of R3 is sunk through R5 and avoids charging of the node *VOUT* [26]. The same principle can be applied for a falling edge. If a rising edge occurs at the input, F1 to F5 are all turned off [28]. When a falling edge occurs, R1 to R5 are turned off and the same operation is performed by F1 to F5 [28]. The propagation delay of the thyristor-based concept depends mainly on the Pull-down network, formed by the transistors MP1 to MP4 [28]. The Pull-down network determines the discharge current of the MOS capacitors via the transistors MP3/MP4 and MP1/MP2. A higher resistance of the Pull-down network leads to a higher propagation delay between *IN* and *DIN3*. As depicted in Figure 66, the resistance of the Pull-down network was raised by increasing L of MP1 and MP2 [28]. For a larger propagation delay the dimensions of the MOS capacitors MC1 to MC4 can be increased.

The most important aspects in the implementation of the thyristor-based delay element are the transistors MP1 to MP4, which form the Pull-down network, and the MOS capacitors MC1 to MC4. Those transistors are responsible for the propagation delay of this thyristor-based delay element. First, a proper L for the Pull-down transistors MP1 to MP4 must be set. Second, the MOS capacitors MC1 to MC4 dimensions were determined by a parametric sweep of W and L, until a propagation delay between *IN* and *DIN3* of approximately 90 ns was reached. The thyristor-based delay element must be implemented symmetrically, to equalize T_{PLH} and T_{PHL}. The output *DIN3* is set to 1.2 V when $res = \overline{VOUT \cdot IN}$ is fulfilled and set to 0 V when the logic function $set = \overline{VOUT\_N \cdot INN}$ is true. In Figure 65 the relevant nodes are presented and markers indicating T_{PLH} and T_{PHL} are inserted.

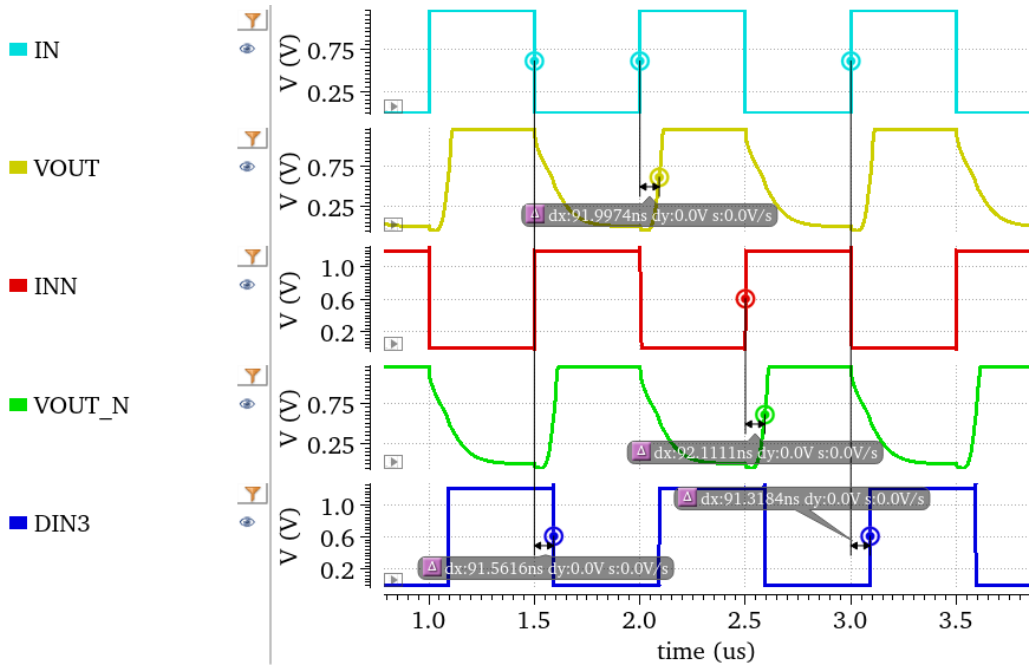

Figure 65: Timing diagram of a thyristor-based delay element.

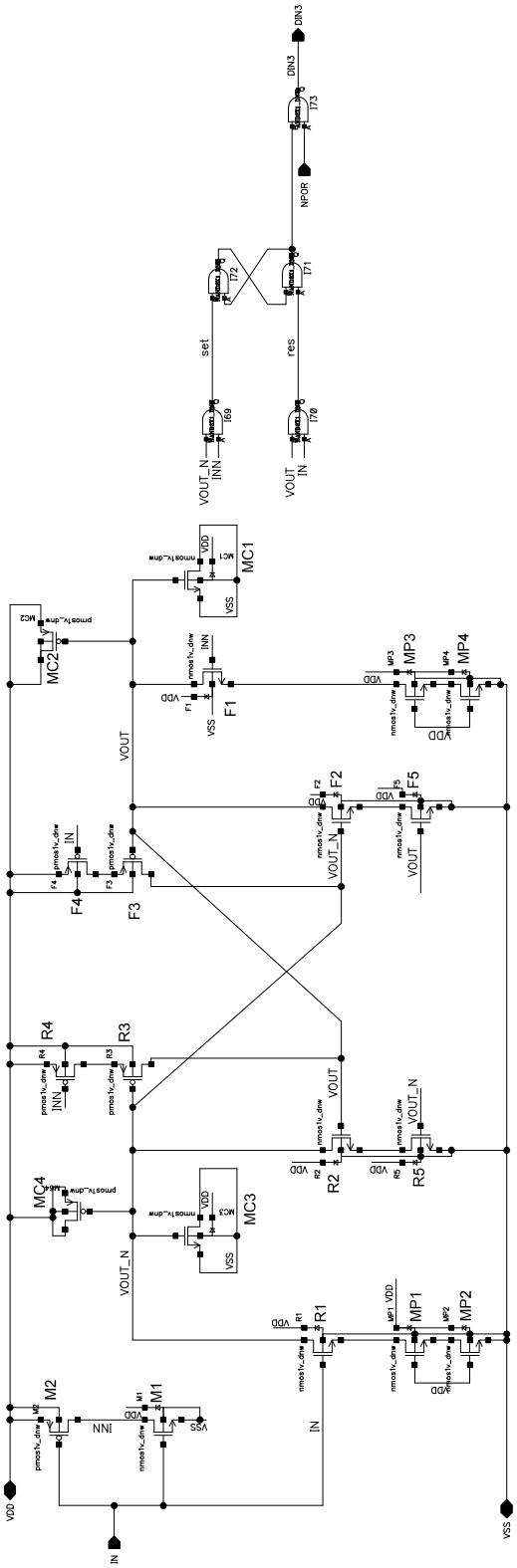

Figure 66: Implementation of a thyristor-based delay.

5.2.3.3 Cascaded glitch filter

The cascaded glitch filter delay is based on two glitch filter circuits, which are presented in Figure 70 and 71. The delay principle is the same as it was introduced in Chapter 4.2.1.6. The first block is delaying the input signal *IN* signal by 45 ns. The output of the first glitch filter block (GLITCH_DELAY_1) is inverted and delayed by the second glitch filter block (GLITCH_DELAY_2) by another 45 ns. The total nominal delay is 90 ns. The only difference is the reset mechanism of the two blocks. A timing diagram of the individual signals is shown in Figure 67 and Figure 68. The reset mechanism of this cascaded glitch filter circuit is shown in Figure 67. If a rising edge is applied to *IN*, the *DL_OUT1* is delayed by 90 ns. The logic function $resh = \overline{INV \cdot DL\_OUT1}$ of *GLITCH_DELAY_1* is true and the node *rcn* is set to *VDD*. The reset mechanism for GLITCH_DELAY_2 works. If the logic function $resh = \overline{INV \cdot DL\_OUT2}$ of *GLITCH_DELAY_2* is true, the node *rcn* is set to *VDD*.

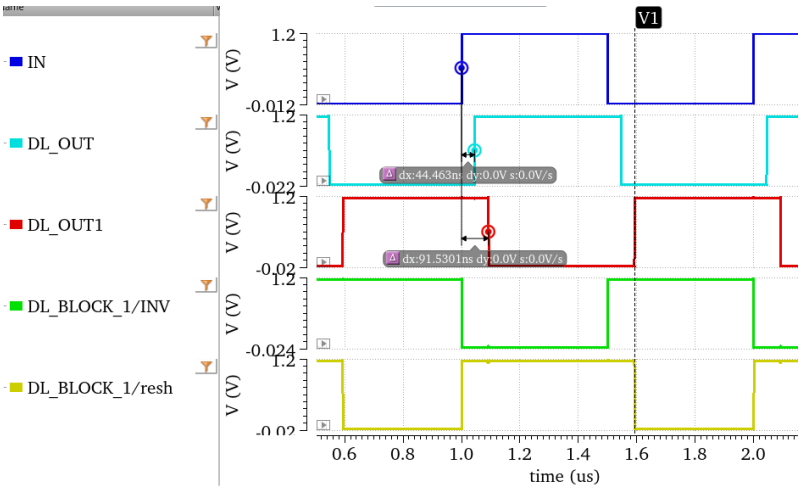

Figure 67: Timing diagram for reset mechanism of GLITCH_DELAY_1.

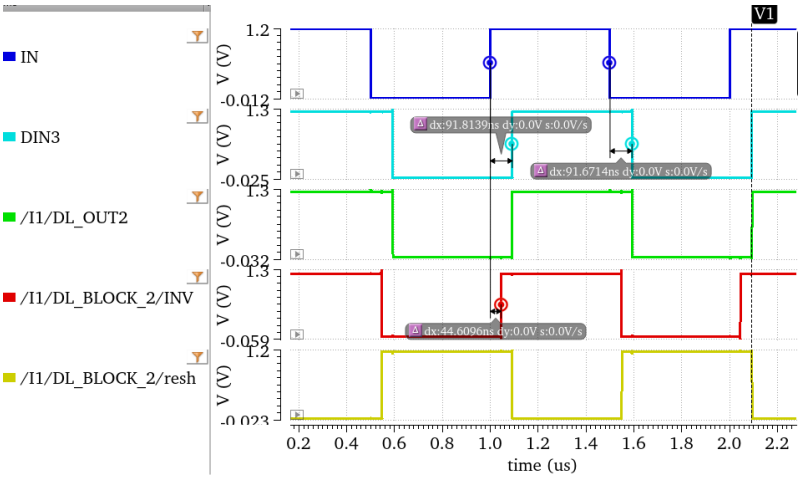

Figure 68: Timing diagram for reset mechanism of GLITCH_DELAY_2.

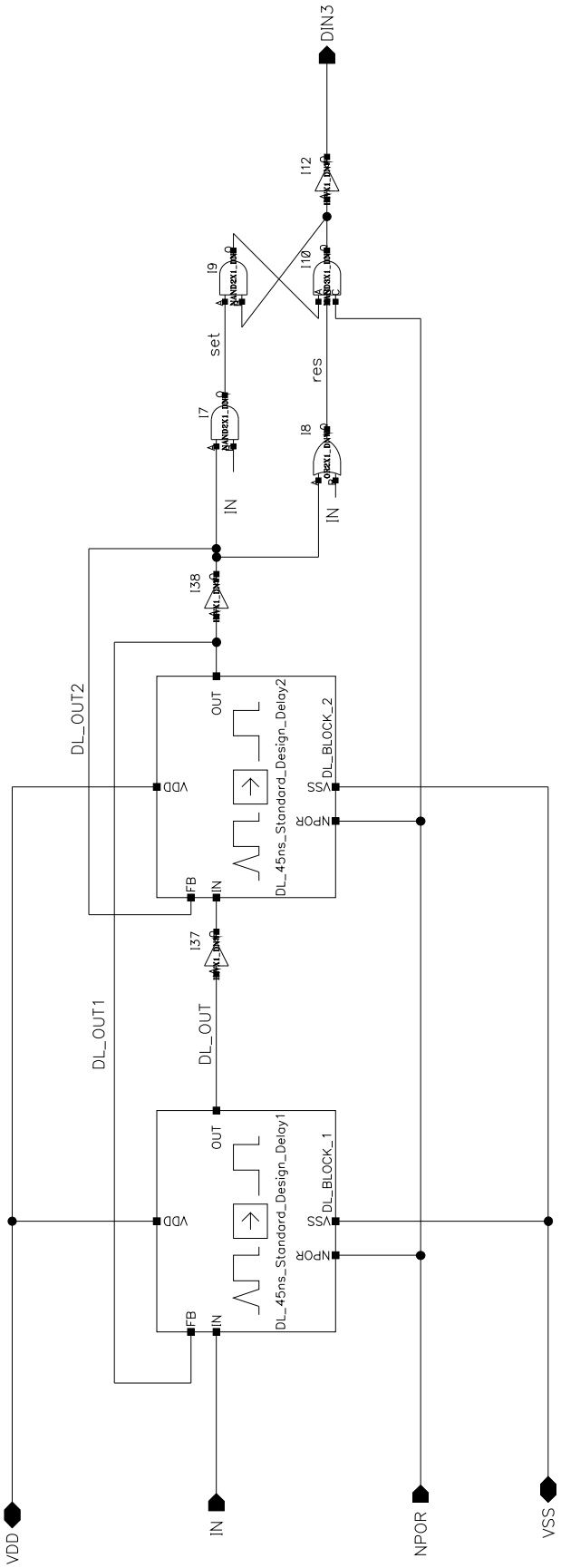

Figure 69: Schematic of a cascaded glitch filter delay.

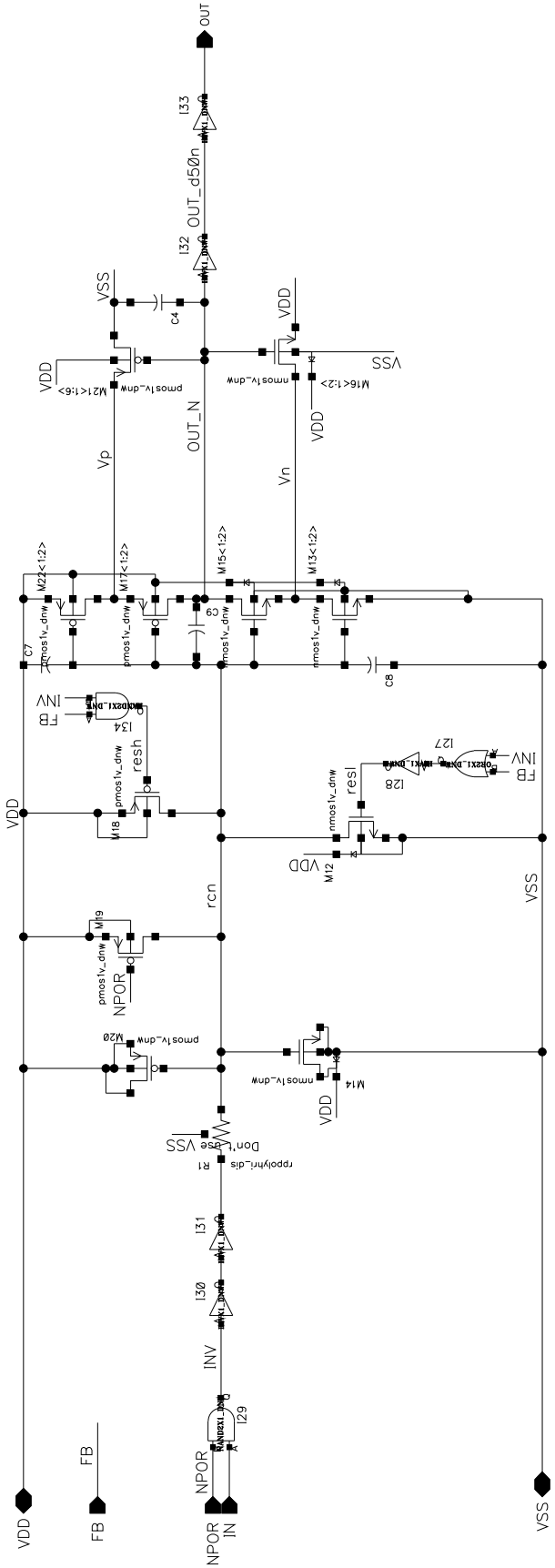

Figure 70: Detailed schematic of the delay DL_BLOCK_1, presented in Figure 69.

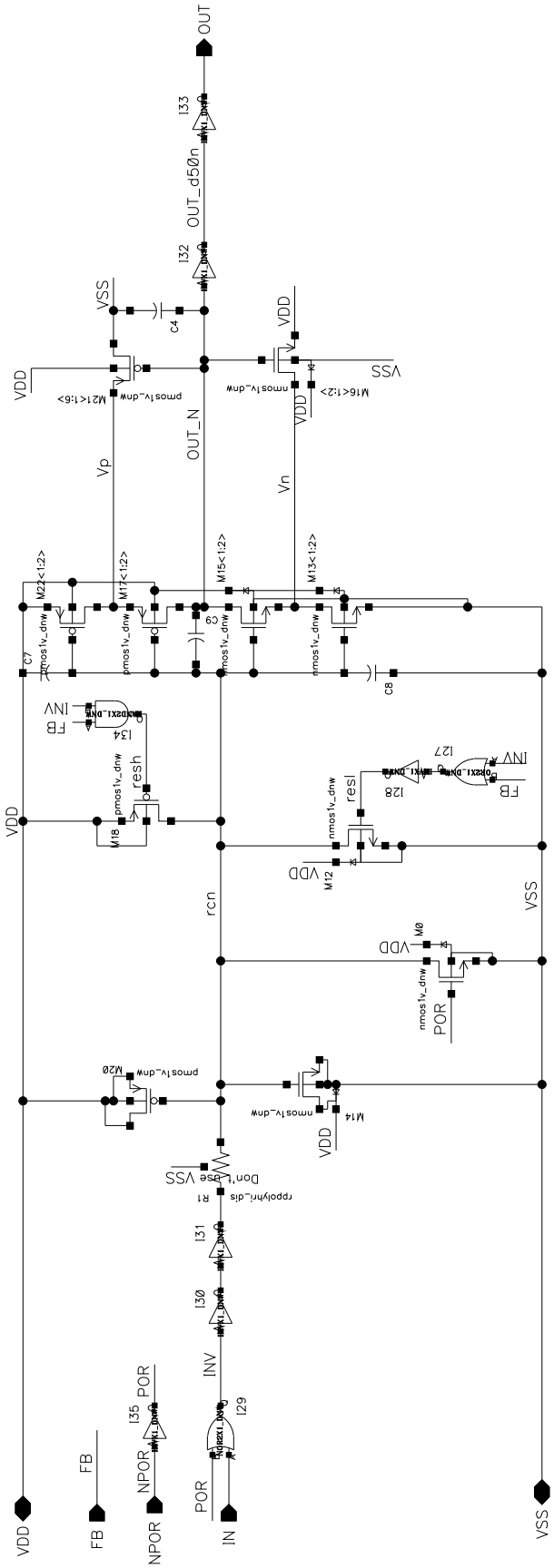

Figure 71: Detailed schematic of the DL_BLOCK_2, presented in Figure 69.

5.2.3.4 Simulation results

The simulation results of all delay implementations are presented in Table 9. The parameters of interest are the propagation delay variation T_{PLH} and T_{PHL}, the average current consumption, and the required chip area (estimated). The thyristor-based delay shows the highest impact on process and mismatch, indicating the lowest Cpk compared to the cascaded inverter and the cascaded glitch filter design. A significant advantage of the thyristor-based delay is the low average current consumption. The cascaded glitch filter implementation is the best design for stability over temperature and supply voltage. A disadvantage of this design is the increased current consumption and a larger area. The third option is the cascaded inverter chain, which is the best compromise regarding propagation delay variation, area, and current consumption. The impact of mismatch and process variation is as low as the result of the cascaded glitch filter design. The cascaded inverter chain was selected as the delay block for the different I/O options from Table 2.

			Thyristor						Cascaded Inverter						Cascaded Glitch Filter					
Parameters	Spec	PASS/FAIL	tm	MIN	MAX	Mean	Std. dev	Cpk	tm	MIN	MAX	Mean	Std. dev	Cpk	tm	MIN	MAX	Mean	Std. dev	Cpk
T_{PLH}	>50 ns	PASS	91.26 ns	51.77 ns	170.7 ns	63.22 ns	2.39 ns	1.85	91.26 ns	57.1 ns	174.6 ns	65.53 ns	1.71 ns	3.03	92.27 ns	70.67 ns	119 ns	85.28 ns	3.81 ns	3.09
T_{PHL}	>50 ns	PASS	91.56 ns	52.01 ns	167.5 ns	63.47 ns	2.40 ns	1.87	93.7 ns	59.43 ns	171.2 ns	67.87 ns	1.89 ns	3.14	91.69 ns	70.22 ns	120.6 ns	84.84 ns	3.85 ns	3.02
$\overline{I_{DD}}$		INFO	587.5 nA	420 nA	1.73 uA	959.2 nA	55.73 nA	-	1.74 uA	1.36 uA	2.91 uA	2.28 uA	42.42 nA	-	7.32 uA	3.31 uA	19.44 uA	13.92 uA	978.8 nA	-
Area Estimation		INFO	707.56 μm^2	-	-	-	-	-	961 μm^2	-	-	-	-	-	1253 μm^2	-	-	-	-	-

Table 9: Simulation results for all different three delay implementations.

5.3 Data Out Path

In this chapter, the implementation of the blocks in the *DATA_OUT_PATH* will be shown. The individual subcircuit explanations of the *DATA_OUT_PATH* will be based on the *I3C_I2C_Fm+_1V2* and the *I3C_Fm+_3V3_V_B3V3* option which are depicted in Figure 75 and 74, respectively. For better clarity, the output driver is split up into smaller subcircuits, which are highlighted in Figure 75 and 74. Those subcircuits of the output path include the non-overlapping logic block, a PMOS output driver, an NMOS output driver, a PMOS pre-driver circuit, a modular driver extension for Fm+ application, and ESD dummies to fulfill the ESD requirements.

The symbol of the *I3C_I2C_Fm+_1V2* output driver is shown in Figure 72. It is supplied via *vddr*, used as a core supply, and *vddo*, used as periphery supply and ESD rail, which was discussed in Chapter 2.2. The *vddr* and the *vddo* rail are at 1.2 V. Two control signals are used for the I2C application. *I2C_EN* is used to set the pad into I2C Fm mode. It is possible to choose the Fm+ mode with *FM_PLUS_EN*. Subsequently, the output data enters the output driver via the *DOUT* pin. *FSC* is the fail save control signal which is used to control all pre-driver inputs to *gndr* when the pad operates in failsafe mode.

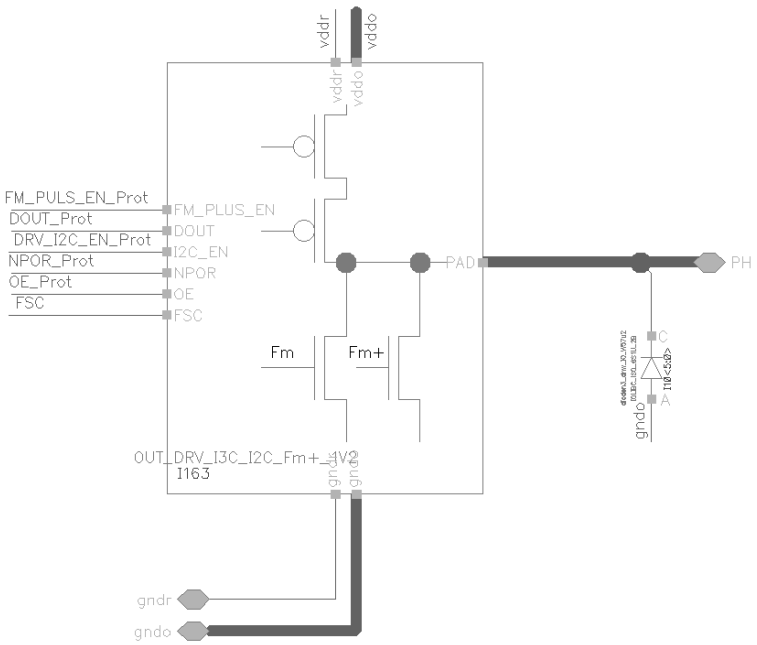

Figure 72: Symbol of the I3C_Fm+_1V2 output driver.

The symbol of the *I3C_Fm+_3V3_V$_B$3V3* output driver is depicted in Figure 73. The output driver has three supply domains. The bus voltage is available via a *VDDIO* pin and supplies *vddr3V3* and *vddo3V3*. The *vddr1V2* supply domain is used to supply the core circuitry. In addition, the inherent failsafe concept of the *I3C_Fm+_3V3_V$_B$3V3* output driver does not have a *FSC* signal since the output driver is inherent failsafe.

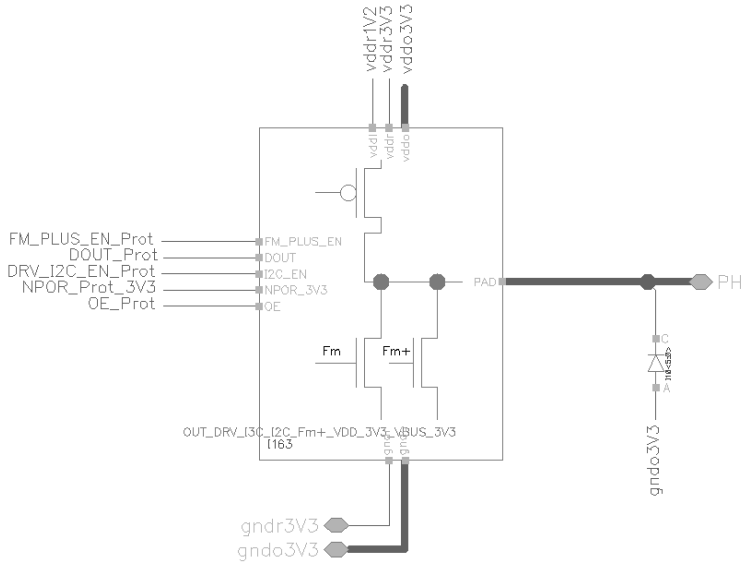

Figure 73: Symbol of the I3C_Fm+_3V3_V$_B$3V3 output driver.

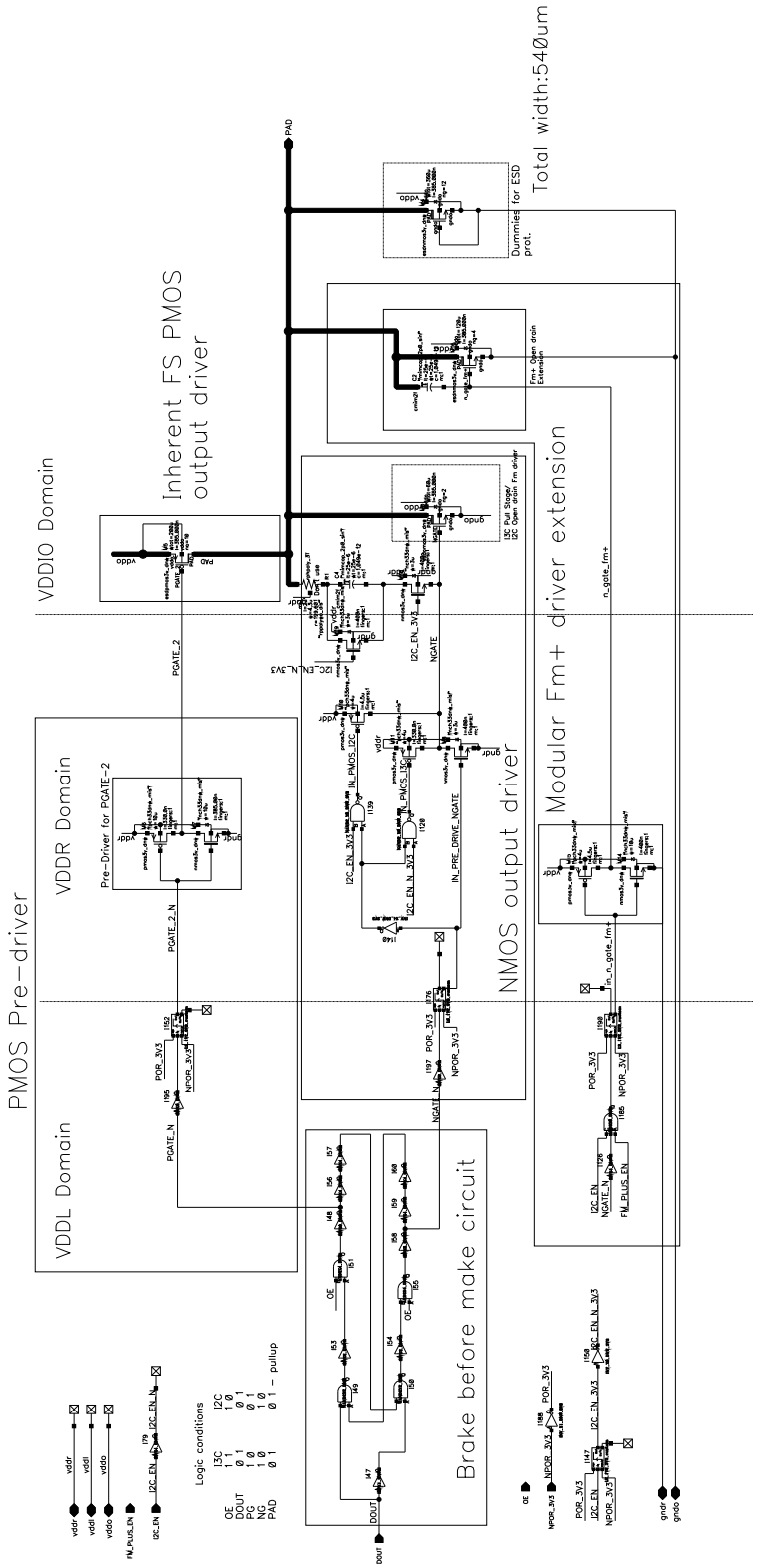

Figure 74: Schematic of the I3C_Fm+_3V3_V_B3V3 output driver.

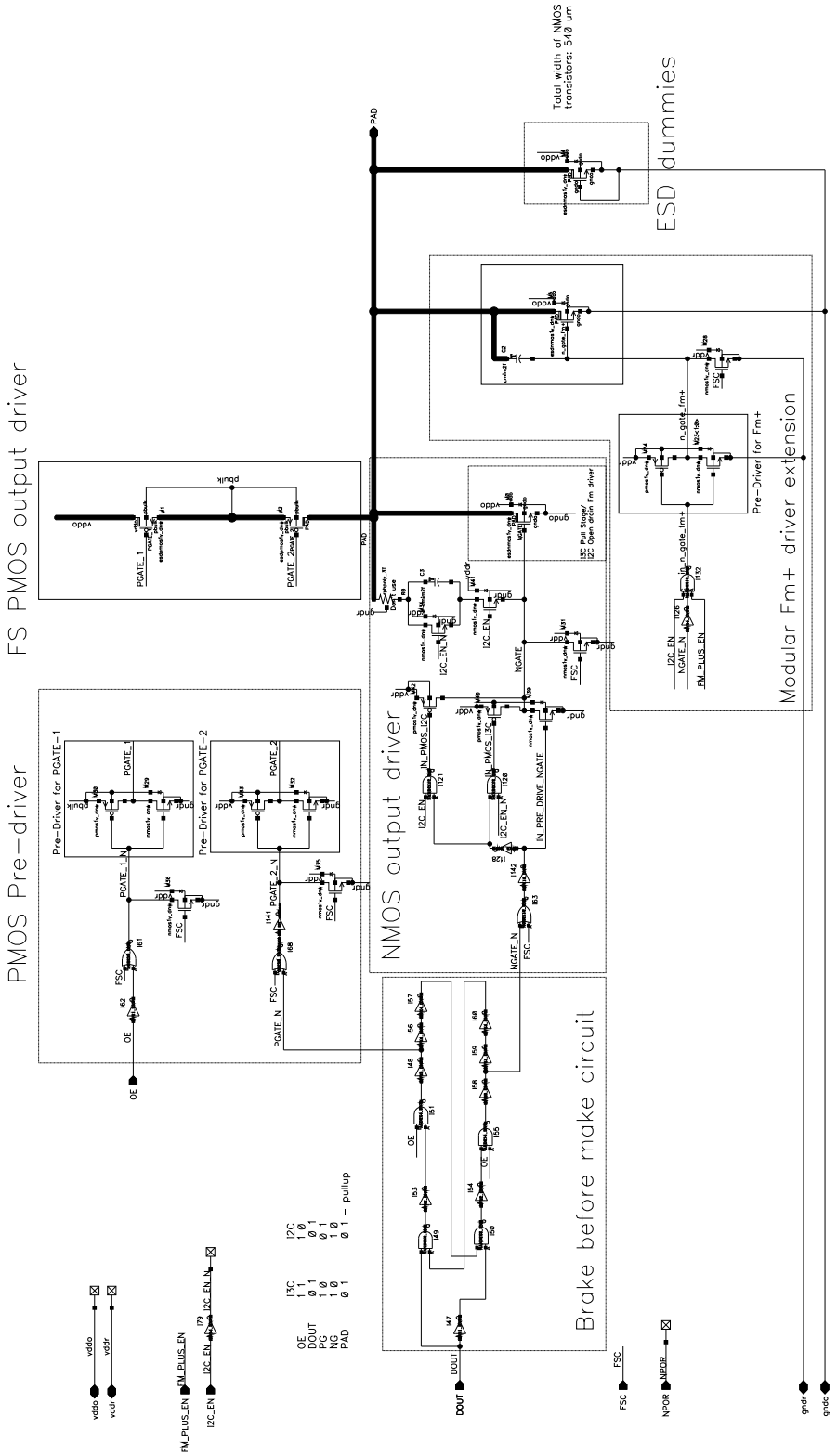

Figure 75: Schematic of the I3C_Fm+_1V2 output driver.

5.3.1 Non-overlapping control logic

The first subcircuit of the output driver is a non-overlapping logic. The non-overlapping control logic is based on the work of [20]. This subcircuit is present in every I/O option from Table 2. This implies, that the non-overlapping logic is not part of the modularity concept. The non-overlapping logic avoids M2 and M0 being turned on simultaneously, which was introduced in Chapter 4.2.2.1. The basic principle is a S-R flip-flop with series inverters. The series inverters are adding the required delay before the signals are fed back to the NAND gates. The delay of the signals *NGATE_N* and *PGATE_N* is shown in Figure 77. The whole signal path from *DOUT* to *PGATE_N* and *NGATE_N* must be designed, such that the propagation delay of this signal path is as small as possible. In addition, the Output Enable signal (OE) is used to control *NGATE_N* and *PGATE_N* in I2C and I3C mode. A logic table for I3C and I2C mode is present in the schematic of Figure 76.

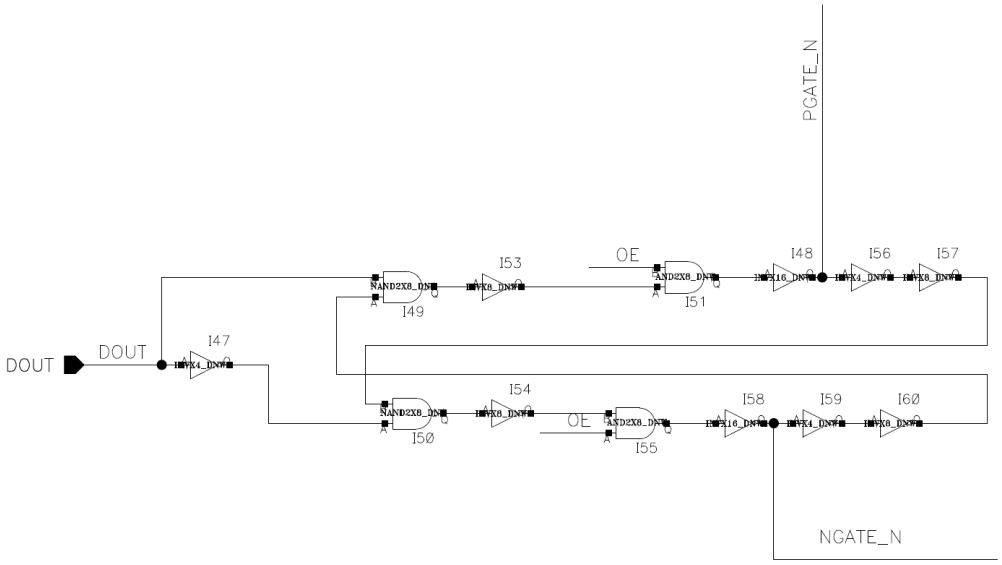

Figure 76: Non-overlapping logic circuit from the I3C_I2C_Fm+_1V2 I/O option.

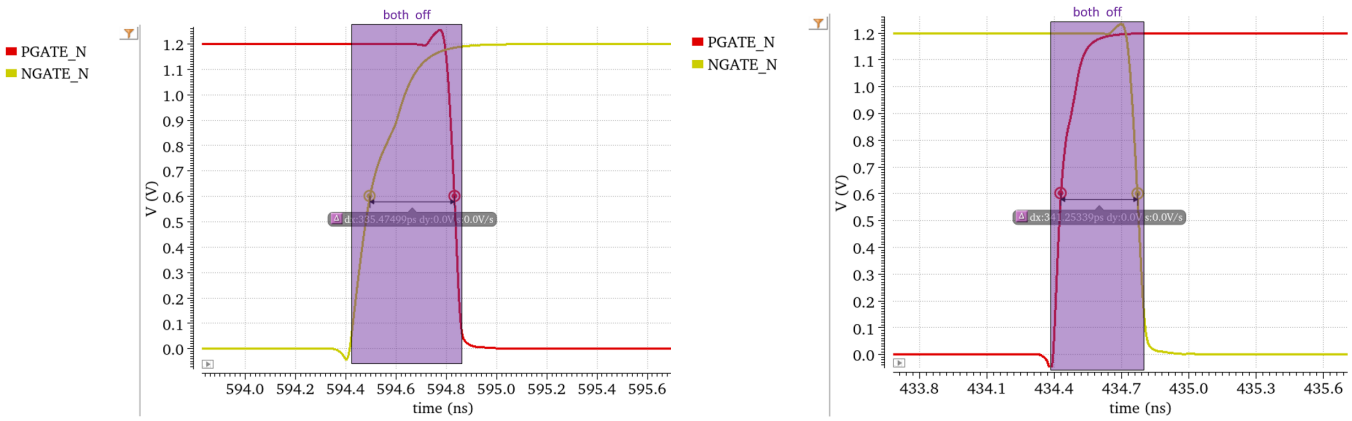

Figure 77: Propagation delay between *NGATE_N* and *PGATE_N*.

5.4 Pre-driver

The signals *NGATE_N* and *PGATE_N* from the non-overlapping gate driver are connected to the pre-driver logic and the pre-driver itself. Three different implementations for the pre-driver must be taken into account.

5.4.1 I3C_Fm_1V2 Pre-driver

Directly attached to the non-overlapping logic is the Gate driver for the output driver. The pre-driver is needed to drive the gate capacitance of the two PMOS transistors M1 and M2, shown in Figure 86. The whole signal chain before the pre-driver is of high importance. Each gate starting from *DOUT* must be capable of driving its output load. The propagation delay from *DOUT* to the input *PGATE_1_N* and *PGATE_2_N* must be minimized since this path is part of the total round trip delay t_{sco}. The FSC signal is connected to the transistors M36 and M35, which drive the input signals *PGATE_1_N* and *PGATE_2_N* to *gndr*. This is necessary to turn on the pre-driver and set the signals *PGATE_1* to *pbulk* and *PGATE_2* to *vddr*. Pulling *PGATE_1* to *pbulk* assures that no backbiasing occures while $vddr/o = 0$ V and $V_{BUS} > 0$ V. The *pbulk* node follows the higher voltage node, either *vddo* or the pad.

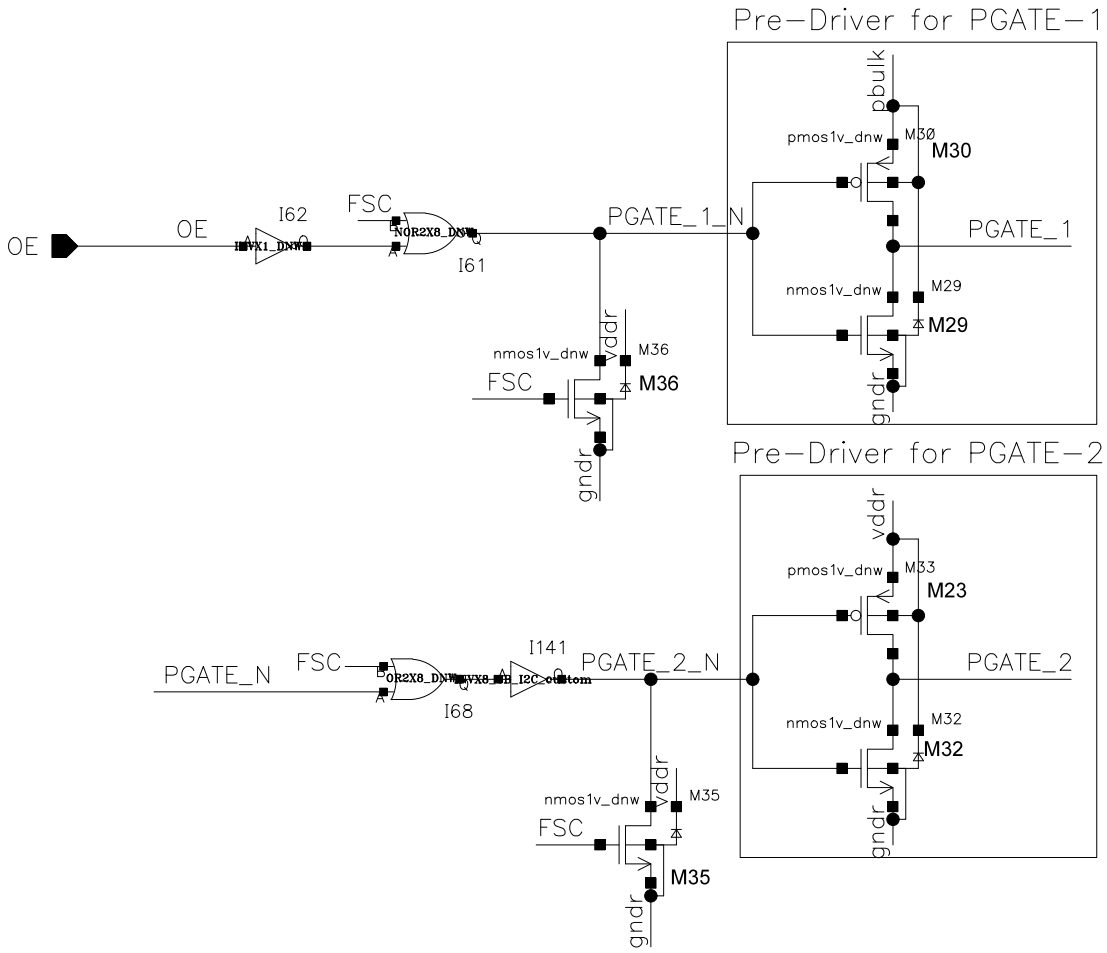

Figure 78: Pre-driver for the PMOS output driver of the I3C_Fm+_1V2 I/O option.

The following describes the Pull part of the output driver. The NMOS transistor M0 is used for I3C and I2C Fm mode. In I2C Fm mode the I2C specification requires a minimum fall time to pull down the I2C bus. This is accomplished with a slope control which is enabled in I2C mode and disabled in I3C mode. The slope control is implemented with a simple RC network consisting of the R_{on} of M42 and the MIM (Metal Insulator Metal) capacitor $C3$. In I2C mode M42 and M41 are turned on. The length of M42 must be high in order to achieve a sufficiently high R_{on} of the transistor. The poly resistor $R0$ is needed to protect M34 from an ESD event. In the case of an I3C application, M40 is turned on since the I3C specification does not require a minimum fall time of the bus. This implies that the length of the transistor M40 must be the smallest possible. Furthermore, the capacitance $C3$ is shorted, to prevent a SOAC violation on transistor M41 when the I3C I/O operates in the I3C mode.

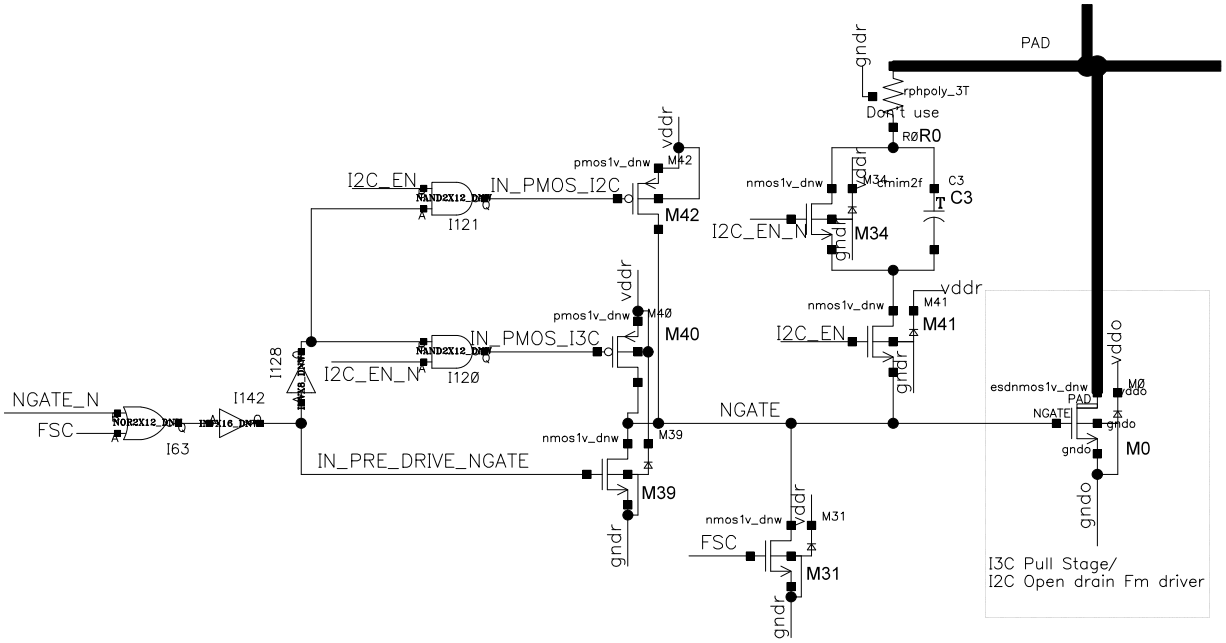

Figure 79: Pre-driver for the NMOS output driver of the I3C_Fm+_1V2 I/O option.

5.4.2 I3C_Fm+_3V3_V$_B$3V3 Pre-driver

The pre-driver for the I3C_Fm_3V3 option is pretty similar to the I3C_Fm_1V2 option. As $V_{BUS} = 3.3$ V, the output driver is implemented with 3.3 V transistors. The pre-driver is also implemented with 3.3 V transistors. Since the core voltage is lower ($vddr1V2 = 1.2$ V), a level shifter is needed to shift the levels from the 1.2 V domain into the 3.3 V domain. The level shifter is marked with $LS1$ in Figure 80. The transition between the 1.2 V and the 3.3 V domain is marked with a dotted line. The nominal voltage of $PGATE\_2\_N$ is 3.3 V. The inverter formed by M6 and M7 must be capable of driving the PMOS output driver connected to $PGATE\_2$, which is presented in Chapter 5.5.3. In addition, no FSC signal is necessary to keep $PGATE\_2\_N$ at 0 V, since the level shifter $LS1$ keeps the $PGATE\_2\_N$ node at 0 V, as long as the POR level is at $vddr3V3 = 3.3$ V. The $vddr3V3$ and the $vddr1V2$ voltage domain must be available for the circuit to become active, which means the POR is set to 0 V.

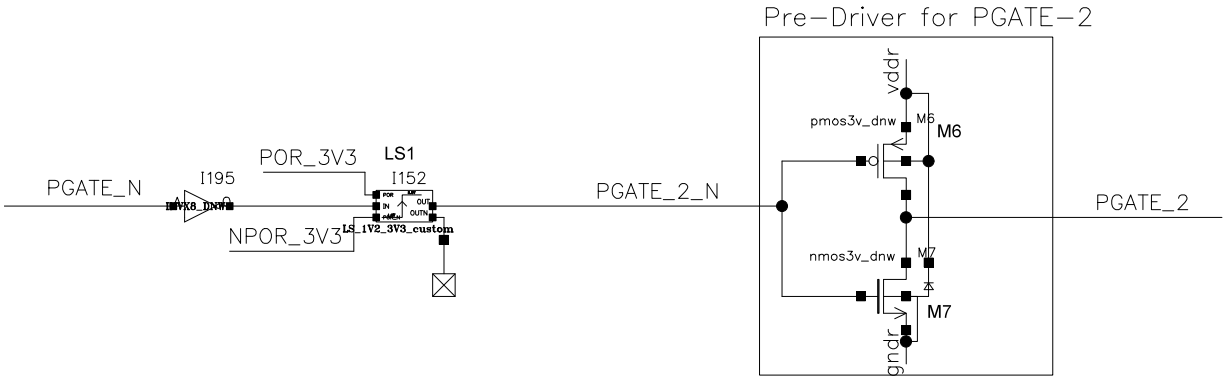

Figure 80: Pre-driver for the PMOS output driver of the I3C_Fm+_3V3_V$_B$3V3 I/O option.

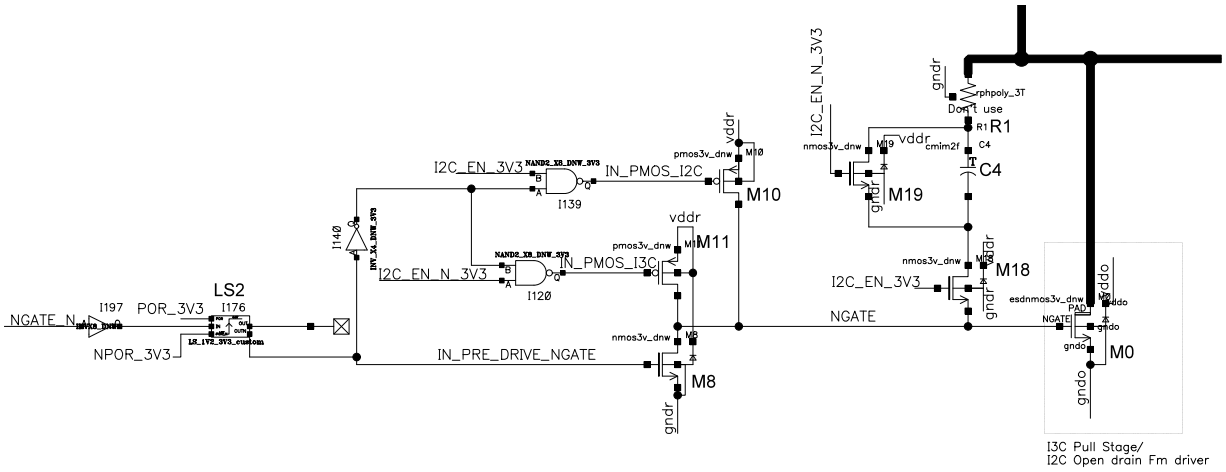

Figure 81: Pre-driver for the NMOS output driver of the I3C_Fm+_3V3_V_B3V3 I/O option.

5.4.3 I3C_Fm+_3V3 Pre-driver

The pre-driver for this variant is significantly different from the I3C_Fm+_3V3 pre-driver implementation, as it requires additional circuitry. The transistors M25 and M26 are added to the pre-driver circuit for the PMOS output driver, shown in Figure 82. In the same manner, M27 is added for the pre-driver circuit for the NMOS output driver. The problem without implementing pre-driver with the *FSC_DEL* signal is depicted in Figure 84. Marker M6 shows a short voltage drop of *PGATE_2*. This voltage drop is caused by the *NPOR* switching when *vddl* reaches approximately $0.9 \cdot vddl$, when the supply (*vddl*) is ramped up. For a short period of time the output of the level shifter is floating. *PGATE_2* is floating and causes that *PGATE_2* sees this voltage drop in the same manner. A short current spike is visible when observing the input leakage. For this reason, the *FSC_DEL* signal is introduced. This *FSC_DEL* assures that the node *PGATE_2* is set to *vddr* when the *NPOR* signal turns on. The input leakage spike is significantly reduced, as shown in Figure 85

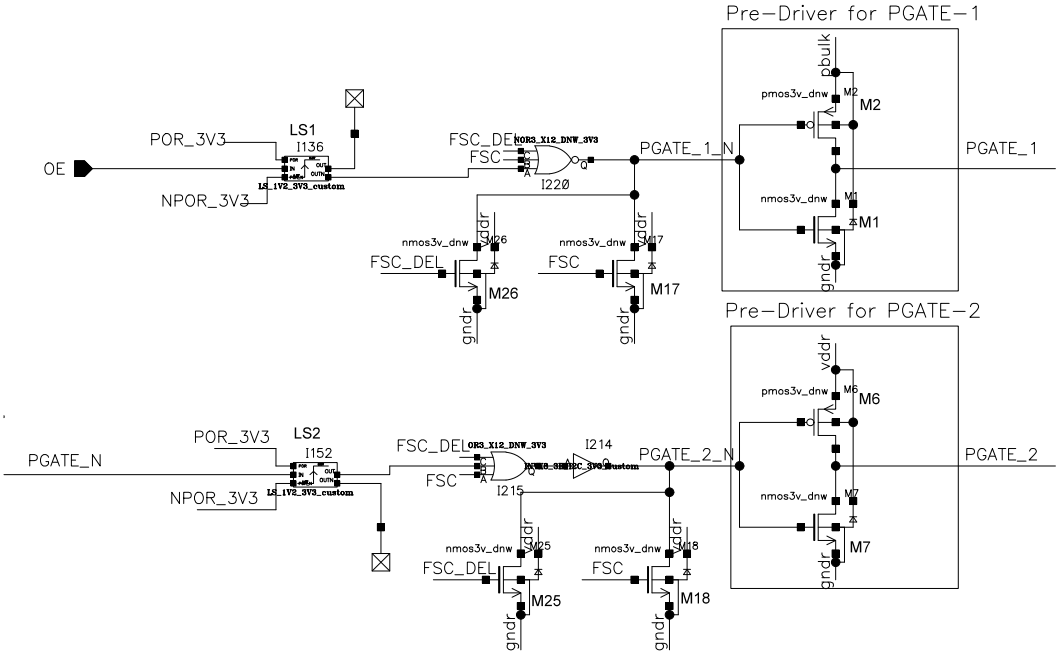

Figure 82: Pre-driver for the PMOS output driver of the I3C_Fm+_3V3 I/O option.

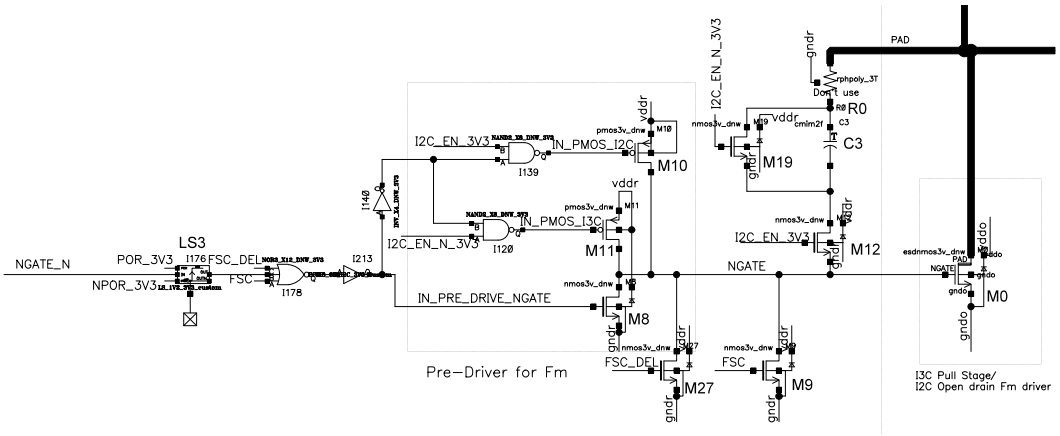

Figure 83: Pre-driver for the NMOS output driver of the I3C_Fm+_3V3 I/O option.

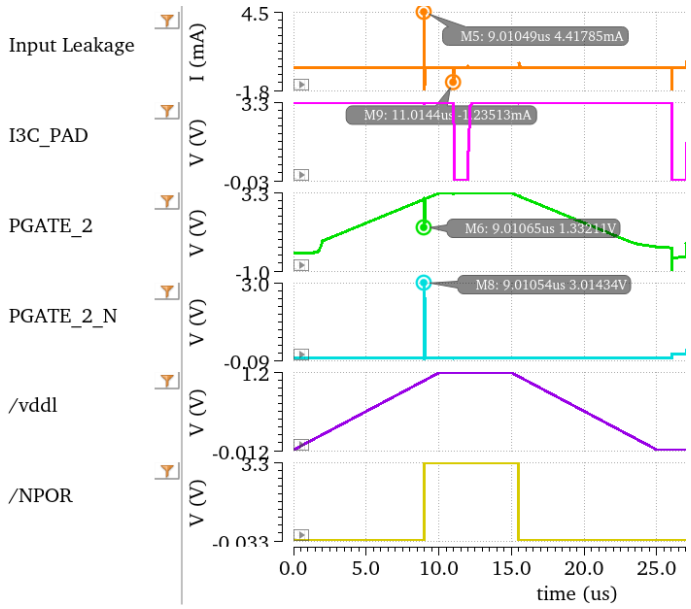

Figure 84: Plot of the failsafe simulation of the I3C_Fm+_3V3 option without the additional FSC_DEL signal.

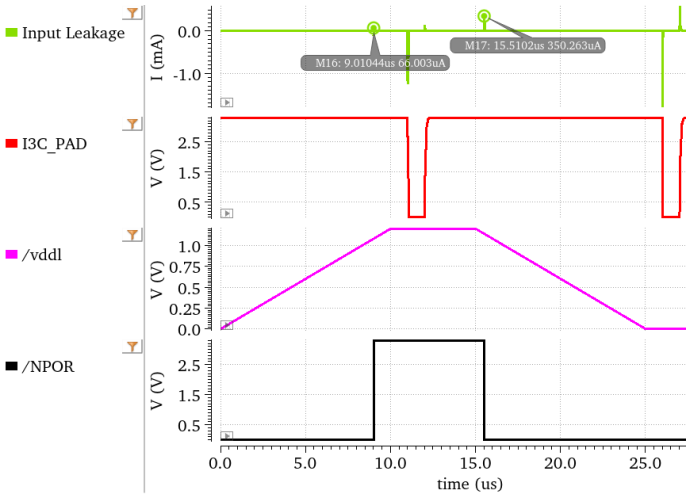

Figure 85: Pre-driver for the PMOS output driver of the I3C_Fm+_3V3 option.

5.5 Output Driver

The modular output driver blocks, which are depicted in Figure 22 will be examined based on the 1.2 V options from Table 2.

5.5.1 I3C with Failsafe

Designing the output driver is rather straightforward. For better readability, the PMOS and NMOS part of the Push-Pull driver is separated. The output driver acts like a switch in the linear region. The switch has a non-zero R_{on}, as it is stated in (6) in Chapter 4.2.1.5. Starting with the Push part of the output driver, a low R_{on} is reached by increasing the width of transistors M1 and M2, which is shown in Figure 81. The bulk contacts of the back-to-back connected transistors M1 and M2 are connected to the source of the transistor M30. This is needed in the failsafe scenario, to keep the $PGATE\_1$ node on the same potential as *pbulk*. The failsafe mechanism is explained in Chapter 4.2.2.2, and is displayed in Figure 87. The plot shows the ramped supply voltage *vddr*, together with the NPOR (Low-Active Power On Reset) which is triggered when the supply voltage *vddr* is ramped up. The Failsafe control (FSC) signal is the inverted $NPOR$ signal. Furthermore, the voltage of the PAD node and input leakage current are displayed in Figure 87. The marker V2 indicates the leakage current when the I3C I/O operates under failsafe conditions. The current is not increasing when the $I3C\_PAD$ is kept static at 1.2 V. The marker V1 shows the input current when the $I3C\_PAD$ is pulled down to VSS. This current spike can be explained by charging/discharging total capacitance on the $I3C\_PAD$.

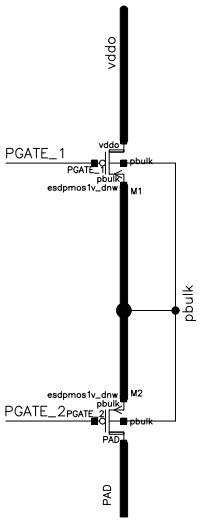

Figure 86: I3C Output driver with back-to-back connected PMOS transistors for the I3C_Fm+_1V2 I/O option.

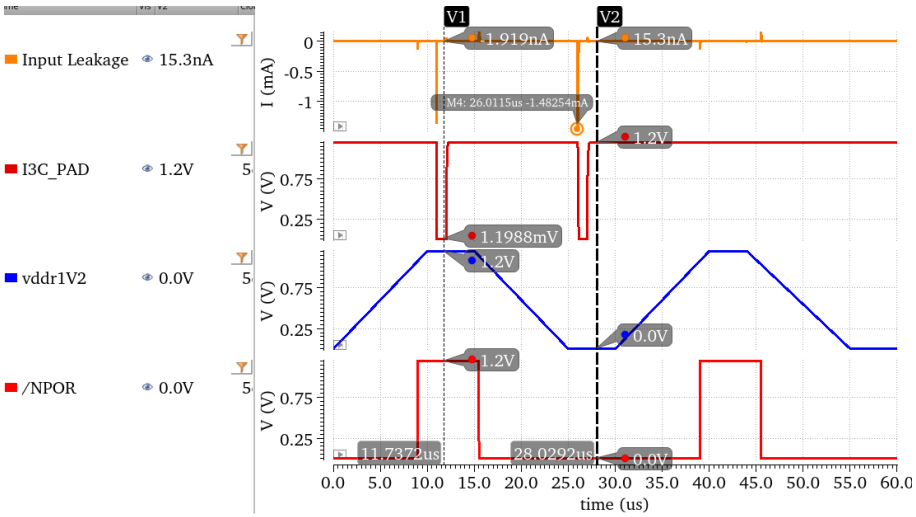

Figure 87: Simulation results for the I3C a failsafe output driver based on the I3C_Fm+_1V2 option.

5.5.2 I2C Fm+

The modular I2C Fm+ driver extension is extending the I2C Fm driver. The Fm+ driver extension can be enabled via the FM_PLUS_EN signal. The output width of M5 must be large enough, to meet the I_{OL} and fall time (t_f) requirements from the I2C specification [5]. The slope control is also required in Fm+ mode, mentioned in Chapter 5.4.1, and must be considered for the Fm+ driver extension. The transistor M24 in Figure 88 must be of the same size as M42 shown in Figure 79. When the I/O operates in I2C Fm+ mode, M5 in Figure 88 is turned on simultaneously with M0 from Figure 79. The fall time t_f should be the same in Fm and Fm+ mode. In addition, the MIM capacitor $C2$, depicted in Figure 88, has the same capacitance as the MIM capacitor $C3$ from the Fm driver, which is presented in Figure 5.4.1.

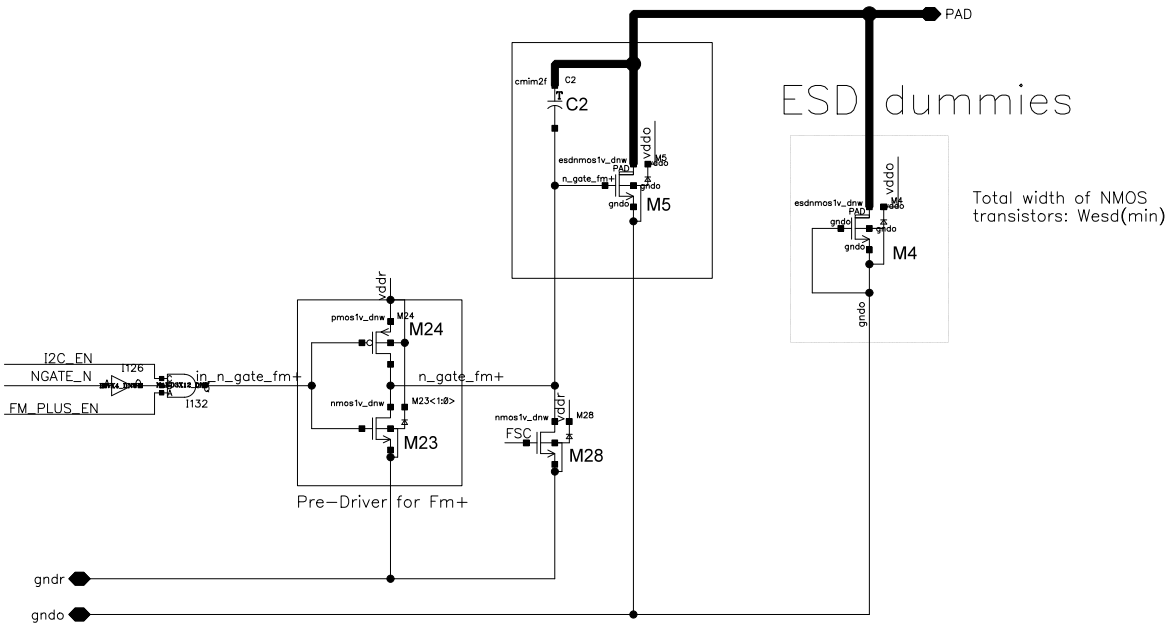

Figure 88: Fm+ Extension for a 1.2 V I/O option.

5.5.3 I3C Inherent Failsafe

The circuit for the inherent failsafe output driver is similar to the circuit shown in Figure 89. Figure 89 shows only the PMOS output driver, since the inherent failsafe concept is only relevant for the PMOS part. As already discussed in Chapter 4.2.2.2.2, the inherent failsafe functionality requires an aligned power concept between the IC and the PCB. The bus voltage is used as a separate voltage domain ($V_{BUS} = vddo$). In Figure 90 the simulation results of the inherent failsafe concept of the output driver are depicted. The input leakage is verified over the whole voltage ramp of *vddr1V2*. The I3C bus, labeled with *I3C_PAD*, is pulled down during the voltage ramp of *vddr1V2*. The marker V1 shows the input current when the $I3C\_PAD$ is pulled down to VSS. This current spike can be explained by charging/discharging total capacitance on the $I3C\_PAD$.

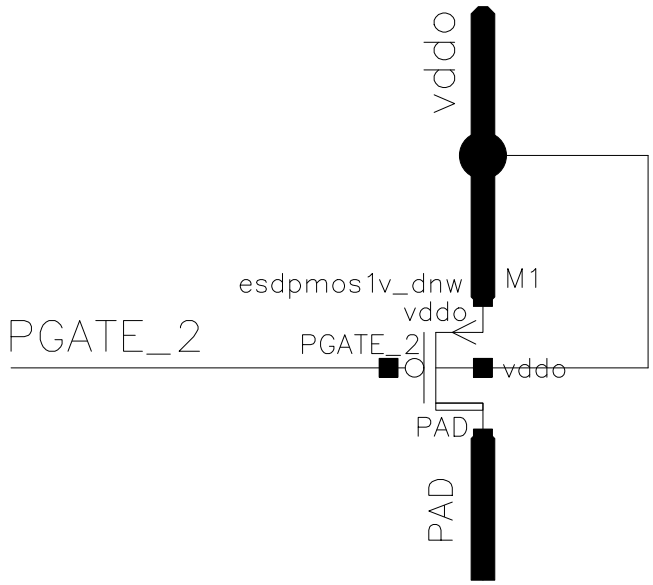

Figure 89: A PMOS output driver with the inherent failsafe concept for the I3C_Fm+_1V2_V_B1V2 option.

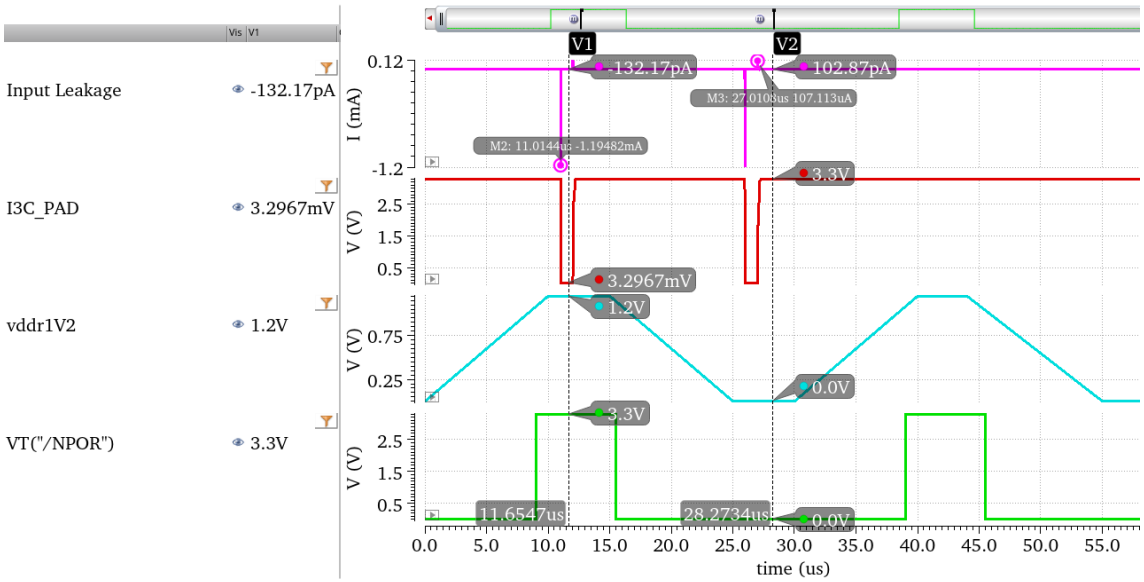

Figure 90: Simulation results for the I3C with FS modular block based on the I3C_Fm+_3V3_V_B3V3 option.

5.5.4 I3C without Failsafe

In case a failsafe functionality is not required, the back-to-back connection of M1 and M2, shown in Figure 78, can be removed. The same output driver from Figure 89 can be used. Unlike the inherent failsafe concept, V_{BUS} via an additional supply pad. The output driver does not meet the failsafe requirements from the MIPI specification.

5.5.5 ESD Dummy Transistor

As already mentioned in Chapter 2.1, an HBM 4 kV requirement of the I3C I/O is needed. Usually, an ESD guideline with the minimum total width of the ESD NMOS devices is provided. The following rule must be fulfilled:

$$\begin{gathered} \mathrm{W}_{tot} = \text{Width of Fm/I3C NMOS} + \text{Width of Fm+ NMOS}, \\ \mathrm{W}_{tot} \geq \mathrm{W}_{ESD}(\mathrm{min}), \\ \\ \mathrm{W}_{tot} = \text{Total width of all ESD NMOS transistors}, \\ \mathrm{W}_{ESD}(\mathrm{min}) = \text{Minimum width of all ESD NMOS devices, stated in the ESD guideline.} \end{gathered} \tag{19}$$

The ESD dummy transistor, depicted in Figure 91, is gate grounded and connected to the ESD rail. The number of units needs to be chosen so that the $W_{ESD}(min)$ requirement is fulfilled.

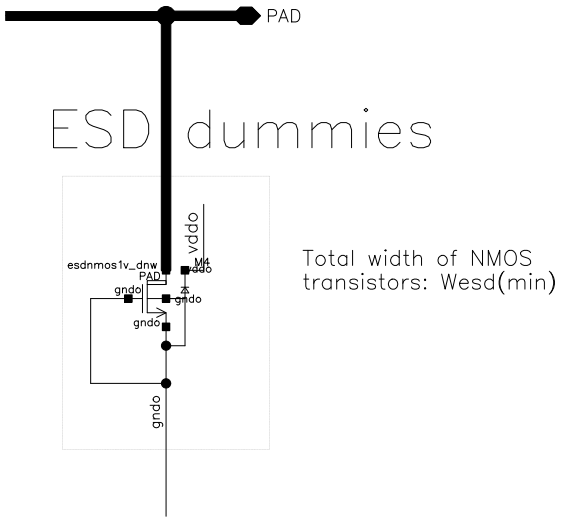

Figure 91: An ESD dummy transistor to meet HBM 4 kV requirement.

6 Implementation of variants

In this chapter, the top-level implementations of the most relevant I/O variants are presented. Since the difference between the Fm and Fm+ options is negligible, the Fm I/O options are not presented in the following chapter. In addition, the major differences between the variants are highlighted. For an overview, not every I/O structure is shown in detail. For every I/O option, a Monte Carlo analysis including mismatch and process with 300 points was performed. In addition, each I3C I/O option was simulated with different load conditions. The load consists of a bus capacitance C_{Load} and a maximum Pull-up resistor for the I2C application. The maximum Pull-up is calculated with (20). The different load conditions are depicted in Table 10. The columns include the maximum Pull-up resistance, which is calculated with (20), the chosen Pull-up resistance R_{PU_Chosen}, the total load capacitance of the bus, and the specification limits for the rise time of the I2C bus t_r. The values for R_{PU_Chosen} are under the maximum Pull-up values since the choice of R_{PU_Chosen} and C_{Load} should not be made within the maximum specification limits. Calculating the R_{PU_MAX} from a minimum and a maximum C_{Load} for I2C Fm mode can be accomplished as follows:

Calculating R_{PU_MAX} with a MIN C_{Load}, presented at index 1 in Table 10,

$$R_{PU\_MAX} = \frac{20 \text{ ns}}{0.8473 \cdot 10 \text{ pF}} = 2.36 \text{ k}\Omega,$$

Calculating R_{PU_MAX} with a MAX C_{Load}, presented at index 3 in Table 10,

$$R_{PU\_MAX} = \frac{300 \text{ ns}}{0.8473 \cdot 385 \text{ pF}} = 919 \ \Omega.$$

(20)

		Index	Combination	R_{PU_MAX}	R_{PU_Chosen}	C_{Load} (C_{BUS} + C_{IN})	MAX C_{Load} from I2C Spec	Rise time t_r
I2C Mode	Fm	1	MIN C_{Load}	2.4 kΩ	2.4 kΩ	10 pF	-	20 ns
		2	MIN C_{Load} and MAX R_{PU}	23 kΩ	20 kΩ	15pF	-	300 ns
		3	MAX C_{Load}	919 Ω	800 Ω	385 pF	400 pF	300 ns
	Fm+	4	MIN C_{Load} and MAX R_{PU}	9.4 kΩ	9 kΩ	15 pF	-	120 ns
		5	MAX C_{Load}	260 Ω	250 Ω	545 pF	550 pF	120 ns

Table 10: Different combinations for C_{load} and R_{PU} for Fm and Fm+ mode.

6.1 I3C_Fm+_1V2 option

The first variant will be discussed in the I3C_Fm+_1V2 option. The top-level schematic in Figure 92 shows the modular and non-modular blocks which are explained in detail in this thesis. The primary ESD protection is implemented with an ESD diode and is sized based on the recommendations of ESD experts. In the same manner, the implementation of secondary ESD protection, which is implemented with a poly-resistor and a GGNMOS, is accomplished. The FSC signal is derived from the ESD-protected PAD node (PAD_PROT). In addition to the examined blocks from the $DATA\_IN\_PATH$ and $DATA\_OUT\_PATH$, ESD interface cells are required. Those interface cells must be added for every I3C I/O input. The input signals of the I3C I/O can come from a core circuitry with a different supply rail. In the case of a CDM test, the whole device is charged up, and different parts of the chip may be discharged faster than others. This can cause an additional voltage drop on the input signals, which can damage the gate oxide of a transistor of the I3C I/O.

The simulation results of the Corner and MC analysis of the I3C_Fm+_1V2 option are depicted in 11. The table is split into two main sections: DC parameters and timing parameters. Those two sections are divided additionally into I2C and I3C-related specification parameters. The Table 11 shows the most important specification parameters from the I2C [5] and the I3C specification from MIPI [9]. Only the parameters relevant to the implementation of an I3C slave device have been used from the specification documents. The columns of the table include the simulation results of the process corner simulation (tm, MIN, MAX) and the results of the MC analysis (Mean, Std. dev, Cpk). For the I3C DC specification parameters, the specification limits are used for $V_{DD} < 1.4$ V [9][p. 136]. For the I2C DC parameters, the specification limits are used for $V_{DD} < 2$ V [5][p. 43]. For further information, the I2C and I3C specifications should be taken into consideration. The voltage-dependent Specification limits in Table 11 are based on the minimum or maximum supply voltage. For the sake of clarity, an example is presented in (21). In the same manner, all other supply voltage-dependent specification limits can be calculated.

$$\begin{gathered}\text{Calculation of the Maximum LOW-level output voltage,} \\ V_{OL} = 0.2 \cdot V_{DD}, \\ \text{Minimum supply voltage } V_{DD\_MIN} = 0.9 \cdot 1.2 \text{ V} = 1.08 \text{ V}, \\ V_{OL} = 0.2 \cdot V_{DD\_MIN} = 180 \text{ mV}.\end{gathered} \tag{21}$$

In addition to these results, two additional tables with the simulation results for the different load conditions for Fm and Fm+ are visible in Table 12 and Table 13. All critical timing parameters for the corner load conditions are within the specification limits.

			Parameters	Spec	PASS/FAIL	tm	MIN	MAX	Mean	Std. dev	Cpk
DC parameters	I3C		I_i	< 5 uA	PASS	546.5 pA	5.22 pA	1.65 µA	278.2 nA	119.4 nA	
			I_{i_FS}	<5 uA	PASS	14.18 nA	10.51 nA	2.55 µA	534.3 nA	144 nA	
			C_i	< 5 pF	PASS	2.9 pF	2.56 pF	3.36 pF	3.0 pF	123.2 fF	
			V_{OL}	< 180 mV	PASS	28.27 mV	18.06 mV	63.69 mV	48.6 mV	3.76 mV	11.6
			V_{OH}	> 900 mV	PASS	1.152 V	998.9 mV	1.29 V	1.02 V	2.72 mV	
			I_{OL}	> 2 mA	PASS	9.30 mA	4.42 mA	14.23 mA	5.86 mA	473 µA	2.72
			I_{OH}	< -2 mA	PASS	-6.90 mA	-10.99 mA	-4.01 mA	-6.5 mA	315.8 µA	4.75
			$V_{TH\_LH\_rel}$	< 70 %	PASS	59.56 %	53.24 %	66.02 %	62.74 %	945.8 m%	2.56
			$V_{TH\_HL\_rel}$	> 30 %	PASS	41.94 %	37.39 %	48.06 %	40.82 %	827.2 m%	4.36
			V_{HYST_rel}	> 10 %	PASS	17.62 %	10.82 %	23.57 %	12.34 %	428.8 m%	1.82
	I2C	Fm	I_{OL}	> 3 mA	PASS	12.11 mA	6 mA	18.23 mA	8.23 mA	730.9 µA	2.38
			V_{OL}	< 216 mV	PASS	43.29 mV	27.34 mV	76.24 mV	50.08 mV	6.5 mV	
		Fm+	I_{OL}	> 20 mA	PASS	49.37 mA	24.67 mA	74.07 mA	33.68 mA	2.96 mA	1.54
			V_{OL}	< 216 mV	PASS	10.19 mV	6.6 mV	21.7 mV	17.05 mV	1.19 mV	
Timing parameters	I3C		t_{sco_rise}	< 12 ns	PASS	7.15 ns	5.64 ns	10.24 ns	ns	212.4 ps	6.43
			t_{sco_fall}	< 12 ns	PASS	7.17 ns	5.69 ns	10.22 ns	7.9 ns	209.6 ps	6.5
			t_{CR}	< 12 ns	PASS	1.83 ns	1.1 ns	3.22 ns	7.92 ns	139.9 ps	23.5
			t_{CF}	<12 ns	PASS	1.97 ns	1.42 ns	3.63 ns	2.63 ns	236.7 ps	13.2
	I2C	Fm	t_{fCL}	3.93 - 300 ns	PASS	19.45 ns	10.85 ns	39.21 ns	2.14 ns	1.46 ns	
			t_{VD_rise}	< 450 ns	PASS	63.89 ns	54.35 ns	75.12 ns	69.43 ns	1.3 ns	
			t_{VD_fall}	< 450 ns	PASS	52.38 ns	28.23 ns	100.6 ns	80.09 ns	4.56 ns	
		Fm+	t_{fCL}	3.93 - 300 ns	PASS	19.16 ns	10.68 ns	37.46 ns	25.91 ns	1.29 ns	
			t_{VD_rise}	< 450 ns	PASS	73.09 ns	68.88 ns	79.62 ns	75.52 ns	598.8 ps	
			t_{VD_fall}	< 450 ns	PASS	59.46 ns	35.78 ns	106.7 ns	77.04 ns	3.92 ns	

Table 11: Simulation results of the I3C_Fm+_1V2 option.

			$C_{BUS} = 10$ pF, $R_{PU} = 20$ kΩ			$C_{BUS} = 10$ pF, $R_{PU} = 2.4$ kΩ			$C_{BUS} = 380$ pF, $R_{PU} = 800$ Ω		
Parameters	Spec	PASS/FAIL	tm	MIN	MAX	tm	MIN	MAX	tm	MIN	MAX
t_{fcl}	3.93 - 300 ns	PASS	17.39 ns	10.41 ns	31.96 ns	17.71 ns	10.6 ns	33.96 ns	26.79 ns	15.6 ns	56.06 ns
t_{rCL}	< 300 ns	PASS	215.2 ns	208.4 ns	223.4 ns	26.93 ns	26.25 ns	27.68 ns	259.4 ns	259.1 ns	259.7 ns
t_{VD_rise}	< 450 ns	PASS	321.1 ns	304.6 ns	341 ns	40.31 ns	30.66 ns	52.04 ns	365.7 ns	353.9 ns	376.6 ns
t_{VD_fall}	< 450 ns	PASS	31.41 ns	13.8 ns	57.28 ns	49.28 ns	26.13 ns	90.25 ns	66.69 ns	37.66 ns	132.9 ns

Table 12: Timing simulation results of the Fm driver for different load conditions.

			$C_{BUS} = 10$ pF, $R_{PU} = 9$ kΩ			$C_{BUS} = 540$ pF, $R_{PU} = 250$ Ω		
Parameters	Spec	PASS/FAIL	tm	MIN	MAX	tm	MIN	MAX
t_{fcl}	3.93 - 300 ns	PASS	17.45 ns	10.46 ns	32.38 ns	26.15 ns	13.64 ns	57.31 ns
t_{rCL}	< 120 ns	PASS	96.85 ns	94.49 ns	99.63 ns	114.9 ns	114.8 ns	115 ns
t_{VD_rise}	< 450 ns	PASS	156.7 ns	149.5 ns	166.8 ns	170.6 ns	165.8 ns	176.2 ns
t_{VD_fall}	< 450 ns	PASS	56.41 ns	34.41 ns	96.86 ns	76.41 ns	44.18 ns	149.8 ns

Table 13: Timing simulation results of the Fm+ driver for different load conditions.

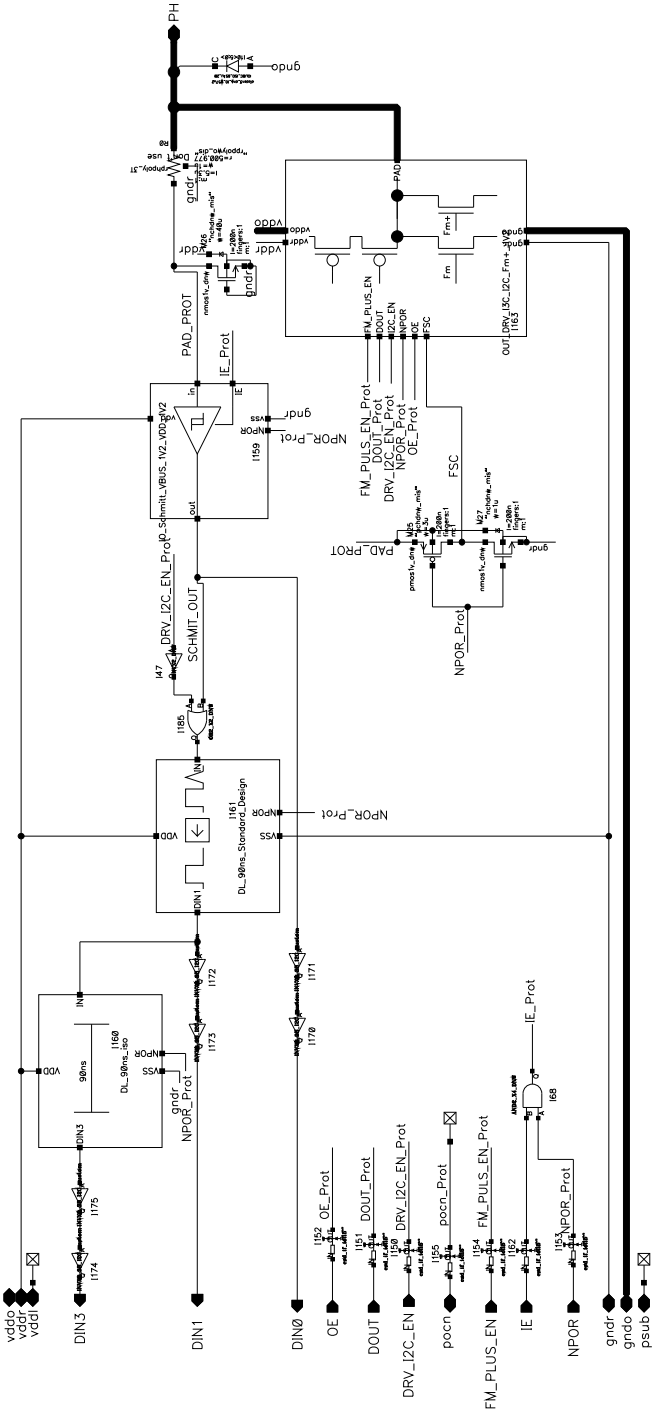

Figure 92: Top level schematic of the I3C_Fm+_1V2 option.

6.2 Implementation of I3C_Fm+_1V2_V_B1V2 option

The I3C_Fm+_1V2_V_B1V2 option differs from the I3C_Fm+_1V2 option in the output driver block and in the supply concept, which is highlighted in red in Figure 93. The biggest difference is the output drive, the power supply concept, and the ESD interface cells. Since this implementation is an inherent failsafe, the V_{BUS} domain from the PCB is connected to *vddo* and *vddr*. The ESD interface cells are exchanged by a level shifter with a failsafe ESD protection. Since the whole I3C I/O is inherent failsafe, the ESD interface protection in the level shifter must be failsafe as well. The IC must not be back powered by the ESD protection. The level shifter with the ESD interface protection is depicted in Figure 94.
The simulation results depicted in Table 14 are within the specification limits and marked with PASS. Since the NMOS output driver for the I3C_Fm+_1V2_V_B1V2 option is the same as for the I3C_Fm+_1V2 option, no results for the different I2C load conditions for Fm and Fm+ mode are presented.

			Parameters	Spec	PASS/FAIL	tm	MIN	MAX	Mean	Std. dev	Cpk
DC parameters	I3C		I_i	< 5 uA	PASS	520.5 pA	4.85 pA	1.63 µA	271.7 nA	119.8 nA	
			I_{IN_FS}	<5 uA	PASS	487.6 pA	2.65 pA	1.62 uA	266.9 nA	123 nA	
			C_i	< 5 pF	PASS	2.75 pF	2.43 pF	3.09 pF	2.78 pF	38.6 fF	
			V_{OL}	< 180 mV	PASS	28.27 mV	18.06 mV	63.68 mV	31.94 mV	48.59 mV	11.6
			V_{OH}	> 900 mV	PASS	1.16 V	1.0 V	1.29 V	1.02 V	2.66 mV	
			I_{OL}	> 2 mA	PASS	9.3 mA	4.42 mA	14.23 mA	5.9 mA	473 µA	2.72
			I_{OH}	< -2 mA	PASS	-6.95 mA	-11.13 mA	-3.97 mA	-6.38 mA	325.4 µA	4.49
			$V_{TH\_LH\_rel}$	< 70 %	PASS	59.56 %	53.45 %	65.92 %	62.73 %	918.2 m%	2.64
			$V_{TH\_HL\_rel}$	> 30 %	PASS	41.94 %	37.39 %	48.05 %	40.83 %	809.2 m%	4.46
			V_{HYST_rel}	> 10 %	PASS	17.62 %	11.01 %	23.51 %	12.34 %	444.9 m%	1.75
	I2C	Fm	I_{OL}	> 3 mA	PASS	12.11 mA	6 mA	18.23 mA	8.23 mA	731 µA	2.38
			V_{OL}	< 216 mV	PASS	43.29 mV	27.34 mV	103.2 mV	76.23 mV	6.5 mV	
		Fm+	I_{OL}	> 20 mA	PASS	49.37 mA	24.67 mA	74.07 mA	33.68 mA	2.96 mA	1.54
			V_{OL}	< 216 mV	PASS	10.19 mV	6.6 mV	21.69 mV	17.05 mV	1.19 mV	
Timing parameters	I3C		t_{sCO_rise}	< 12 ns	PASS	7.43 ns	5.88 ns	10.76 ns	8.22 ns	235.9 ps	5.34
			t_{sCO_fall}	< 12 ns	PASS	7.51 ns	5.91 ns	10.97 ns	8.3 ns	238.6 ps	5.16
			t_{CR}	< 12 ns	PASS	1.95 ns	1.21 ns	3.45 ns	2.29 ns	147.8 ps	21.9
			t_{CF}	<12 ns	PASS	1.97 ns	1.42 ns	3.62 ns	2.63 ns	236.6 ps	13.2
	I2C	Fm	t_{fCL}	3.93 - 300 ns	PASS	19.44 ns	10.84 ns	39.19 ns	27.37 ns	1.42 ns	
			t_{VD_rise}	< 450 ns	PASS	64.11 ns	54.51 ns	75.36 ns	69.65 ns	1.33 ns	
			t_{VD_fall}	< 450 ns	PASS	52.53 ns	28.33 ns	100.8 ns	70.34 ns	4.46 ns	
		Fm+	t_{fCL}	3.93 - 300 ns	PASS	19.17 ns	10.68 ns	37.55 ns	25.94 ns	1.28 ns	
			t_{VD_rise}	< 450 ns	PASS	73.39 ns	69.17 ns	80.25 ns	75.86 ns	623.6 ps	
			t_{VD_fall}	< 450 ns	PASS	59.68 ns	35.91 ns	107.1 ns	77.41 ns	3.86 ns	

Table 14: Simulation results of the I3C_Fm+_1V2_V_B1V2 option.

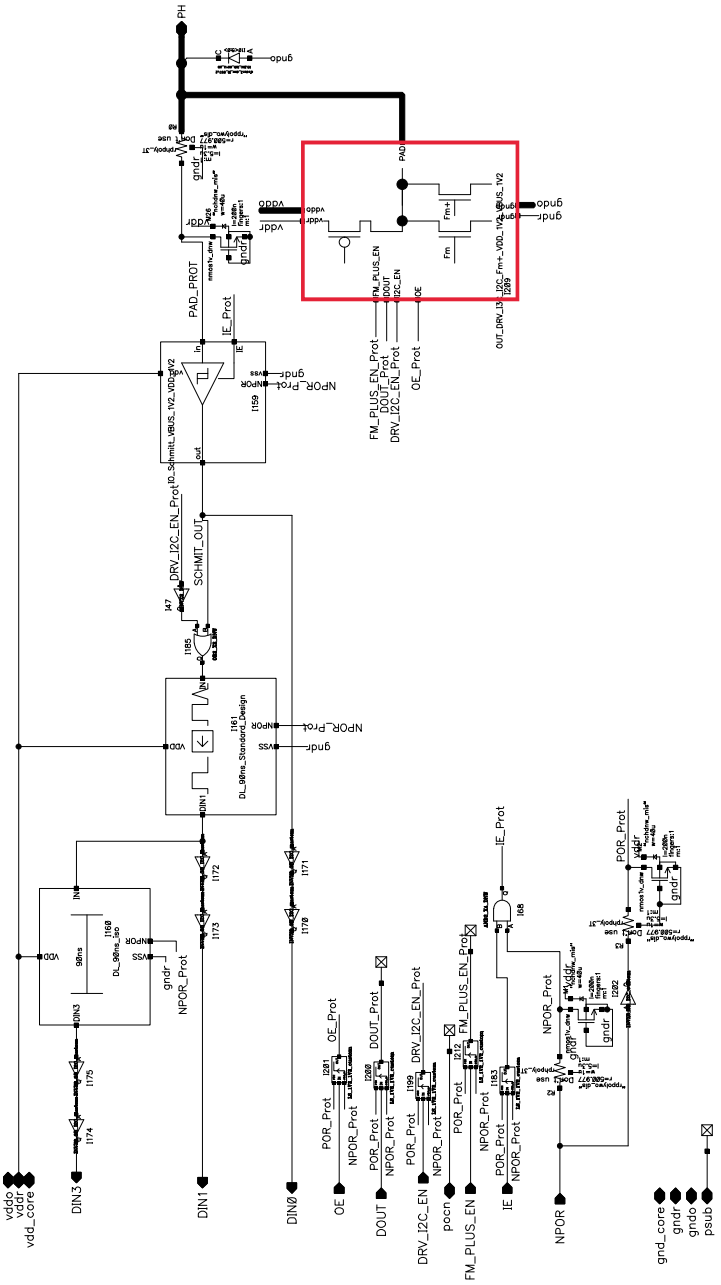

Figure 93: Top level schematic of the I3C_Fm+_1V2_V$_B$1V2 option.

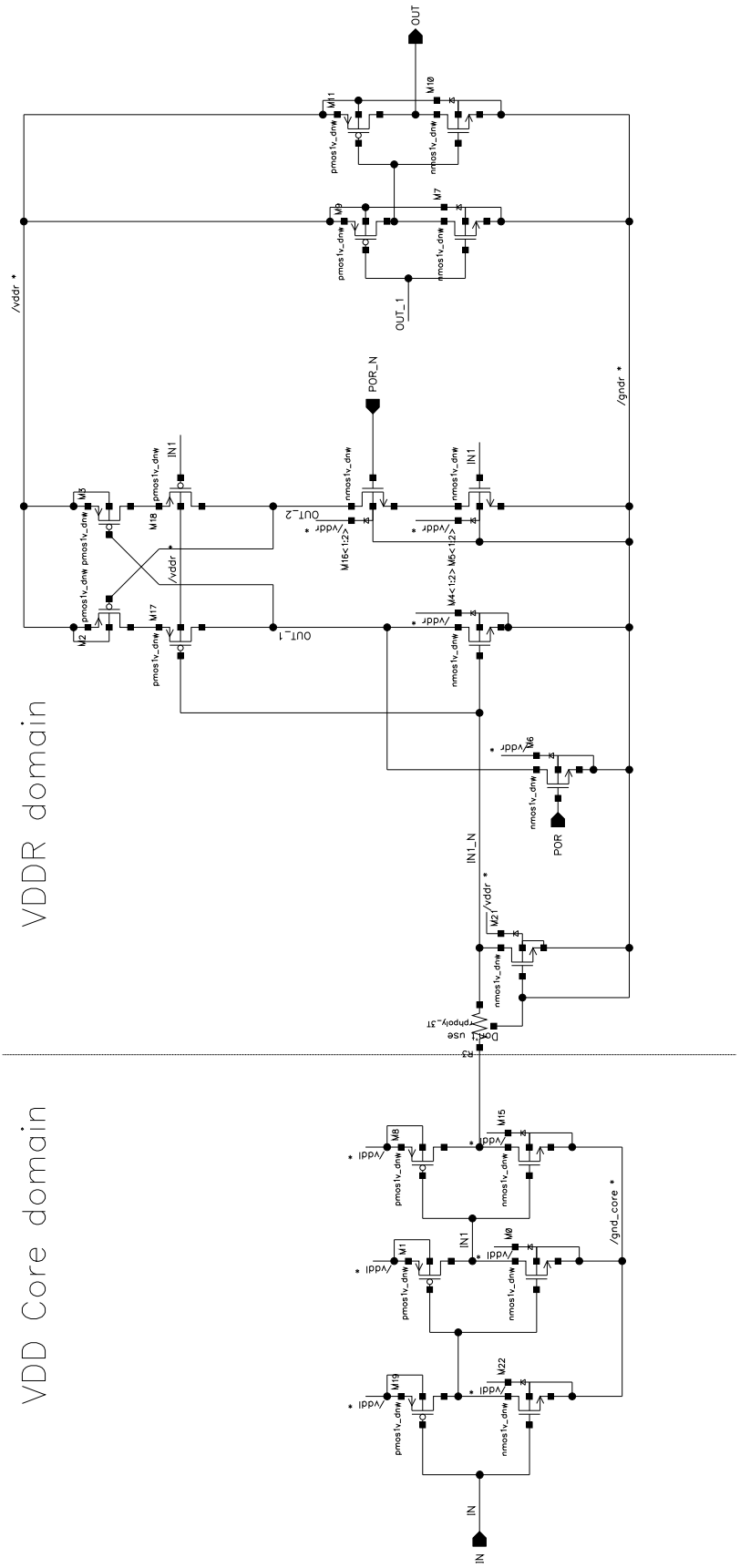

Figure 94: Level shifter with the failsafe ESD protection.

6.3 Implementation of I3C_Fm+_3V3 option

The major differences to the I3C_Fm+_1V2 are the exchanged Schmitt trigger block, the output driver, the different supply concept, and the circuit for the *FSC_DEL* signal. The supply concept contains a 3.3 V rail including *vddr3V3* and *vddo3V3* and a 1.2 V supply including *vddr1V2*. The input Schmitt trigger is connected to *vddr3V3* and the *vddr1V2* rail. The transition between the 3.3 V and 1.2 V domain is made at the output inverter of the Schmitt trigger. Furthermore, the output driver is replaced by the 3.3 V option. As mentioned in Chapter 5.4.3, the output driver requires the signal *FSC_DEL* to get rid of the current spike while *vddr1V2* is ramping up. In Table 15 all results are within the limits and are marked with PASS. Since the bus voltage is now 3.3 V, the specification limits for certain parameters must be adjusted. For the I3C DC specification parameters, the specification limits are used for $V_{DD} > 1.4$ V [9][p. 136]. For the I2C DC parameters, the specification limits are used for $V_{DD} > 2$ V [5][p. 43]. In addition, the simulation results for the various load conditions are visible in Tables 16 and 17.

			Parameters	Spec	PASS/FAIL	tm	MIN	MAX	Mean	Std. dev	Cpk
DC parameters	I3C		I_i	< 10 uA	PASS	103.1 pA	1.38 pA	1.21 µA	82.52 nA	55.04 nA	
			I_{IN_FS}	< 10 uA	PASS	18.57 nA	13.44 nA	1.31 uA	128.6 nA	55.31 nA	
			C_i	< 5 pF	PASS	2.78 pF	2.42 pF	3.16 pF	2.84 pF	132.4 fF	
			V_{OL}	< 270 mV	PASS	56.25 mV	44.67 mV	91.04 mV	83.92 mV	1.52 mV	40.7
			V_{OH}	> 810 mV	PASS	3.21 V	2.83 V	3.57 V	3.56 V	8.79 mV	
			I_{OL}	> 3 mA	PASS	13.48 mA	8.37 mA	17.15 mA	9.10 mA	176.6 µA	11.5
			I_{OH}	< -3 mA	PASS	-8.85 mA	-12.71 mA	-5.56 mA	-10.72 mA	1.19 mA	2.16
			$V_{TH\_LH\_rel}$	< 70 %	PASS	59.99 %	56.22 %	64.21 %	61.43 %	554.8 m%	5.15
			$V_{TH\_HL\_rel}$	< 70 %	PASS	38.45 %	33.94 %	42.71 %	38.08 %	545.6 m%	4.94
			V_{HYST_rel}	> 10 %	PASS	21.54 %	19.36 %	23.6 %	20.36 %	257.7 m%	13.4
	I2C	Fm	I_{OL}	> 3 mA	PASS	18.75 mA	11.67 mA	24.03 mA	12.74 mA	265.1 µA	12.2
			V_{OL}	< 594 mV	PASS	56.25 mV	44.67 mV	91.04 mV	83.92 mV	1.52 mV	
		Fm+	I_{OL}	> 20 mA	PASS	56.83 mA	35.43 mA	72.77 mA	38.66 mA	803.1 µA	7.75
			V_{OL}	< 594 mV	PASS	18.44 mV	14.7 mV	29.54 mV	27.31 mV	477.9 µV	
Timing parameters	I3C		t_{sCO_rise}	< 12 ns	PASS	7.17 ns	5.89 ns	10.17 ns	8.16 ns	114.3 ps	11.2
			t_{sCO_fall}	< 12 ns	PASS	7.42 ns	6.2 ns	10.55 ns	8.47 ns	121.1 ps	9.7
			t_{CR}	< 12 ns	PASS	1.83 ns	1.24 ns	3.0 ns	1.72 ns	153.8 ps	22.3
			t_{CF}	<12 ns	PASS	1.9 ns	1.53 ns	2.76 ns	2.46 ns	70.92 ps	44.8
	I2C	Fm	t_{fCL}	10.8 - 300 ns	PASS	24.55 ns	14.01 ns	52.58 ns	23.34 ns	1.84 ns	
			t_{VD_rise}	< 450 ns	PASS	68.84 ns	59.5 ns	73.37 ns	64.73 ns	709.9 ps	
			t_{VD_fall}	< 450 ns	PASS	61.93 ns	33.37 ns	133.4 ns	59.9 ns	4.5 ns	
		Fm+	t_{fCL}	10.8 - 300 ns	PASS	23.74 ns	13.58 ns	50.12 ns	22.74 ns	1.79 ns	
			t_{VD_rise}	< 450 ns	PASS	73.61 ns	70.28 ns	78.58 ns	73.37 ns	296.2 ps	
			t_{VD_fall}	< 450 ns	PASS	63.75 ns	38.23 ns	130.3 ns	62.88 ns	4.23 ns	

Table 15: Simulation results of the I3C_Fm+_3V3 I/O option.

			$C_{BUS} = 10$ pF, $R_{PU} = 20$ kΩ			$C_{BUS} = 10$ pF, $R_{PU} = 2.4$ kΩ			$C_{BUS} = 380$ pF, $R_{PU} = 800$ Ω		
Parameters	Spec	PASS/FAIL	tm	MIN	MAX	tm	MIN	MAX	tm	MIN	MAX
t_{fCL}	10.8 - 300 ns	PASS	22.67 ns	15.91 ns	37.64 ns	23.7 ns	16.46 ns	40.17 ns	29.36 ns	22.07 ns	47.24 ns
t_{rCL}	$<$ 300 ns	PASS	213.1 ns	208.8 ns	217.6 ns	26.7 ns	26.13 ns	27.31 ns	259.3 ns	259.1 ns	259.5 ns
t_{VD_rise}	$<$ 450 ns	PASS	321.8 ns	312.1 ns	332.7 ns	42.43 ns	39.85 ns	45.9 ns	364.7 ns	360.4 ns	368.1 ns
t_{VD_fall}	$<$ 450 ns	PASS	54.52 ns	38.39 ns	89.36 ns	56.37 ns	39.37 ns	94.11 ns	82.87 ns	61.55 ns	132.5 ns

Table 16: Timing simulation results of the Fm driver for different load conditions.

			$C_{BUS} = 10$ pF, $R_{PU} = 9$ kΩ			$C_{BUS} = 540$ pF, $R_{PU} = 250$ Ω		
Parameters	Spec	PASS/FAIL	tm	MIN	MAX	tm	MIN	MAX
t_{fCL}	10.8 - 300 ns	PASS	22.85 ns	16.04 ns	38.0 ns	26.59 ns	18.99 ns	44.6 ns
t_{rCL}	$<$ 120 ns	PASS	95.95 ns	93.98 ns	97.98 ns	114.9 ns	114.9 ns	115 ns
t_{VD_rise}	$<$ 450 ns	PASS	155.4 ns	150.5 ns	162.2 ns	168.9 ns	167 ns	171.2 ns
t_{VD_fall}	$<$ 450 ns	PASS	59.54 ns	43.51 ns	93.98 ns	78.56 ns	57.17 ns	126.7 ns

Table 17: Timing simulation results of the Fm+ driver for different load conditions.

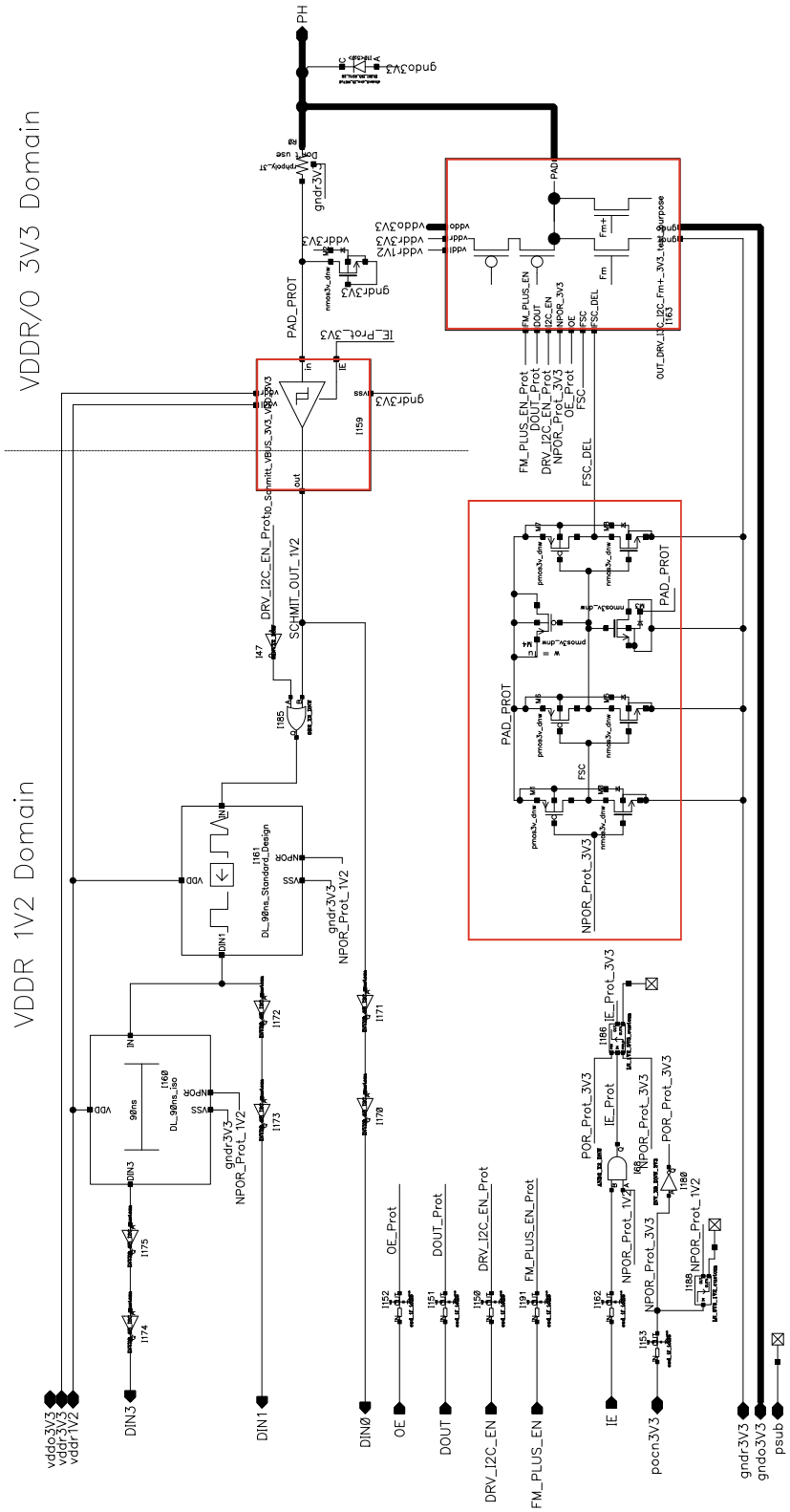

Figure 95: Top level schematic of the I3C_Fm+_3V3 option.

6.4 I3C_Fm+_3V3_V_B3V3 option

In the same manner, the I3C_Fm+_3V3_V_B3V3 option is implemented. Again the output driver was replaced by the inherent failsafe block with only one PMOS transistor for the I3C mode. In addition, the ESD interface cells must assure failsafe functionality as well. They are replaced by a poly resistor with a GGNMOS for all inputs of the I3C I/O. The results show expected results, which means that all results are within the specification limits shown in Table 18.

			Parameters	Spec	PASS/FAIL	tm	MIN	MAX	Mean	Std. dev	Cpk
DC parameters	I3C		I_i	< 10 uA	PASS	100.5 pF	831 fF	1.21 µA	31.82 nA	55.16 nA	
			I_{IN_FS}	< 10 uA	PASS	101.6 pA	3 pA	1.21 uA	61.91 nA	55.31 nA	
			C_i	< 5 pF	PASS	2.71 pF	2.37 pF	3.07 pF	2.73 pF	157.2 fF	
			V_{OL}	< 270 mV	PASS	63.91 mV	50.71 mV	103.7 mV	71.29 mV	1.75 mV	
			V_{OH}	> 810 mV	PASS	3.22 V	2.84 V	3.58 V	3.21 V	7.8 mV	
			I_{OL}	> 3 mA	PASS	11.8 mA	7.37 mA	15.12 mA	11.39 mA	155.7 µA	10.7
			I_{OH}	< -3 mA	PASS	-9.88 mA	-14.2 mA	-6.19 mA	-9.42 mA	1.35 mA	2.2
			$V_{TH\_LH\_rel}$	< 70%	PASS	59.99 %	56.22 %	64.21 %	59.92	554.8 m%	5.15
			$V_{TH\_HL\_rel}$	< 70%	PASS	38.45%	33.95 %	42.71 %	38.65 %	545.6 m%	4.94
			V_{HYST_rel}	> 10%	PASS	21.54%	19.36 %	23.6 %	21.27 %	257.7 m%	13.4
	I2C	Fm	I_{OL}	> 3 mA	PASS	16.53 mA	10.28 mA	21.19 mA	17.96 mA	265.1 µA	12.2
			V_{OL}	< 594mV	PASS	63.91 mV	50.71 mV	103.7 mV	62.72 mV	1.52 mV	
		Fm+	I_{OL}	> 20 mA	PASS	50.1 mA	31.23 mA	64.15 mA	54.43 mA	803.1 µA	7.75
			V_{OL}	< 594 mV	PASS	mV	mV	mV	mV	µV	
Timing parameters	I3C		t_{sCO_rise}	< 12 ns	PASS	7.44 ns	6.08 ns	10.78 ns	7.34 ns	114.3 ps	11.2
			t_{sCO_fall}	< 12 ns	PASS	7.45 ns	6.08 ns	10.78 ns	7.61 ns	121.1 ps	9.7
			t_{CR}	< 12 ns	PASS	1.94 ns	1.35 ns	3.14 ns	2.01 ns	153.8 ps	22.3
			t_{CF}	<12 ns	PASS	2.15 ns	1.73 ns	3.14 ns	2.02 ns	70.92 ps	44.8
	I2C	Fm	t_{fCL}	10.8 - 300 ns	PASS	24.69 ns	14.08 ns	52.9 ns	27.46 ns	1.84 ns	
			t_{VD_rise}	< 450 ns	PASS	65.77 ns	59.22 ns	73.83 ns	65.75 ns	709.9 ps	
			t_{VD_fall}	< 450 ns	PASS	62.56 ns	33.66 ns	134.9 ns	68.38 ns	4.5 ns	
		Fm+	t_{fCL}	10.8 - 300 ns	PASS	23.72 ns	13.56 ns	50.16 ns	26.42 ns	1.79 ns	
			t_{VD_rise}	< 450 ns	PASS	73.76 ns	70.28 ns	79.4 ns	73.72 ns	296.2 ps	
			t_{VD_fall}	< 450 ns	PASS	64.1 ns	38.39 ns	131.3 ns	69.52 ns	4.23 ns	

Table 18: Simulation results of the I3C_Fm+_3V3_V_B3V3 option.

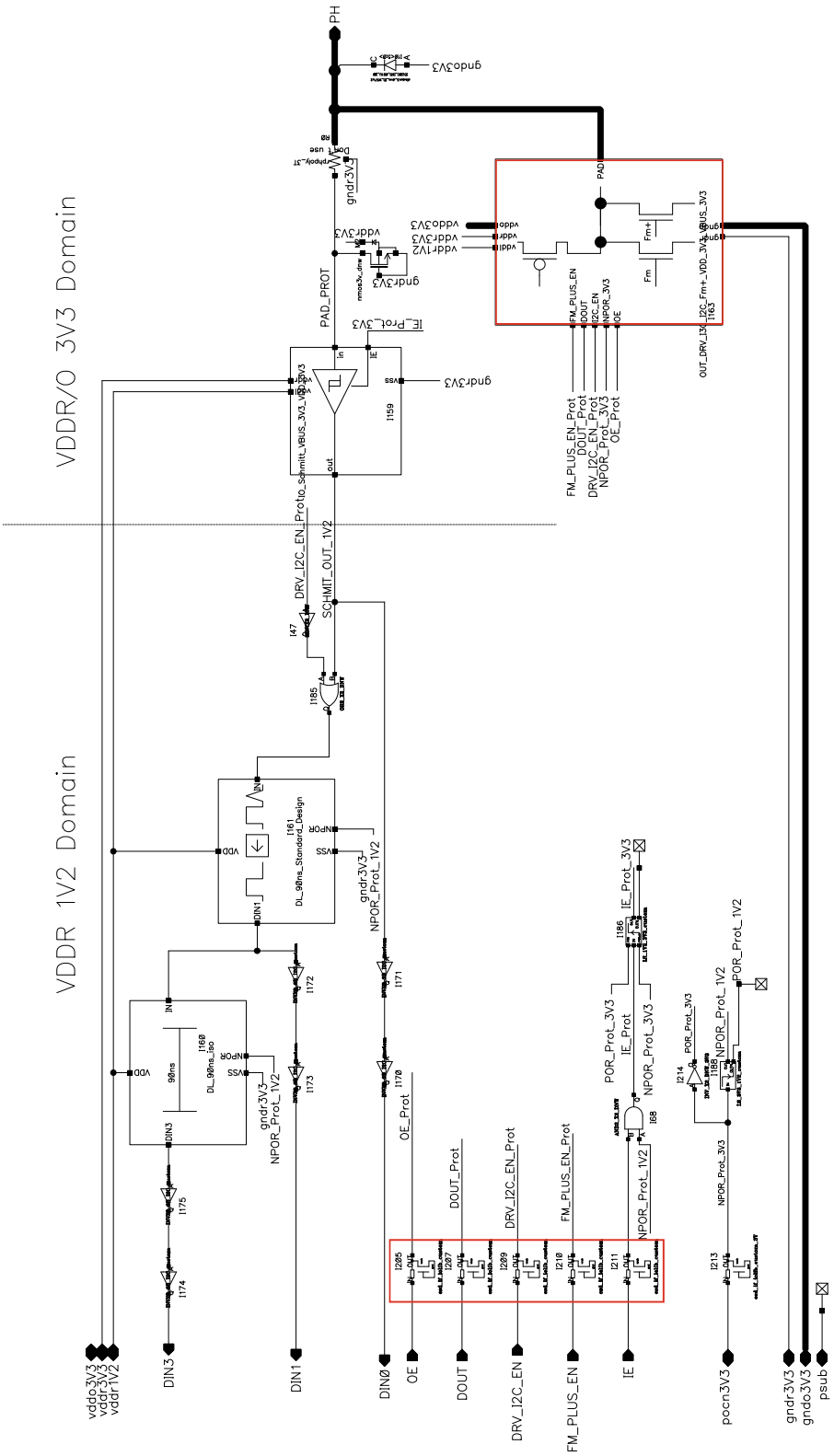

Figure 96: Top level schematic of the I3C_Fm+_3V3_V$_B$3V3 option.

6.5 I3C_Fm+_3V3_V_B1V8 option

During the development of this option, it was concluded, that this option has no practical sense since three different supply voltages are needed: A 1.2 V core supply, a 3.3 V supply voltage, and a 1.8 V supply for the output driver. Since three different supply voltages for an I/O are not common, this option can be neglected.

			Parameters	Spec	PASS/FAIL	tm	MIN	MAX	Mean	Std. dev	Cpk
DC parameters	I3C		I_i	< 5 uA	PASS	62.81 pA	889 fA	194.1 nA	14.77 nA	8.29 nA	
			I_{IN_FS}	<5 uA	PASS	105 pA	10.4 pA	1.4 uA	14.83 nA	8.31 nA	
			C_i	< 5 pF	PASS	2.7 pF	2.4 pF	3.16 pF	2.85 pF	385.5 fF	
			V_{OL}	< 270 mV	PASS	63.91 mV	50.71 mV	103.7 mV	95.75 mV	2.15 mV	
			V_{OH}	> 810 mV	PASS	1.733 V	1.5 V	1.94 V	1.71 V	5 mV V	
			I_{OL}	> 3 mA	PASS	11.88 mA	7.37 mA	15.12 mA	8.0 mA	189.9 µA	8.77
			I_{OH}	< -3 mA	PASS	-10.57 mA	-17.18 mA	-5.9 mA	-13.24 mA	1.28 mA	2.65
			$V_{TH\_LH\_rel}$	< 70%	PASS	57.85 %	44.73 %	61.96 %	57.05	1.45 %	1.85
			$V_{TH\_HL\_rel}$	< 70%	PASS	40.35%	32.26 %	46.49 %	36.03 %	783.5 m%	2.57
			V_{HYST_rel}	> 10%	PASS	17.5 %	12.47 %	22.95 %	15.34 %	648.4 m%	2.74
	I2C	Fm	I_{OL}	> 3 mA	PASS	16.53 mA	10.28 mA	21.19 mA	11.19 mA	285.2 µA	9.57
			V_{OL}	< 324 mV	PASS	63.91 mV	50.71 mV	103.7 mV	95.75 mV	2.15 mV	
		Fm+	I_{OL}	> 20 mA	PASS	50.1 mA	31.23 mA	64.15 mA	33.97 mA	864 µA	5.39
			V_{OL}	< 324 mV	PASS	20.93 mV	16.68 mV	33.55 mV	31.08 mV	668.2 µV	
Timing parameters	I3C		t_{sCO_rise}	< 12 ns	NEAR	8.16 ns	5.97 ns	12.21 ns	9.7 ns	116.5 ps	6.59
			t_{sCO_fall}	< 12 ns	NEAR	8.05 ns	5.85 ns	12.24 ns	9.64 ns	118.4 ps	6.64
			t_{CR}	< 12 ns	PASS	1.984 ns	1.18 ns	3.55 ns	2.48 ns	157 ps	20.2
			t_{CF}	<12 ns	PASS	1.42 ns	1.02 ns	2.39 ns	2.06 ns	65.59 ps	50.5
	I2C	Fm	t_{fCL}	5.89 - 300 ns	PASS	14.04 ns	6.8 ns	36.39 ns	24.02 ns	1.25 ns	
			t_{VD_rise}	< 450 ns	PASS	66.79 ns	52.82 ns	82.76 ns	65.41 ns	769 ps	
			t_{VD_fall}	< 450 ns	PASS	45.26 ns	13.07 ns	118 ns	51.66 ns	3.4 ns	
		Fm+	t_{fCL}	5.89 - 300 ns	PASS	13.25 ns	6.28 ns	34.09 ns	22.34 ns	1.21 ns	
			t_{VD_rise}	< 450 ns	PASS	75.9 ns	69.86 ns	84.09 ns	76.15 ns	244.9 ps	
			t_{VD_fall}	< 450 ns	PASS	48.02 ns	23.5 ns	110.1 ns	52.59 ns	3.14 ns	

Table 19: Simulation results of the I3C_Fm+_3V3_V_B1V8 option.

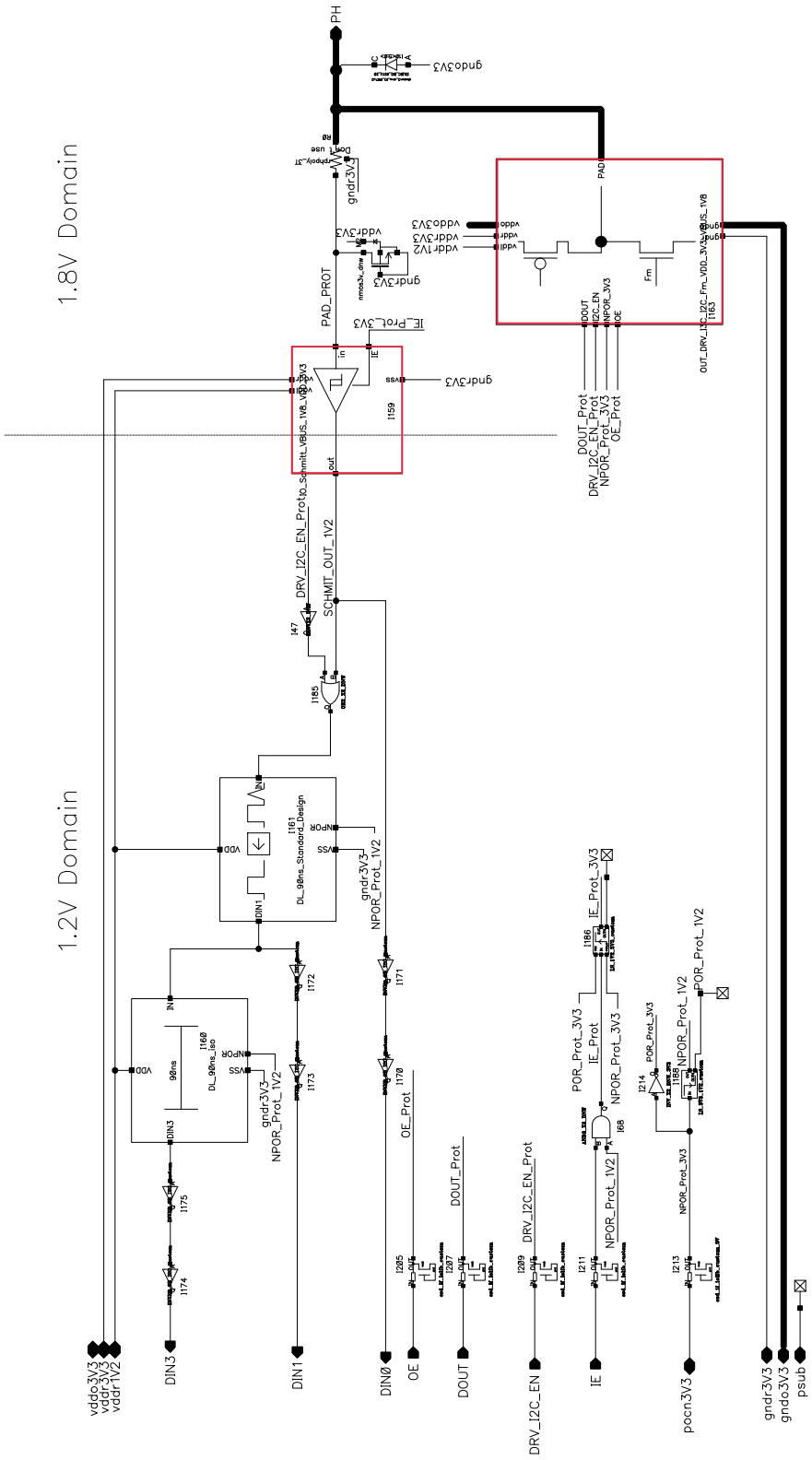

Figure 97: Top level schematic of the I3C_Fm+_3V3_V_B1V8 option.

7 Results and Discussion

In order to discuss the results of this thesis, a layout analysis of the implemented I/O variants from Chapter 6 is accomplished. This layout analysis is only an estimation of the required area. This area estimation will differ from a final layout, which may be accomplished in the future. By placing the components of each variant in the layout tool the area was estimated by considering the PR boundary box with a cell density placement of 70 %. The results of this area estimation are presented in Table 20 for the 1.2 V I/O options and Table 21 for the 3.3 V I/O options. The I3C_Fm+_3V3_V$_B$1V8 option is not suitable for practical use and as it did not fulfill the specification requirements, this option was not considered for the layout comparison. The I3C_Fm+_3V3_V$_B$1V8 option requires a $VDDIO = 1.8$ V, a 1.2 V core supply, and a 3.3 V supply voltage. It is an uncommon practice to provide three voltage domains to the I/O.

Table 20 shows the area estimation of the individual blocks, the additional devices needed on the top level of the I/O variant, and the total area. Additional Devices include a level shifter, ESD protection, and additional logic cells. For Table 20 and Table 21 the relative change in the area to the I3C_Fm_1V2/3V3 variant is calculated.
Analyzing the data in Table 20 it can be concluded, that the output driver consumes the most area of all blocks. The output driver of the I3C_Fm+_1V2 design is 17.63 % larger than the I3C_Fm_1V2 design. As it was introduced in Chapter 5.5.5, the total width of the ESD NMOS transistors is determined by ESD experts, to achieve a 4 kV HBM requirement. However, the width is not achieved with the Fm and Fm+ drivers and dummy transistors must be added. In addition, the I3C_Fm+_1V2 option requires an additional slope control which includes an additional MIM capacitor. This is the reason why the I3C_Fm+_1V2 option is 17.63 % larger than the I3C_Fm_1V2 option. Summing up, the I3C_Fm+_1V2 can be merged with the I3C_Fm_1V2 variant. Comparing now the failsafe option I3C_Fm_1V2 with the inherent failsafe concept of option I3C_Fm+_1V2_V$_B$1V2, the result was different from the expectation. The expected result was a significant area reduction by using an inherent failsafe concept. As it is presented in Table 20 the inherent output driver is 14.16 % smaller than the I3C_Fm_1V2 option, though the area of the additional devices doubled. This is because additional level shifters are required for all inputs of the inherent failsafe options. An inherent failsafe concept for the 1.2 V option is not meaningful in saving area. Heading now to the results of the table, 21 a total area of 25.81 % with an inherent failsafe concept of the I3C_Fm_3V3_V$_B$3V3 option can be saved. The area of the required additional devices on the top-level stays approximately the same for all variants.

Block names	I3C_Fm_1V2	I3C_Fm+_1V2		I3C_Fm_1V2_V_B_1V2		I3C_Fm+_1V2_V_B_1V2	
	Base Design	(μm^2)	Rel to Base (%)	Abs (μm^2)	Rel to Base (%)	Abs (μm^2)	Rel to Base (%)
Output driver	8064	9486	17.63	5745	-28.76	6922	-14.16
Glitch Filter	922	922	0	922	0	922	0
Schmitt trigger	549	549	0	549	0	549	0
Delay block	961	961	0	961	0	961	0
Additional devices	2431	2449	0.74	4979	104.8	5800	138.6
Total area	12927	14367	11.14	13156	1.77	14884	15.14

Table 20: Area estimation of 1.2 V I/O options with relative change to I3C_Fm_1V2 variant.

Block names	I3C_Fm_3V3	I3C_Fm+_3V3		I3C_Fm_3V3_V_B_3V3		I3C_Fm+_3V3_V_B_3V3	
	Base Design	(μm^2)	Rel to Base (%)	Abs (μm^2)	Rel to Base (%)	Abs (μm^2)	Rel to Base (%)
Output driver	12409	14304	15.27	7938	-36.0	9584	-22.76
Glitch Filter	922	922	0	922	0	922	0
Schmitt rigger	635	635	0	635	0	635	0
Delay block	961	961	0	961	0	961	0
Additional devices	3487	3256	-6.62	3186	-8.63	3249	-6.83
Total area	18144	20078	10.66	13642	-25.81	15351	-15.39

Table 21: Area estimation of 3.3 V I/O options with relative change to I3C_Fm_3V3 variant.

8 Conclusion

The aim of this thesis was to determine the feasibility of modular I3C I/O development and the economic benefits that such a modular design could possibly bring. The first economic question focuses on the area reduction with the usage of a modular system. As the results of the layout comparison showed, an inherent failsafe concept for a 3.3 V I/O can reduce the area consumption. Subsequently, to the first economical question, another research question is: How complex must the modularity principle for an I3C I/O be for it to make economic sense? Given the complexity of the modular system, there is no point in developing more complex modular blocks as there is no economic benefit to be gained. Because customer requests can vary widely, it makes no sense to add complexity by adding features.
The last question to be answered is: Is it possible to decrease the development time with this modularity principle? The starting assumption is that the modular concept can not cover all individual design requests. A simple way of achieving reusability is preferable when it comes to analog circuit design. For individual customer requests the design has to be modified anyhow. Nevertheless, the modular system can be a good starting point for the modified design. The modular concept is developed to reuse the I3C I/O easily. In addition, the more variants there are, the better impact the modular concept has over development time. One example would be the development of the I3C_Fm_1V2 out of the I3C_Fm+_1V2 option. This development is very efficient since the Fm+ driver extension can be simply removed and the next variant is ready and functional.
Finally, this thesis fills the gap in the literature regarding the development of I3C I/O structures. I/Os are generally an underestimated and undesired topic. However, each IC requires one or multiple I/Os. This thesis introduces a structured guideline for the development of an I3C I/O. In addition, the I3C I/O development was optimized by applying a modular concept, resulting in saving area, development time, and finally cost.

9 Outlook

The first further improvement of this work would be the optimization of the inherent 1.2 V variant. The implemented level shifter used for each input can be further optimized to save area, even for static configuration signals. An additional step to minimize the area is the optimization of the ESD secondary protection. For future work, ESD protection can be added to the modular blocks, to fulfill different ESD criteria. For different applications, different ESD criteria may be required. For this thesis, a 4 kV HBM requirement was needed. In the future, different ESD modules could be developed to satisfy various ESD requirements. Going forward, a layout may be done from this thesis. To save the layout design time, the individual blocks from Table 20 can be arranged on a grid with a fixed position, so they can exchanged by another module. With the modular output driver, the length of the I3C I/O can be varied, as depicted in Figure 98. The width of the pad-limited design is based on the widest block of the I3C I/O, like the output driver. A possible next development step based on this thesis, would be the design of a pure I3C I/O without I2C backward compatibility. A huge advantage would be a further decrease in area, since the glitch filter, the delay block, and the I2C slope control can be removed. With this modular approach, a pure I3C I/O is simple to implement. Furthermore, a pure I2C Pad can also be derived from the work of this thesis. In this thesis, no layout of the pad variants was accomplished, but the decrease in development time can be also related to the layout. If the individual blocks stated in Table 20 and Table 21 are placed in the layout that they can be easily exchanged, the development time can be further decreased.

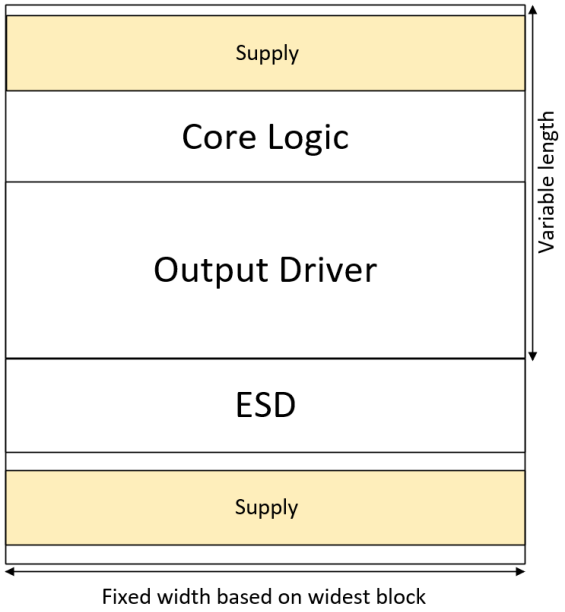

Figure 98: A floorplan of the pad-limited I3C I/O with a variable length.

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